

An X- and Ku-Band Wideband Recursive Receiver MMIC With Gain-Reuse

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Abstract—This paper presents an 8–18 GHz wideband receiver with recursive super-heterodyne topology. A multi-feedback technology is utilized in the LNA design for the input matching over the wide frequency range in X- and Ku-band. In order to save power, both the RF and IF signals share a tunable transconductance stage. The IF output of the first mixer is fed back into the tunable input stage for IF amplification in a recursive manner, which significantly enhances the gain tuning without increasing the power. The wideband receiver MMIC is implemented in a 0.13 μm SiGe BiCMOS technology and achieves a 6.7–7.8 dB noise figure. The receiver average gain over the frequency range is measured as 53 dB maximum gain with 20 dB continual tuning and 36 dB discrete tuning. The average output P1dB over the frequency range is measured as -10 dBm at maximum gain. The receiver dissipates only 180 mW with a 2.2 V power supply.

Index Terms—BiCMOS, gain reuse, Ku-band receiver, SiGe, X-band.

I. INTRODUCTION

THE development of modern radar and wireless applications require next generation receivers to achieve wideband frequency range and low power consumption. The proposed recursive X- and Ku-band receiver can be widely used in radar, satellite communication, direct broadcast satellite (DBS), ultra-wide-band (UWB) [1] and software-defined radio [2] applications. The proposed architecture can be certainly extended to other frequency bands for a wide range of applications. Conventional radar transceiver (TR) modules are constructed with discrete analog components. Because analog components are sensitive to temperature, supply voltage and semiconductor processing variations, the performance of discrete analog radar TR module is very limited and power hungry. Integrated single-chip radar is capable of supporting the required functions in a variety of commercial and military applications. As an example, an integrated portable radar TR module can be used in an unmanned aerial vehicle (UAV) for surveillance. The proposed low power X- and Ku-band receiver is a good candidate for use in the single chip radar. In satellite communication and broadcasting, a low power X- and Ku-band receiver can directly receive and down-convert the received signal.

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The aim of this work is to produce a compact, low power and inexpensive wideband receiver for portable digital wideband radars and other wireless applications. Wideband receiver MMICs with coverage of the entire X-band and Ku-band have been published recently [3], [4]. However, their commercial applications are limited due to their high cost, high power consumption and large size. These limitations result from the use of expensive and power-hungry III-V technologies that are not compatible with silicon baseband integrations. The integration of wideband RF blocks with baseband processors on a commercially available silicon technology will greatly reduce the overall system cost. Silicon-germanium (SiGe) Heterojunction Bipolar Transistor (HBT) BiCMOS technology is an excellent platform that utilizes bandgap engineering to improve transistor performance while maintaining compatibility with low cost CMOS baseband implantations [5]. Also, improvements in advanced SiGe HBT BiCMOS technology yield low cost, high integration and excellent performance including faster device and low noise figure. The receiver presented in this paper is implemented in a commercial SiGe HBT BiCMOS technology featuring a 0.12 μm lithography, a peak cutoff frequency (f_T) of 200 GHz and a maximum oscillation frequency (f_{max}) of 250 GHz.

In the proposed receiver design, a multi-feedback topology [6], [7] in conjunction with inductive compensation is applied to the low-noise amplifier (LNA) design to achieve wideband operation. Gain reuse topology that employs recursive signal amplification through the same transconductance was first proposed in an integrated form for direct-conversion or low-IF type implementations in [8]. For the super-heterodyne mixing stages in our design, the gain reuse topology is chosen. In addition, a current steering gain adjustment approach is applied to the Gm stage [9]. Thus, the Gm stage not only operates as an input stage for two mixers, but also as a variable gain amplifier (VGA). The VGA simultaneously adjusts the RF and IF signals utilizing the wide bandwidth of the Gm stage and sufficient separation between RF and IF frequencies. With recursive gain adjustment, the proposed super-heterodyne receiver simultaneously achieves tunability enhancement and power reduction.

The phased array receiver based on SiGe BiCMOS technology in [10] shows excellent performance in X- and Ku-band frequency range. However, there is no frequency translation realized in their receiver. In this paper, the wideband receiver MMIC is implemented in a 0.13 μm SiGe BiCMOS technology and achieves a 6.7–7.8 dB noise figure in the 8–18 GHz frequency band that covers the entire X- and Ku-bands. The maximum voltage gain of the receiver is measured as 53 dB. The average output P1dB is about -10 dBm at maximum gain over the entire operational frequency range. The receiver

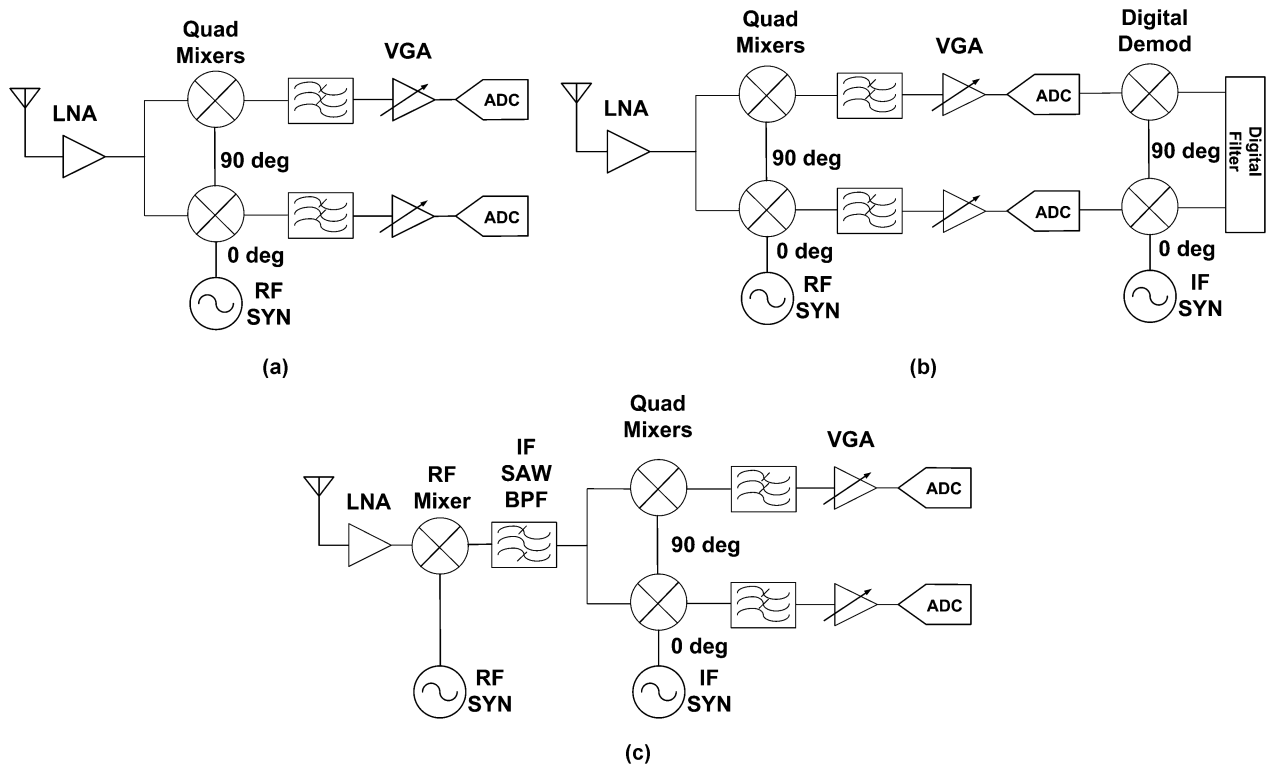


Fig. 1. Basic receiver architectures. (a) Direct conversion receiver. (b) Low-IF receiver. (c) Super-heterodyne receiver.

MMIC occupies 1.81 mm^2 and dissipates 180 mW with a 2.2 V power supply in maximum gain mode.

This paper is organized as follows. The proposed receiver architecture and design considerations are summarized in Section II. In Section III, the receiver circuit design details are discussed, and the wideband LNA and the recursive gain reuse topologies are addressed. Section IV summarizes the experimental results of the implemented receiver. Conclusions are presented in Section V.

II. RECEIVER ARCHITECTURE DESIGN

In modern wireless receiver design, there are three common architectures: direct conversion [11], [12], super-heterodyne [13], [14] and low intermediate frequency (low IF) [15], as shown in Fig. 1.

For applications with high performance requirements, the super-heterodyne architecture is normally the first choice due to the attendant low design risk [13], [14]. However, the main disadvantages of this architecture are the high cost and high power consumption [16], since this architecture requires more than one mixer and usually multiple VGAs, thereby consuming more power when compared with other receivers. This characteristic makes the super-heterodyne architecture unsuitable for low power applications. Another issue introduced by the super-heterodyne architecture is the image signal, which must be removed in order to prevent degrading the sensitivity of the receiver.

In order to achieve good performance at a high operating frequency and relax the requirements on the ADC, the super-heterodyne architecture is chosen in the proposed receiver. In addition, some particular techniques including wideband LNA and recursive gain re-use topology are applied to the receiver cir-

cuit design in order to overcome the natural drawbacks of the super-heterodyne receiver.

Fig. 2 illustrates the system block diagram of the proposed wideband recursive receiver, which consists of a wideband LNA, two mixers, internal and external filters, and a baseband VGA. The input X-band and Ku-band RF signals are amplified by the wideband LNA. The amplified RF signal is adjusted in the Gm/VGA cell and then down converted to the first IF (IF1). The first IF output is fed back to the input of the same Gm stage through an external surface acoustic wave (SAW) filter. Thanks to the high performance of the SiGe HBT technology, a very wide gain bandwidth can be easily achieved in the Gm/VGA stage. Fig. 3 shows the simulated frequency response of the tunable Gm stage at different gain settings. As shown, the gain bandwidth of the Gm stage is approximately 83 GHz at different gain modes. This gain bandwidth is wide enough to adjust both RF and IF1 signals so that both signals can share the unique gain stage. After re-amplification, the first IF signal is down converted again to the second IF (IF2), which is adjusted in the baseband VGA and then quantized by the ADC.

In order to overcome the disadvantages of a super-heterodyne architecture, the following design issues are addressed.

- 1) To save cost, the proposed receiver, especially the input LNA, can operate over a wide frequency range without splitting the frequency band into a number of sub-bands. This leads to a compact and power-saving implementation.
- 2) The issue of high power consumption is addressed by the gain re-use topology, which is applied to the super-heterodyne mixing stages. The recursive gain re-use topology makes it possible to achieve multiple functions in a unique stage for power and cost saving purposes.

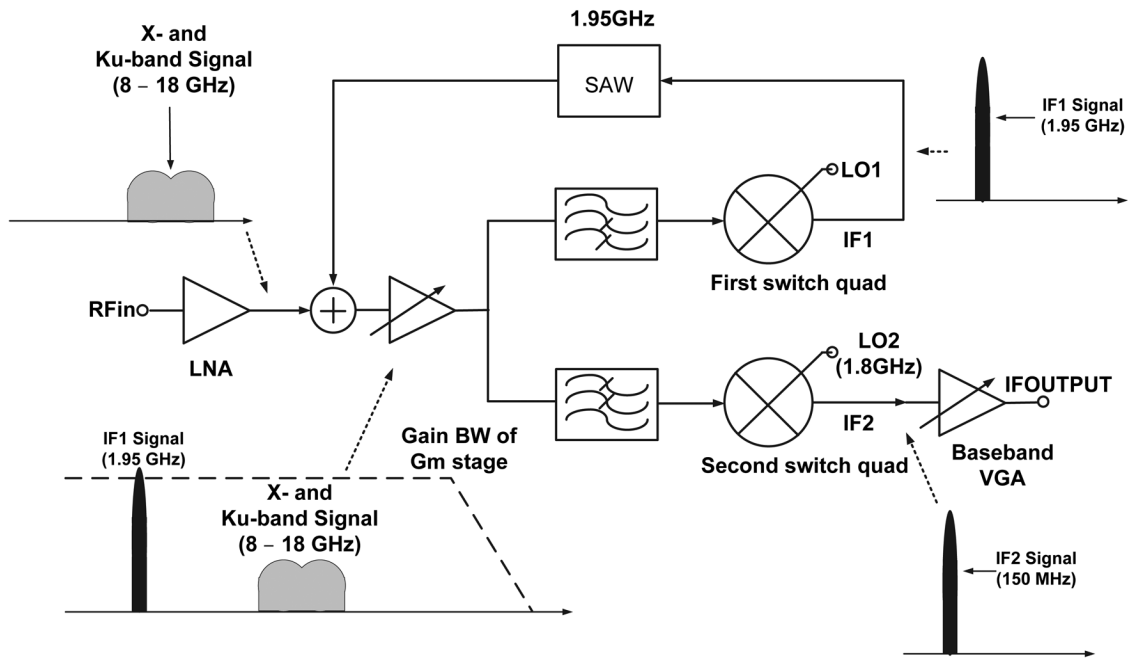


Fig. 2. Block diagram of the wideband recursive receiver.

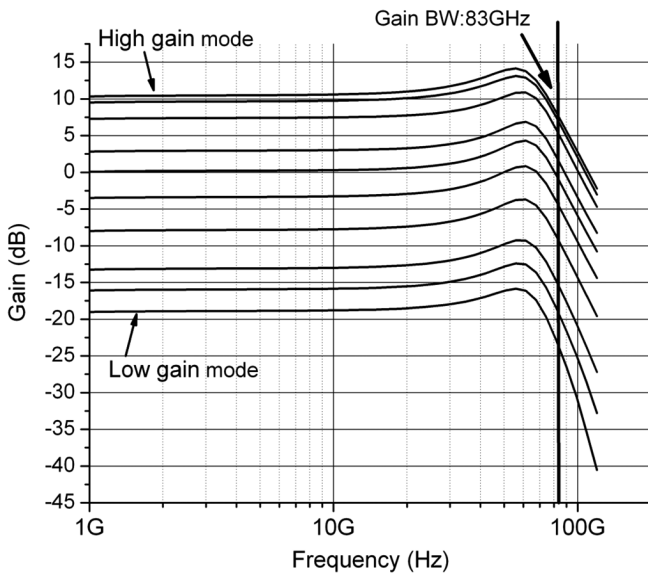


Fig. 3. Simulated frequency response of tunable Gm stage.

- 3) The image signal is removed by employing an external SAW filter in the feedback loop. For some applications that experience large jamming signals, especially for radar, it's often difficult to remove the image and jamming signals using an on-chip filter due to the poor quality factor of the inductor. For additional image-rejection and channel filtering, the receiver chip provides an option of routing the signal through the off-chip filter which also provides access to the RF and IF signals for separate testing purposes.
- 4) The issue of local oscillator (LO) leakage is eliminated by using cascode LNA and Gm/VGA circuits that provide high isolation between input and output. In addition, deep

trench (DT) isolation rings were located around each cell and critical transistors to suppress substrate crosstalk.

- 5) A double-balanced configuration is chosen in the mixer design to eliminate even-order distortion, thus relaxing the half-IF issue in the receiver [16]. In addition, careful layout including symmetric tracing of differential signals, also helps suppress the even-order distortion.

III. RECEIVER CIRCUIT DESIGN

In the following section, the building blocks of the wideband receiver are described in detail at the circuit level.

A. LNA Design

In the design of wideband LNAs in modern receivers, there are common considerations that include a low noise figure (NF), flat gain over the operating frequency range, stable input impedance matching, and sufficient linearity. Satisfying all of the design goals for the LNA over X- and Ku-bands is particularly difficult due to the high operating frequency and the broad bandwidth. A few existing topologies that can provide flat gain over a wide frequency band include an LNA using an LC-ladder matching [17], [18], distributed amplifiers [19]–[21], common-base LNAs [22], [23] and a LNA with reactive feedback [24]. However, all of these technologies have some drawbacks when they are operating in the X- and Ku-band frequency range. The LC-ladder matching technology occupies large area, and the noise figure is also large due to bulky and lossy on-chip inductors. Although distributed amplifiers can achieve the widest bandwidth, the inherent poor noise performance and large power consumption limit their application. The noise figure of the common-base LNA degrades quickly with the increase of frequency, which makes it unsuitable for X- and Ku-band application.

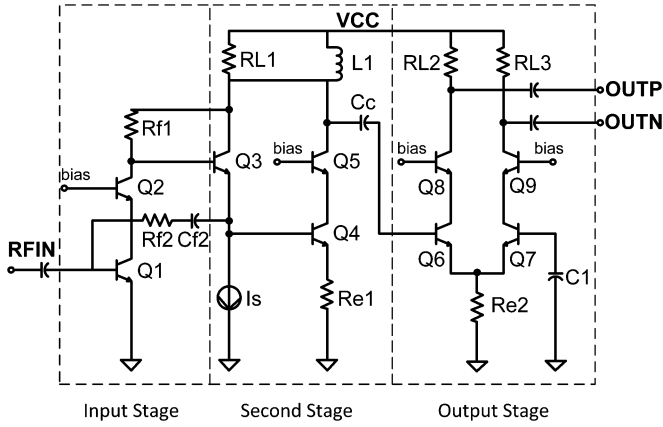


Fig. 4. Simplified schematic of the wideband LNA.

In comparison with the above LNA topologies, the shunt feedback topology is a good candidate because wideband input matching is relatively easy, chip size is small, and there is low sensitivity to process variations with the use of precision resistors [24]–[29]. However, feedback can degrade the noise figure for input matching and consume large amounts of current to achieve the desired gain, especially in CMOS technology. The SiGe HBT technology offers the advantages of excellent noise performance and an improved transconductance over CMOS devices [5]. These major advantages are employed to overcome the limitations of the shunt feedback topology. In addition, the multi-feedback topology, in conjunction with inductive compensation, is chosen in the LNA design. In comparison with [6] and [7], the proposed LNA in our design achieves higher operating frequency and wider frequency range with low NF.

A simplified schematic of the proposed wideband LNA, which consists of three stages, is shown in Fig. 4. The input stage of the LNA is a single-ended cascode amplifier which achieves simultaneous power and noise matching over the wide bandwidth. Although a differential architecture provides high linearity and common-mode rejection, a differential input makes testing very difficult when the network analyzer only supports a single-ended port. Moreover, most of antennas are single-ended, which are not compatible with the LNAs which have differential inputs. Thus, our design utilizes a single-ended input and differential output. Besides improving reverse isolation, the cascode architecture reduces the Miller capacitance of the input transistor, which degrades the wideband impedance matching.

Three different feedback paths are provided in this design to achieve the input matching: emitter degeneration feedback R_{e1} , shunt feedback R_{f1} and shunt feedback R_{f2} , as shown in Fig. 4. Among these feedback resistors, feedback resistor R_{f2} is the main component that not only determines the input impedance but also affects the overall noise figure of the amplifier.

The feedback resistor directly contributes noise to the amplifier and the noise design must carefully address mitigation of the noise contribution of the feedback resistor and reduce the overall noise figure of the LNA.

Based on noise factor equation of an N-stage system in [30], it is clearly necessary to reduce the noise of the input stage,

which is the dominate factor of the noise figure of the whole amplifier, even the whole receiver. Thus, the noise performance of the input stage is first analyzed and then combined with noise theory of shunt feedback to evaluate the overall noise figure of the LNA [31].

The input referred noise voltage $\overline{V_{Q1}^2}$ and noise current $\overline{I_{Q1}^2}$ are used to characterize the noise figure of input transistor Q1. In order to minimize the noise figure, there is no degeneration resistor located at the emitter of the input transistor Q1. On the other hand, shunt feedback resistor R_{f2} senses current and feeds it back to the input. Thus, R_{f2} affects only the input referred noise current without disturbing the input referred noise voltage.

Then the total input referred noise current can be given as

$$\overline{I_{total}^2} = \overline{I_{Q1}^2} + \frac{\overline{V_{Q1}^2}}{R_{f2}^2} + 4kT \frac{1}{R_{f2}} \Delta f \quad (1)$$

where Δf is the bandwidth of interest.

With both input referred noise current and voltage, the overall noise figure of the amplifier can be represented as follows (the noise contribution of following stages is neglected):

$$\begin{aligned} \text{NF}_{total} &= 1 + \frac{\overline{V_{Q1}^2}}{4kTR_S\Delta f} + \frac{R_S\overline{I_{Q1}^2}}{4kT\Delta f} + \frac{\overline{V_{Q1}^2}R_S}{4kTR_{f2}^2\Delta f} + \frac{R_S}{R_{f2}} \\ &= 1 + \left(r_{b1} + \frac{1}{2g_{m1}} \right) \cdot \left(\frac{1}{R_S} + \frac{R_S}{R_{f2}^2} \right) \\ &\quad + \frac{R_S}{4kT} \left(2qI_B + \frac{2qI_{C1} + \frac{4kT}{(R_{f1} + R_{L1})}}{|\beta(jf)|^2} + \frac{4kT}{R_{f2}} \right) \quad (2) \end{aligned}$$

where r_{b1} and g_{m1} represent the base resistance and transconductance of the transistor Q1, respectively. $\beta(jf)$ is the small-signal current gain, Δf is the bandwidth of interest and R_S represents the source resistance.

From (2), a relatively large value of feedback resistor R_{f2} is required in order to avoid degrading the overall noise figure. In addition, the input transistor Q1 must be sized to achieve minimum noise figure. Referring to the (2), if we further neglect the current noise contribution from the base and collector of Q1, the overall noise figure can be simplified as

$$\text{NF} = 1 + \left(r_{b1} + \frac{1}{2g_{m1}} \right) \cdot \left(\frac{1}{R_S} + \frac{R_S}{R_{f2}^2} \right). \quad (3)$$

From the above simplified expression of overall noise figure, we can see that the overall noise figure is dominated by the base resistance and bias current of Q1.

With this type of amplifier, it is advantageous to establish the feedback between the input and the emitter of Q3 instead of the collector of Q2. This topology provides some inductance at the input, which leads a better input match. Since there are several feedback paths in our design, it is very hard to derive the input impedance through general feedback theory. Therefore, direct derivation of the input impedance based on an equivalent small-signal model is performed to examine the input impedance of the wideband LNA. Fig. 5 shows the equivalent small-signal

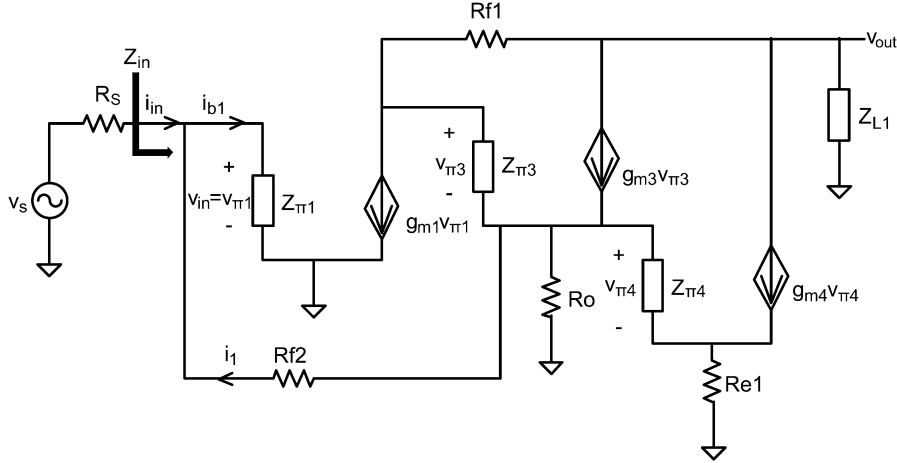


Fig. 5. Equivalent small signal model of first two stages of the wideband LNA. In the model, the cascode transistors were replaced with single common emitter transistor for simplicity.

model of the first two stages of the wideband LNA that are associated with the input impedance. In the equivalent model, cascode transistors are replaced with a single common-emitter transistor to simplify the derivation.

Referring to Fig. 5 and performing KVL law along the path from degeneration resistor R_{e1} to the input point v_{in} , $v_{\pi4}$ can be expressed as follows:

$$v_{\pi4} = \frac{i_{b1}Z_{\pi1} + i_1R_{f2}}{1 + g_{m4}R_{e1}} \quad (4)$$

where i_1 is the feedback current and g_{m4} is the transconductance of transistor Q4.

Performing KVL law along the path from degeneration resistor R_{e1} to the output point v_{out} , $v_{\pi3}$ is given as

$$(1 + g_{m3}Z_{L1})v_{\pi3} \approx -g_{m1}v_{\pi1}(Z_{L1} + R_{f1}) - (i_{b1}Z_{\pi1} + i_1R_{f2}) \left(1 + \frac{g_{m4}Z_{L1}}{1 + g_{m4}R_{e1}}\right) \quad (5)$$

where we have substituted $v_{\pi4}$.

Applying KCL law on both sides the feedback resistor R_{f2} , we can get the relationship between i_1 and i_{b1} . From this relationship, the input impedance of the amplifier can be written as

$$Z_{in} \approx \frac{R_{f2}}{1 + \frac{R_{f2}}{Z_{\pi1}} + g_{m1}(R_{e1} + r_{e4}) \left(1 + \frac{R_{f1}}{Z_{L1}}\right)} \quad (6)$$

where Z_{L1} represents the parallel combination of R_{L1} and load inductor L1. Compared to the total impedance of R_{f1} , the variation of Z_{L1} with frequency is very small. g_{m1} represents the transconductance of the input transistor Q1 while r_{e4} is the equivalent small-signal emitter resistor of transistor Q4. As (6) indicates, feedback resistors R_{e1} , R_{f1} and R_{f2} all play important roles in the input impedance. So input matching can be achieved by carefully choosing the value of these feedback resistors.

Compared to a traditional shunt feedback architecture in which the input matching is only determined by the shunt feedback resistor and the gain of the amplifier, the proposed

wideband LNA design provides more control parameters to adjust the input impedance, which means more freedom of achieving input matching. It helps break the trade-off between input matching and noise minimization. In designing the LNA, component values are first estimated based on analytical expressions [31], and the transistors are biased at the point where minimum noise figure is achieved. Then the input matching is tuned to an acceptable range by adjusting R_{f2} . The value of R_{f2} cannot be too small in order to avoid degrading the noise figure. Once transistors bias points and R_{f2} are determined, other component parameters such as R_{e1} and R_{f1} are fine-tuned to further improve the input matching.

In order to cover the entire X-band and Ku-band frequency range, the overall gain should be flat over the entire operating frequency range. However, the collector current from the transistor rolls off inversely with frequency. Inductor L1 in Fig. 4 helps equalize the voltage gain over the wide bandwidth, and the bandwidth at high frequency can be widened. In addition, the load inductor provides more headroom to achieve higher linearity.

The second stage of the LNA is a combination of a common-collector amplifier and a cascode amplifier, which operates similarly to the common-collector-common-emitter (CC-CE) configuration. The only difference comparing to CC-CE is that the collector of Q3 is connected to the output of the second stage instead of the power supply, which will reduce the effective output resistance of the second stage because of the feedback through Q3. With this implementation, the effective current gain of the basic transistor is increased. Referring to (2), the collector shot noise is directly related to the current gain and the collector shot noise of the second stage can be dramatically reduced with boosted current gain. The overall noise figure of the wideband LNA is further improved. Degeneration resistor R_{e1} was added to the second stage to improve the linearity performance, in addition to input matching.

The differential cascode architecture [32] in the output stage transforms the single-ended signal to a differential output. Compared to an external balun, the internal single-ended to differential transformation makes the receiver more compact

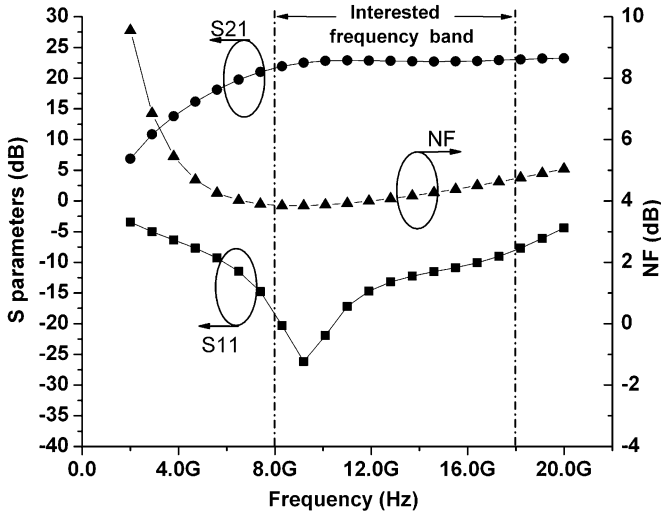


Fig. 6. Simulated S11, S21 and NF of the stand-alone LNA.

with lower noise figure. The on-chip single-ended to differential transformation usually contributes more noise than single-ended architectures, especially at the front-end. In our design, the single-ended to differential transformation is performed at the output stage with high gain budgeted for the first and second stages. This architecture contributes much less noise to the overall LNA, compared to the architecture where the transformation occurs at the input of the amplifier [10].

In this stage, resistor R_{e2} was used for common-mode rejection, since ac current is forced to flow through Q6 and also Q7, thereby creating an approximate 180° phase shift in differential paths. Although a tail current source realized by nMOS transistor can save some headroom requirement, the capacitance of the tail current transistor will cause common-mode degradation. This capacitive degeneration, through impedance transformation performed by the transistors Q6 and Q7, can easily trigger common-mode oscillation at high operating frequency. Also, the equivalent output impedance of tail current source is actually comparable to the degeneration resistor at X- and Ku-band frequency range. Thus, degeneration resistor R_{e2} was chosen in our design, instead of a current source. As the two branches are under the same bias conditions, roughly identical output amplitudes will be achieved.

In designing the proposed LNA, the emitter length of input transistor Q1 is chosen as $16 \mu\text{m}$ to minimize r_b . The emitter length of cascode transistor Q2 is $5 \mu\text{m}$. The sizes of cascode amplifiers in other stages are similar to the size of first stage. Feedback resistor $R_{f2} = 300 \Omega$ is chosen from the SPECTRE simulation. Fig. 6 shows the simulated S11, S21 and NF of the stand-alone LNA after parasitic extraction. As shown, the simulated S11 is below -8 dB over the entire X- and Ku-band. The simulated S21 is 22 dB from 8 GHz to 18 GHz with gain variation less than 1 dB. The simulated NF increases from 3.8 dB at 8 GHz to 4.7 dB at 18 GHz as shown in Fig. 6. The LNA stage is the dominate source of noise. The simulated gain of the LNA is about 20 dB which is high enough to suppress the noise contributed by the following stages, namely, the noise contributed by the mixer and the VGA is ignorable. The input 1-dB com-

pression point (P1dB) of the LNA is simulated to approximately -25 dBm over the frequency range of interest.

B. Mixers With Gain-Reuse

The dual-conversion gain-reuse mixers are based upon a folded mixer architecture, and are composed of the Gm stage, two switching quads and some internal and external filters, as shown in Fig. 7. The folded approach is chosen for operation at low supply voltage to reduce the power consumption of the whole receiver. Moreover, the folded topology offers the advantage of permitting independent settings of the Gm stage and the switching quads to optimize the performance of each. In addition, a current steering gain tuning approach is applied to the transconductance stage to adjust the input signal level. The gain control voltage V_{ctrl} that is applied to the base of the upper multiplier in the Gm/VGA cell, is used to adjust the gain. With the control of V_{ctrl} , the conversion gain from the input of the transconductance stage to the output of the first switching quad is related to the control voltage as follows, assuming ideal square wave switching is applied to the switching transistors:

$$A_{v,IF1} \cong \frac{2}{\pi} \cdot \frac{1}{1 + \exp\left(\frac{V_{ctrl}}{V_T}\right)} \cdot \frac{R_{L1}}{r_e + R_E} \quad (7)$$

where V_T is the thermal voltage of the bipolar transistor, and r_e represents the equivalent emitter resistance of Q1 and Q2. Degeneration resistor R_E is used to increase the linearity since the mixer requires relatively high linear performance. As mentioned above, the first IF signal at the output of the first switching quad is re-applied to the input through the SAW filter. Hence, both the RF signal and the first IF signal are separately adjusted in the unique Gm stage before they are coupled into switch quads for the frequency-translation. Consequently, the tunability of the proposed super-heterodyne mixers' gain can be improved as indicated by (8) neglecting the loss in the feedback loop, namely,

$$A_{v,total} \cong \frac{4}{\pi^2} \cdot \frac{1}{\left[1 + \exp\left(\frac{V_{ctrl}}{V_T}\right)\right]^2} \cdot \frac{R_{L1}R_{L2}}{(r_e + R_E)^2} \quad (8)$$

The tunability of the gain is enhanced due to the tuning factor $[1 + \exp(V_{ctrl}/V_T)]$ when compared to traditional multi-stage mixers without increasing the current consumption. Furthermore, since both RF and IF signals are simultaneously adjusted in the unique Gm stage, the power consumption of the two VGAs is further reduced with the same gain setting. Based on system requirements, a 20 dB tuning range is finally determined as the continuous analog tuning range. Although the continuous gain tuning range can be further increased until the IF2 output reaches the noise floor, the noise figure of the receiver will dramatically decrease. Meanwhile, spurs will increase due to reduced linearity of the Gm/VGA stage because the linearity of cascode transistors will be affected if too much current is steered away.

For noise considerations, the amplifier transistor in the Gm stage is carefully chosen to operate at the current density required for minimum noise figure. The minimum noise performance of the mixer also relies upon fast switching of the transistors in the switching quads, since fast switching will minimize the time in which the switching transistors stay in the ac-

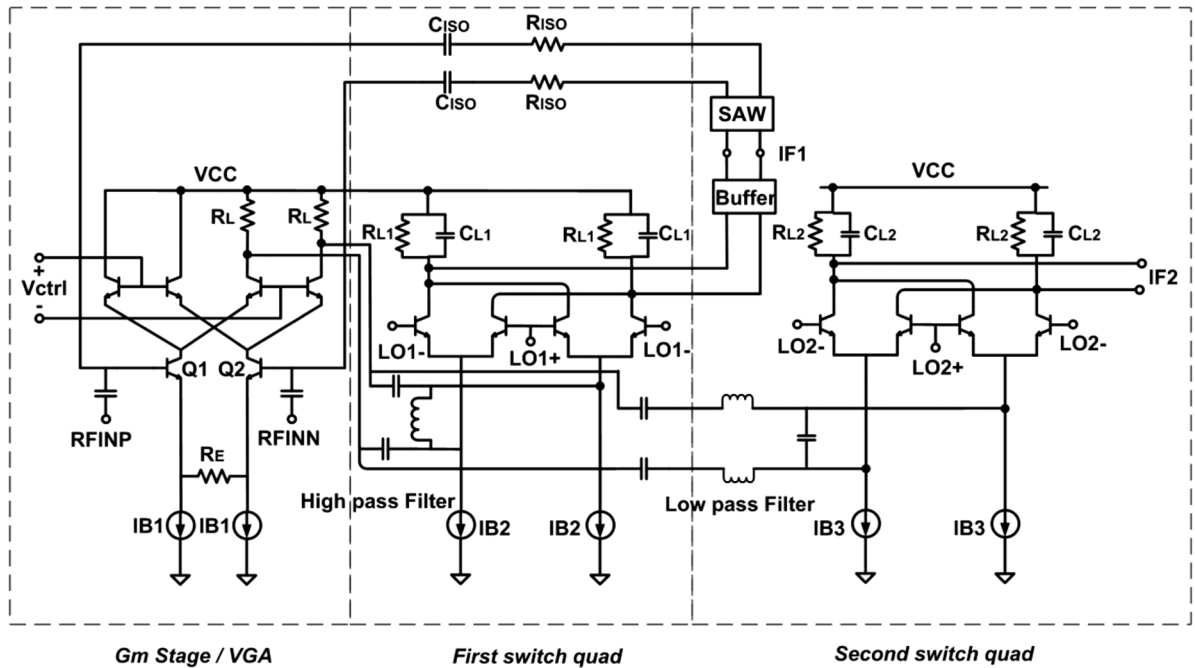


Fig. 7. Simplified schematic of the mixers with gain-reuse topology.

tive region. Therefore, the switching transistors are designed to operate at a current density near that corresponding to the peak f_T .

In the circuit implementation of the proposed current reuse topology shown in Fig. 7, the outputs of the Gm stage are ac-coupled to the inputs of the switching quads of the mixers through a filter network. Both high-pass and a low-pass networks are needed in front of the switching quads to separate the RF and IF signals and avoid generating unwanted signals through the mixers. Load resistors for the tunable transconductance stage provide high impedance such that most of the small signal current flows into the switch quad. Isolation resistors R_{ISO} are used to prevent the RF signals from being loaded by small impedances, and isolation capacitors C_{ISO} are used to isolate the DC bias.

The differential LO signals are generated by external signal generators. The signals, which are adjusted by current mode logic (CML) inverter-type LO buffers with low-power and good slew-rate performance, drive the switching quad in Fig. 7. Each LO buffer, as shown in Fig. 8, consists of a CML inverter and an emitter follower. Through use of an external balun, the single-ended LO signal is transferred to differential mode and the LO voltage swing applied to the switching transistor is about 0.6 Vp-p to achieve the desired noise figure and gain.

With the option of routing the IF signal off-chip, the first IF signal is fed back to the inputs of the Gm stage through an external SAW filter that removes unwanted signals, such as image signals, LO leakages and their harmonics, before being reapplied to the input stage. Furthermore, leakage of the first IF signal will generate an up-converted RF signal at the output of the first switching quad. This interference signal, along with the leakage of the RF signal, can lead to instability if they were fed back to the input of the Gm stage [8]. The bandpass SAW filter in the feedback loop will help remove these interference sig-

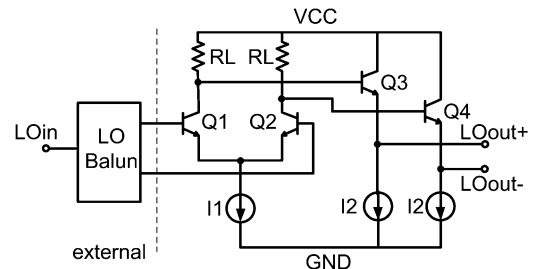


Fig. 8. Simplified schematic of the LO buffer.

nals and keep the system stable. Since the second mixer requires higher linearity than the first, load resistor $RL2$ and the bias current of the second mixer are chosen properly to give sufficient headroom for linearity.

In the circuit implementation of the mixer, the gm stage is optimized to operate where minimum noise figure is achieved. Thus, an emitter length of $15 \mu\text{m}$ is chosen for input transistors Q1 and Q2. The emitter lengths of the switching quad transistors are sized at $4 \mu\text{m}$ so that they operate close to their peak f_T .

C. Baseband VGA Design

The baseband VGA, used in this design, has 8 gain settings. It has three cascade amplifiers, each consisting of two differential pairs with their collectors tied together. The core cells of each amplifier are similar, as shown in Fig. 9. The only differences are the values of the load and degeneration resistors in each stage. The emitter lengths of the driving transistors are chosen as $4 \mu\text{m}$. All tail current sources are controlled by 6-bit digital control signals that are translated from a 3-bit external control signal through a decoder. The control signals determine which of the differential pairs in each stage will be active; current flows through one differential pair, never both. The differential gain

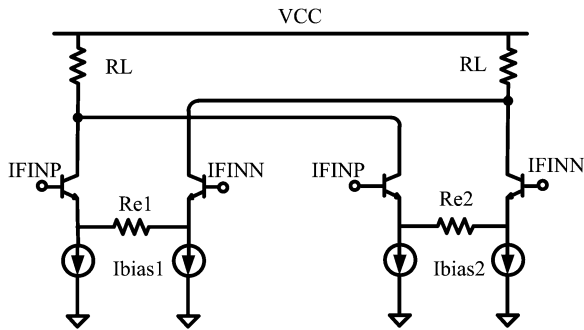


Fig. 9. Simplified core cell of each stage of baseband VGA.

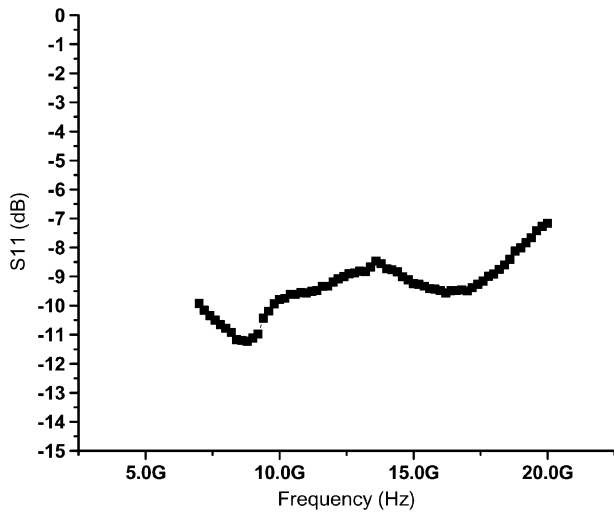


Fig. 10. Measured S11 of wideband receiver versus frequency.

of each stage is approximately equal to the ratio of the load resistance to the degeneration resistance. In order to drive the output pad, two output buffers are included in the final stage. The VGA can be discretely tuned from -4 dB to $+32$ dB.

IV. MEASURED RESULTS

The wideband receiver MMIC is implemented in a $0.13 \mu\text{m}$ SiGe BiCMOS process with f_T of about 200 GHz [9], occupies a total silicon area of $1.46 \times 1.24 \text{ mm}^2$, and is packaged in a 48-pin QFN package. To obtain accurate RF measurements, a wafer probe was used for RF inputs while all other pads were wire-bonded to the package. Fig. 10 shows the RF input return loss of the receiver. As shown, the input is well-matched to achieve smaller than -8.5 dB return loss over the entire X- (8–12 GHz) and Ku- (12–18 GHz) bands. In order to evaluate the performance of the receiver from 8 GHz to 12 GHz, the LO1 frequency was varied to follow the frequency change of the RF input to achieve a fixed IF2 signal at 150 MHz. The noise performance of the wideband receiver at maximum gain is shown in Fig. 11. The double-sideband (DSB) noise figure was measured between 6.7 and 7.8 dB from 8–18 GHz with the minimum NF achieved at 11 GHz. In order to examine the continuous tuning range of the receiver, the base-band VGA is set at

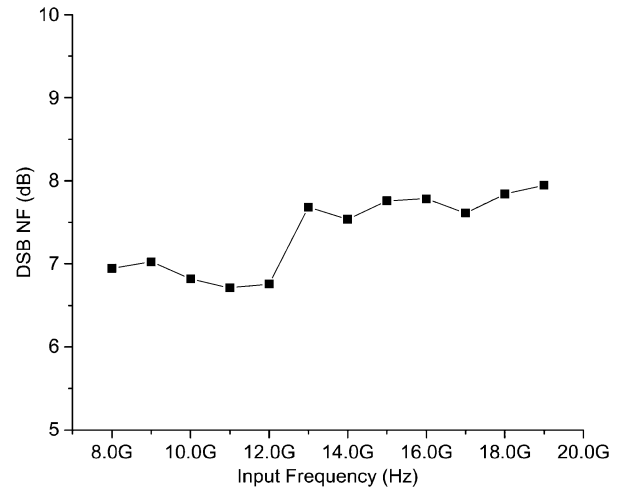


Fig. 11. Measured NF of the wideband receiver.

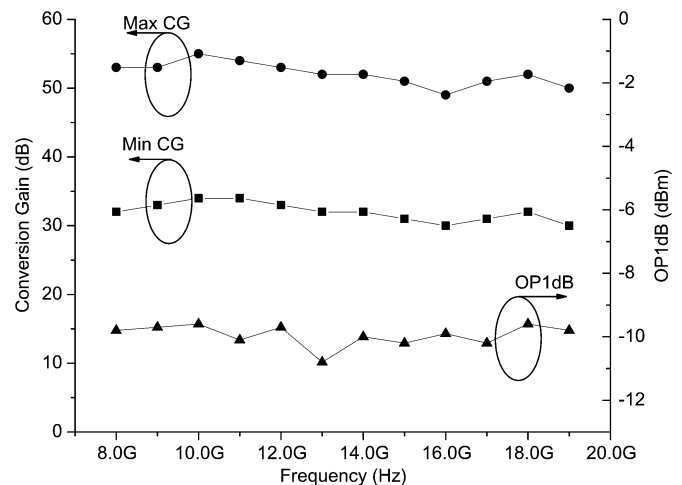


Fig. 12. Measured conversion gain and the linearity performance of the wideband receiver when the baseband VGA is set at fixed gain.

high gain mode with a fixed gain of 32 dB. The average maximum conversion gain of the wideband receiver is measured at 53 dB, as shown in Fig. 12, and the tuning range resulting from tuning the Gm stage is also shown in this figure. The gain range between the minimum conversion gain (CG) and its maximum can be easily achieved by simply tuning the mixers of the Gm stage, and measured results show that a 20 dB continuous tuning-range can be achieved. In the case of the gain-reuse design, the output in-band 1-dB gain compression point, measured at maximum gain, is nearly identical at different input frequencies. The measured average output compression point (OP1dB) is about -10 dBm, as shown in Fig. 12. As measured, the LO2 to IF isolation is 41 dB and the LO1 to IF isolation is better than 58 dB over the operating frequency band. The measured performance and a comparison with previous work are summarized in Table I, and the die photo of the receiver MMIC is given in Fig. 13. Compared to previous work [3], this design consumes much less power and occupies a smaller area. It also achieves much larger gain and higher dynamic range.

TABLE I
PERFORMANCE COMPARISON WITH PUBLISHED WIDEBAND RECEIVER

	This Work	REF [3]
Technology	0.13 μm SiGe BiCMOS	0.25 μm GaAs pHEMT
Supply Voltage	2.2V	5V
Supported Band	X band (8 – 12 GHz) Ku band (12 – 18 GHz)	S band and C band (2–8 GHz) X band (8 – 12 GHz) Ku band (12 – 18 GHz)
Voltage Gain	53dB (21dB from front end)	7.8dB
Tuning Range	56dB (20dB from front end)	0dB
Noise Figure	6.7 – 7.8dB @ Max gain	7dB
Input Return Loss	<-8.5dB @ 8 – 18GHz	<-10dB @ 2 – 18GHz
OPI1dB @Max gain	-10dBm	--
Power Consumption	180mW (Maximum)	1.3W
Die Area	1.46x 1.24mm ²	5.7 x 4.2mm ²

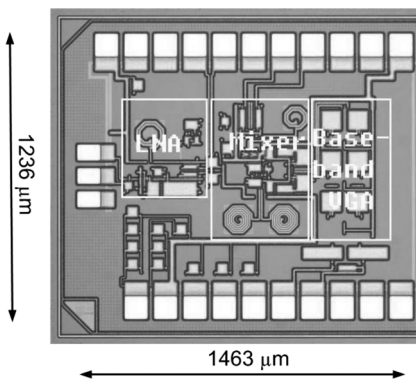


Fig. 13. Die micrograph of the SiGe wideband receiver.

V. CONCLUSION

A compact and power saving wideband receiver, which covers the entire X- and Ku- bands, without an external balun and matching network, is designed and fabricated in a commercial SiGe BiCMOS technology. Multi-feedback technology in conjunction with inductive compensation is applied to the input LNA design to achieve wideband operation. The design also utilizes a recursive gain reuse topology to save power with increased dynamic range. The receiver provides a flexible architecture with the option to use an external SAW for image rejection and antijamming. This work represents the demonstration of a fully integrated single-chip wideband receiver MMIC that is capable of operating over the entire X- and Ku-bands. The MMIC represents a key component for next generation wideband radar and other wireless communication applications.

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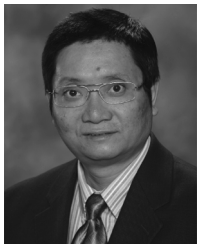
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