24-Bit 5.0 GHz Direct Digital Synthesizer RFIC With Direct Digital Modulations in 0.13 μm SiGe BiCMOS Technology

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Abstract—This paper presents a 24-bit 5.0 GHz ultrahigh-speed direct digital synthesizer (DDS) with direct digital modulation capabilities used in a pulse compression radar. This design represents the first DDS RFIC in over-GHz output frequency range with direct digital modulation capabilities. It adopts a ROM-less architecture and has the capabilities for direct digital frequency and phase modulation with 24 bit and 12 bit resolution, respectively. The DDS includes a 24-bit ripple carry adder (RCA) accumulator for phase accumulation, a 12-bit RCA for phase modulation and a 10-bit segmented sine-weighted digital-to-analog converter (DAC) for phase-to-amplitude conversion (PAC) as well as digital-to-analog conversion. The DDS core occupies 3.0 × 2.5 mm² and consumes 4.7 W of power with a single 3.3 V power supply. This 24-bit DDS has more than 20,000 transistors and achieves a maximum clock frequency of 5.0 GHz. The measured worst case SFDR is 45 dBc under a 5.0 GHz clock frequency and within a 50 MHz bandwidth. At 1.24628914 GHz output frequency, the 50 MHz narrowband SFDR is measured as 82 dBc. The best Nyquist band SFDR is 38 dBc with a 469.360351 MHz output using a 5.0 GHz clock frequency. This DDS was developed in a 0.13 μm SiGe BiCMOS technology with

\[ \frac{f_T}{f_{MAX}} = 200/250 \text{GHz} \]

and tested in a CLCC-68 package.

Index Terms—Accumulator, carry look ahead (CLA), digital-to-analog converter (DAC), direct digital synthesizer (DDS), frequency modulation (FM), linear frequency modulation (LFM), phase modulation (PM), pulse compression, radar, ripple carry adder (RCA), ROM-less DDS, sine-weighted DAC, stretch processing.

I. INTRODUCTION

The ultrahigh-speed direct digital synthesizer (DDS) will play a key role in next generation radar and communication systems. Recent developments in radar systems require frequency synthesis with low power consumption, high output frequency, fine frequency resolution, fast channel switching and versatile modulation capabilities. Linear frequency modulation (LFM) or chirp modulation is widely used in radars to achieve high range resolution, while pulsed phase modulation (PM) can provide anti-jamming capability. With fine frequency resolution, fast channel switching and versatile modulation capabilities, the DDS provides frequency synthesis and direct modulation capabilities that cannot be easily implemented by other synthesizer tools such as analog-based phase-locked loop (PLL) synthesizers. It is difficult for conventional PLL-based frequency synthesizers to meet these requirements due to internal loop delay, low resolution, modulation problems and limited tuning range of the voltage-controlled oscillator (VCO).

The increasing availability of ultrahigh-speed DACs allows a DDS to generate over-GHz frequency waveforms. However, no DDS with over-GHz output that have been developed thus far provide the desired modulation capabilities [1]–[7]. To achieve an over-GHz output frequency, all existing DDS RFICs use pipeline accumulators that work only with a constant input frequency control word (FCW), and thus no frequency modulation (FM) can be performed [1]–[7]. To implement direct FM or PM, carry-look-ahead (CLA) or ripple carry adder (RCA) must be used with the attendant penalty of reduced speed. Ref. [8] reported a 9-bit DDS with RCA accumulator. It has the capability of FM, but only at low frequency because the FCW cannot change too fast with the bipolar plus NMOS adder architecture, and no PM can be performed. This paper presents a 24-bit 5.0 GHz DDS with over-GHz output frequency and direct digital modulation capabilities. To our best knowledge, this work represents the first DDS RFIC with over-GHz range output as well as direct digital FM and PM capabilities.

This paper is organized as follows: Section II introduces the direct digital modulation DDS used in modern radar systems. Pulse compression and stretch processing implemented using DDS are briefly discussed. In Section III, the ultrahigh-speed adders using both CLA and RCA architectures are discussed and compared. Circuit implementation of the RCA is discussed as well. The design of a 10-bit sine-weighted DAC is described in Section IV. In Section V, measurement results are presented and compared. Finally, conclusions are given in Section VI.

II. DIRECT DIGITAL MODULATION DDS USED IN MODERN RADAR SYSTEMS

A. DDS Modulated Signals Used in Modern Radar Systems

Range resolution is the ability of a radar system to distinguish between two or more targets on the same bearing but at different distances. Weapon-control radar, which requires great precision, should be able to distinguish between targets that are only yards apart. Search radar is usually less precise and only distinguishes between targets that are hundreds of yards or even

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The degree of range resolution depends on the width of the transmitted pulse, the types and sizes of the targets, and the efficiency of the receiver and indicator. The range resolution of simple single pulse radar is $cT/2$, where $c$ is the pulse transmitting velocity and $T$ is the pulse width transmitted by the pulse radar. In pulse compression radar shown in Fig. 1, with the help of a versatile modulated signal generated by a DDS, such as LFM, nonlinear FM or phase-coded waveforms, the range resolution can be improved to $c/(2B)$ without losing received pulse strength [9], where $c$ is the signal transmitting velocity and $B$ is the bandwidth of the transmitted signal. In comparison to the simple single pulse radar, the range resolution is increased by $T/B$ times while the transmitted signal maintains the same instantaneous power. The quantity $T/B$ is the pulse compression ratio, and it is usually much greater than 1.

The traditional radar receiver uses a wide bandwidth convolution processor with a matched filter to process the received pulse compression signal. It requires high bandwidth for the analog-to-digital converter (ADC) as well as the back-end processing. In modern radar systems, stretch processing is used to reduce the bandwidth requirement of the ADC and back-end processing. Stretch processing is a technique for processing LFM, or other modulated wideband waveforms, using a signal processor with a bandwidth that is much smaller than the transmitted signal bandwidth, without losses in the signal-to-noise ratio (SNR) or range resolution [10], [11]. As shown in Fig. 1, stretch processing can be implemented in modern radar systems with the help of a simple mixer and the modulated reference signal generated from the same DDS as in the transmit path.

B. Ultrahigh-Speed DDS With Direct Digital Frequency and Phase Modulations

All these modulated signals used in modern radar can be generated from a DDS with direct digital FM and PM capabilities. Fig. 2 shows a general architecture of a ROM-less DDS with direct digital modulation capabilities designed for radar systems. The architecture has four parts, a D-bit sine-weighted DAC, a P-bit adder used as a phase modulator, an N-bit phase accumulator and another N-bit accumulator used as an N-bit chirp ramp signal generator. Chirp control words (CCW), frequency control words (FCW) and phase control words (PCW) provide the control signal for the chirp accumulator, phase accumulator and phase modulator, respectively. Through the direct use of digital control words to change the values of registers in the data path of the DDS, the frequency, phase, and amplitude of the output waveforms can be precisely controlled. Since all the modulations are done in the digital domain, many disadvantages associated with normal analog modulations can be avoided. In this ROM-less DDS architecture, the sine-weighted DAC assumes the responsibility for phase-to-amplitude conversion (PAC) as well as digital-to-analog conversion. Without a ROM, which is usually the speed bottleneck, this DDS architecture can be developed to produce over-GHz frequency waveforms. To perform the direct digital modulations, the accumulators and modulator (full adder) must be updated in every clock cycle. As a result of this requirement, a pipeline accumulator is used with an attendant sacrifice in speed.

The DDS can be used to implement modulations and generate waveforms such as PM, LFM, step FM (frequency hopping), binary frequency shift-keying (BFSK), binary phase shift-keying (BPSK) and other hybrid modulations. Fig. 3 shows some direct digital modulation waveforms generated from a 16-bit phase resolution DDS. This DDS has both 16-bit FM resolution and another N-bit accumulator used as an N-bit chirp ramp signal generator. Chirp control words (CCW), frequency control words (FCW) and phase control words (PCW) provide the control signal for the chirp accumulator, phase accumulator and phase modulator, respectively. Through the direct use of digital control words to change the values of registers in the data path of the DDS, the frequency, phase, and amplitude of the output waveforms can be precisely controlled. Since all the modulations are done in the digital domain, many disadvantages associated with normal analog modulations can be avoided. In this ROM-less DDS architecture, the sine-weighted DAC assumes the responsibility for phase-to-amplitude conversion (PAC) as well as digital-to-analog conversion. Without a ROM, which is usually the speed bottleneck, this DDS architecture can be developed to produce over-GHz frequency waveforms. To perform the direct digital modulations, the accumulators and modulator (full adder) must be updated in every clock cycle. As a result of this requirement, a pipeline accumulator is used with an attendant sacrifice in speed.

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C. System Architecture of the 24-bit 5.0 GHz Ultrahigh Speed ROM-less DDS

A 24-bit 5.0 GHz ultrahigh-speed DDS is implemented with direct digital FM and PM capabilities using RCA adders. The block diagram of the 24-bit 5.0 GHz ROM-less DDS with RCA accumulator and modulator is shown in Fig. 4 [12]. The major parts of the ROM-less DDS are a 24-bit RCA phase accumulator, a 12-bit RCA modulator, and a 10-bit sine-weighted DAC. The 24-bit RCA phase accumulator output is truncated to 12 bits and modulated with a 12-bit PCW. After PM, the output is truncated again, and the highest 11 bits are fed into the sine-weighted DAC. The sine-weighted DAC maps the 11-bit linear phase word to the digital amplitude and generates the analog waveform. The ultrahigh-speed RCA accumulator/adder and sine-weighted DAC will be described in the following two sections, respectively.

III. ULTRAHIGH SPEED ADDER DESIGN

A. Wire Delay in the 0.13 μm SiGe BiCMOS Technology

With the introduction of deep submicron semiconductor technology, the parasitic effects introduced by the wire delay begin to dominate the performance of high-speed digital integrated circuits. The typical buffer delay in the 0.13 μm SiGe BiCMOS technology is less than 4 ps while the wire delay of a 2 μm wide and 100 μm long wire can be as high as 10 ps. From [13], the transmission line effects should be considered when the rise or fall time of the input signal is smaller than the time of flight of the transmission line. The following equation is used to determine when transmission line effects should be considered.

\[ t_{rf} \leq 2.5t_{flight} = 2.5 \frac{L}{v} \]  \hspace{1cm} (1)

In (1), \( t_{rf} \) is the rise and the fall time of the signal transmitted through the wire. \( t_{flight} \) is the flight time, which is the time it takes for the wave to propagate from one end of the wire to the other, and is 15 cm/ns in silicon oxide (SiO₂). So the minimum length that must be considered as a transmission line for a signal is

\[ L_{\text{min}} = 0.4t_{rf} \cdot v. \]  \hspace{1cm} (2)

For a 5.0 GHz signal the rise and fall time should not be longer than 67 ps. If the wire length is less than 4 mm, a lumped RC model can be used to evaluate the propagation delay through the wire. Fig. 5 shows the equivalent circuit of a wire with length \( L \). From the Elmore delay rule, the dominant time constant is

\[ \tau_D = R_i c L + 0.5 r c L^2 \]  \hspace{1cm} (3)

where \( R_i \) is the internal resistance of the driver, and \( r \) and \( c \) are the unit length parasitic resistance and capacitance of the wire. The delay introduced by the wire resistance becomes dominant when the second term is bigger than first, i.e. when \( L \geq 2R_i/r \). In the 0.13 μm SiGe BiCMOS technology, the first term in (3) will dominate the propagation delay, as long as \( L < 2 \text{ mm} \), and as a result the propagation delay of the wire is approximately proportional to the length.

To evaluate wire delay effects in high-speed digital logic design, several simulations have been performed in a 0.13 μm SiGe process for a current-mode-logic (CML) cell implemented using a differential pair without an emitter follower as the output buffer and its connection wires. Fig. 6 shows the test bench used to simulate the wire delay effects. Fig. 6(a) is the schematic view. It is used to find the intrinsic propagation delay of the CML buffer that is 2 μm wide and 100 μm long. Differential wires with the third metal layer are inserted between the two buffers in Fig. 6(b). The space between the two differential wires is typically maintained at 2 μm in the layout. Fig. 6(c) uses the same test bench as that employed in Fig. 6(b), with the exception of an additional piece of metal under the differential wires. Fig. 6(d) uses the same test bench as that in Fig. 6(b), except in this case two pieces of metal are used to sandwich the differential wires. Clearly, cases Fig. 6(c) and (d) result in a larger parasitic capacitance than Fig. 6(b). However, it is not always possible to place the wire without any overlap with the metals that are under and above the wires, especially for modern processes with more than 5 layer metal connections. The simulated results are plotted in Fig. 7. In Fig. 7, plot (A) represents the propagation delay of Fig. 6(a), and illustrates the propagation delay of only the input and output buffers. It does not include the wire delay so it is constant along the wire length. Plots (B), (C) and (D) show the propagation delay of test bench (B), (C) and (D) but does not include the buffer delays in the test benches.
Fig. 4. Block diagram of the 24-bit 5.0 GHz DDS RFIC.

Fig. 5. Lumped RC model for a wire with length of L.

Fig. 6. Test bench to simulate the wire propagation delay.

Fig. 7. Simulated wire propagation delay versus length.

These three plots reflect the third metal wire propagation delay in a 0.13 μm SiGe process. It is proportional to the wire length as long as the length is less than 2 mm. Comparing (B), (C) and (D), the wire delay with shielded metal is two (for (C)) or three (for (D)) times larger than an unshielded metal wire. This conclusion, as well as the linear relationship between the wire delay and the wire length, indicates that the wire delay is dominated by the time constant of the product of parasitic capacitance and the input buffer output impedance, as described by the first term of (3). Note that test benches (C) and (D) are more practical cases than (B), because in a real layout environment all the wires overlap each other and produce several times more parasitic capacitance than the coupling capacitance with the substrate. From the wire delay plot of Fig. 7, the wire delay coefficient (delay for 1 μm wire) for case (C) is about 0.10 ps/μm. This number will be used to estimate the adder delay in the following sections.

B. Propagation Delay Comparison Between the CLA and RCA Accumulator/Adder

A pipeline accumulator can only handle a fixed input FCW. Direct modulations such as LFM require a varying input FCW. Thus, either RCA or CLA adders must be used to implement direct modulations. Ref. [14] has calculated a 9-bit CLA adder delay for the critical path with 3-input CML implementations. However, the calculation did not count the level shifters that are used to shift between different input voltage levels, as well as the wire delays. In general, level shifters usually run much faster than CML gates, and thus can be ignored when counting the gate delays. Furthermore, the XOR gate delay is treated the same as the AND gate delay since CML gate delays are essentially identical for different gates. For example, both the carry and sum logic in a full adder can be implemented by only one current tail CML gate. Given this information, the 9-bit CLA adder has a total of 8 CML gate delays. One CML gate delay is about 9 ps in the 0.13 μm SiGe BiCMOS technology. In the 9-bit full adder, the total logic delay is approximately 72 ps without the wire delay. From Fig. 8 and the actual layout, the wire delay in the critical path of the 9-bit CLA adder is calculated as follows: (A) A 200 μm wire is added to calculate the delay of level I generate and propagate $g_i$ and propagate $p_i$; (B) A 200 μm wire is added to calculate the delay of level II generate $G_i$ and propagate $P_j$; (C) A 300 μm
wire is added to calculate the delay of the level II carry; (D) A 200 μm wire is added to calculate the delay of level I carry; (E) A 200 μm wire delay is added to calculate the delay of the sum and carry-out. Therefore, the total wire length to calculate the delay of the critical path is 1100 μm. If the bit number of the adder is higher than 9 bits and less than 27 bits, level III CLA block is needed to calculate the carry-out. To generate the third level CLA logic and the carry-in signal for the second level CLA block, the total gate delay increases to 12 CML gate and the total wire length increases to 1800 μm. The worst case delay from a 10-bit CLA adder to 27-bit CLA adder remains the same since these adders have an identical critical path.

The calculation of propagation delay for the RCA is much easier than the CLA adder. Fig. 9 shows the architecture of an N-bit RCA. It represents the layout floor plan and the component placement as well as the schematic wire connection. The output and carry-out for each bit are calculated as

\[
\begin{align*}
\text{Carry out: } c_i &= A_i B_i + B_i c_{i-1} + c_{i-1} A_i \\
\text{Sum: } s_i &= A_i \oplus B_i \oplus c_{i-1}
\end{align*}
\]

where \(A_i\) and \(B_i\) are the input of the N-bit full adder, \(i = 0, 1, \cdots, (N-1)\). \(c_i\) is the carry-out of the \(i\)th-bit full adder. \(c_{-1} = C_{in} = 0\) is the initial carry-in of the N-bit full adder. \(C_{out} = c_{N-1}\) is the last bit carry-out of the N-bit full adder. Therefore, the worst case propagation delay of the N-bit full adder is the delay of N-1 carry logic gates and one sum logic gate. There is almost no wire delay since the carry logic can be placed as close as possible to minimize the amount of wire in the connection. The level shifter delay can be eliminated as well because the input voltage level can be intentionally removed from the critical path.

Fig. 8. Diagram of 9-bit CLA adder.

Fig. 9. Diagram of N-bit RCA.

Fig. 10. Estimated adder propagation delays with different number of bit.

Fig. 10 shows the comparison of the estimated propagation delay of the CLA adder and RCA. Not counting the wire delay, the speed of the CLA adder is close to that of the RCA for small numbers of bits. At high numbers of bits, the CLA adder runs much faster than the RCA. With the added wire delay, the RCA delay does not change too much because the RCA is very compact and can be laid out very closely, thus having almost no wire delays. However the layout of the CLA is very complex and introduces significant wire delay. So the CLA adder runs much slower than the RCA especially for 10-bit to 25-bit adders. In addition to the internal wire delays of the CLA adder, the CLA adder layout area is several times larger than the RCA adder, which results in more wire delays for global wiring.

In conclusion, at the low or medium speed with an older and slower fabrication technology, the CLA speeds up the adder operation by using additional logic for carry calculations. However, for high-speed implementation with fast technology (e.g., \(< 0.13 \mu m\)), adder delay is mainly dominated by the wire delays. When compared to a CLA adder, the RCA adder has a simple ripple architecture, which can be laid out in cascaded format one bit after another, leading to very compact layout with short wire interconnections between stages.
C. Circuit Implementation of the 24-bit 5.0 GHz RCA

In this DDS design, a 24-bit RCA is used to implement the 24-bit accumulator. The 24-bit RCA is composed of 24 1-bit full adders carefully designed in a compact manner. The output of the carry-out logic remains at the top CML level, and no level shifter is needed to convert the signal level for the critical path. Therefore the longest delay from input to output of the 24-bit RCA is 23 carry-out CML delays and 1 sum CML gate delay. The wire delay in the RCA can be minimized since the carry-in can be directly connected to the carry-out of the previous bit, leading to a compact layout in a cascaded format. Another 12-bit RCA was implemented for the 12-bit phase modulator. In addition, the 24-bit CLA adder runs slower than the RCA adder as shown in Fig. 10. When the 0.13 μm SiGe BiCMOS technology is used, long wires contribute much more delay than the logic gates. So a 24-bit CLA adder cannot run as fast as the RCA adder, not only because of the amount of cascade CLA logic with the attendant limited CML fan-in numbers but also because of the much longer wire delays needed by CLA logic. The wire delay in the RCA adder can be minimized since the carry-in can be directly connected to the carry-out of the previous bit, leading to a compact layout in a cascaded format.

IV. 10-BIT SEGMENTED SINE-WEIGHTED DAC

A. Architecture of the 10-bit Sine-Weighted DAC

The structure of the 10-bit sine-weighted DAC is shown in Fig. 11. The total phase word input for the sine-weighted DAC is 11 bits. The two most significant bits (MSB) are used to determine the quadrants of the sine wave. The MSB output of the phase word is used to provide the proper mirroring of the sine waveform about the π phase point. The 2nd MSB is used to invert the remaining 9 bits for the 2nd and 4th quadrants of the sine wave by a 1’s complementor, and the outputs of the complementor are applied to a 9-bit sine-weighted DAC core to form a quarter of the sine waveform. Because of this π phase point mirroring, the total amplitude resolution of the sine-weighted DAC is 10 bits.

To reduce the complexity of the sine-weighted DAC, segmentation has been employed [7], [15]. The 9-bit sine-weighted DAC core is divided into a 6-bit thermometer-decoded coarse sine-weighted DAC and eight 3-bit thermometer-decoded fine sine-weighted DACs. The first 6 bits of the complementor’s output control the coarse DAC and the highest 3 bits also address the selection of the fine DACs. The lowest 3 bits of the complementor’s output determines the output value of each fine DAC. The bit division between the 6-bit coarse DAC and the 3-bit fine DACs is based on the trade-off of static and dynamic accuracy, chip area and power consumption. As shown in Fig. 11, the bottom current source array implements the coarse DAC. The coarse DAC current source array provides 512 unit current sources. The top current source array implements the fine DACs. Each column of the fine DAC current source array forms the current sources of one fine DAC. Every fine DAC has about 8 unit current sources used to interpolate the coarse DAC. The unit current of both the coarse and fine DACs is set at 26 μA. The largest current in the current source matrix is 338 μA, which is composed of 13 unit current sources. In the layout, with consideration for current source matching, each current source is split into four identical current sources which carry a quarter of the whole current. To further improve their matching, all current source transistors, including those used in both the coarse and fine DACs, are randomly distributed in the whole current source matrix.

The current switch contains two differential pairs and improves the bandwidth of the switching operation with minimum
logic transistors and cascode current sources that provide better isolation and current mirror accuracy. The current outputs are converted to differential voltages by a pair of off-chip 15 \( \Omega \) pull-up resistors. Fig. 12 shows that the currents from the cascode current sources are fed to outputs \( \text{OUT}_p \) and \( \text{OUT}_m \) by pairs of switches (Msw). The MSB controls the selection between different half periods.

B. Bandwidth Limitation of the DAC Switch Output Impedance

The dynamic performance of the current-steering DAC is closely related to the current switch output impedance as well as the frequency response of the output impedance. With a full thermometer decoded DAC, the SFDR can be written as a function of the output impedance \( Z_{\text{out}} \) and the DAC’s number of bits of resolution \( N \) [16].

\[
\text{SFDR} = 20 \log \left( \frac{Z_{\text{out}}}{R_L} \right) - 6.02(N - 2) \tag{5}
\]

where \( R_L \) is the load resistance of the current switch. The core switch cell of the sine-weighted DAC is shown in Fig. 13(a). \( C_0 \) and \( C_1 \) denote the parasitic capacitance at the drain of the current source transistor and the collector of the cascode transistor, including the device parasitic capacitance and the wire capacitance. The small signal equivalent circuit is drawn in Fig. 13(b).

If \( r_p \) is neglected, the total output impedance looking through the switch output is given by

\[
Z_{\text{out}} = g_{\text{mSW}}r_{\text{osw}} \cdot \left( \frac{1}{sC_1} \right) \cdot \left( \frac{1}{sC_0} \right) \cdot \left( \frac{1}{r_{\text{os}}} \right) \tag{6}
\]

In (6), \( g_{\text{mSW}} \) and \( r_{\text{osw}} \) denote the transconductance of the switch and the cascode transistor, respectively. \( r_{\text{osw}} \) and \( r_{\text{os}} \) denote the output resistance of the switch and the cascode and the current source transistor, respectively. At low frequency, the output impedance can be simplified as

\[
Z_{\text{out}} = g_{\text{mSW}}r_{\text{osw}} \cdot \left( \frac{1}{sC_1} \right) \cdot r_{\text{os}} \tag{7}
\]

\( g_{\text{mCAS}}r_{\text{osCAS}} \) is the maximum gain of the cascode transistor. The bipolar transistor is chosen since it has higher maximum gain than the MOS counterpart, while an MOS transistor is chosen for the current source because it has higher output resistance than the bipolar transistor as well as a lower overdrive voltage.

From (6), the dominant pole of the output impedance is

\[
\omega_p = \frac{1}{r_{\text{os}}(C_0 + r_{\text{os}}(g_{\text{mCAS}}C_1))} \tag{8}
\]

To increase the bandwidth of the output impedance, the parasitic capacitances \( C_0 \) and \( C_1 \) must keep as small as possible. Because the maximum gain of the cascode transistor \( g_{\text{mCAS}}r_{\text{osCAS}} \) is much larger than 1, parasitic capacitance \( C_1 \) affects the bandwidth of the output impedance much more significantly than \( C_0 \). So the
the output frequency is 1.251 kHz with a 1.246258914 GHz output frequency for the 24-bit 5.0 GHz DDS within a 50 MHz bandwidth, and demonstrates about 45 dBc narrowband worst case SFDR. In addition, the DDS has several sweet spots, in the interest of many applications [15].

Figs. 14 and 15 illustrate the measured DDS output spectra and waveforms for different outputs and clock frequencies. All measurements were done with single-ended output and using CLCC-68 packaged parts without calibrating the losses of the cables and PCB tracks.

Fig. 14 shows a 469.360351 MHz DDS output with a 5.0 GHz clock input with FCW = 0x180800 in hex format. Because of the MSB mirroring shown in Fig. 12, the single output peak to peak voltage is 400 mV. So the output power in theory can be calculated as

$$10 \log \left( \frac{400 \text{ mV}}{(2\sqrt{2})} \right)^2 \approx 1.25 \text{ dBm}. \quad (9)$$

Fig. 15 shows a 1.256258914 GHz output and the maximum 5.0 GHz clock (FCW = 0x3FCFE7), showing an 82 dBc narrowband SFDR.

Counting the loss due to the parasitic capacitances, PCB tracks and RF cables, the measured output power is approximately −2.12 dBm. The measured SFDR is approximately 38 dBc in Nyquist bandwidth. Since the FCW = 0x180800, the output frequency is given by

$$\frac{\text{FCW}}{2^N} \times f_{\text{clk}} = \frac{0x180800}{2^{24}} \times 5.0 \text{ GHz} = 469.360351 \text{ MHz}, \quad (10)$$

In the stretch processing radar, which is essentially a narrowband system, the narrowband SFDR of the DDS is often more important since wideband spurs can be removed relatively easily. It is only a specific narrowband near the output, which is usually less than 1% of the update frequency, that is of the interest of many applications [15]. Fig. 15 provides an example of a 1.246258914 GHz output frequency (FCW = 0x3FCFE7) with a 5.0 GHz clock frequency in a 50 MHz band. The measured narrowband SFDR is about 82 dBc.

Fig. 16 demonstrates the operation of the DDS with an LFM output. With a 300 MHz clock input, a 24-bit 300 MHz ramp from 0x0000001 to 0x00AD9c is fed into the FCW input. The output sweeps from 18 Hz to 397.367947 kHz. In this DDS, CMOS logic was used to provide the modulation data inputs. The speed is limited by the speed of the data source that was provided by an Agilent pattern generator through the PCB board. A maximum of 2.5 GHz LFM can be reached if the modulation ramp is generated inside the DDS chip.

Fig. 17 shows the measured DDS output with FCW = 7, phase modulated by a step of PCW = 0x800 resulting in an 180° phase shift. The output frequency is 1.251 kHz with a 3.0 GHz clock. Both the LFM and the PM waveforms can be used in radar transceivers as the source of transmitted chirp signal and the reference chirp signal for stretch processing, as described in Section II. Based on the discussion in Section II, chirp modulated waveform improves the radar range resolution, while the stretch processing using LFM reduces the bandwidth requirement for the ADC in the receiver path.

Fig. 18 provides a plot of the measured SFDR versus the output frequency for the 24-bit 5.0 GHz DDS within a 50 MHz bandwidth, and demonstrates about 45 dBc narrowband worst case SFDR. In addition, the DDS has several sweet spots, in

Fig. 14. Measured DDS output with a 469.360351 MHz output and the maximum 5.0 GHz clock (FCW = 0x180800), showing a 38 dBc Nyquist band SFDR.

Fig. 15. Measured DDS output with a 1.246258914 GHz output and the maximum 5.0 GHz clock (FCW = 0x3FCFE7), showing an 82 dBc narrowband SFDR.

Fig. 16. Measured DDS LFM output as FCW sweeps from 1 to 0x005AD9C and using a 300 MHz clock.
TABLE I
ULTRAHIGH-SPEED DDS RFIC PERFORMANCE COMPARISON

<table>
<thead>
<tr>
<th>Technology</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
<th>[6]</th>
<th>[7],[15]</th>
<th>[8]</th>
<th>[14]</th>
<th>[this work]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_T / f_{MAX}$ [GHz]</td>
<td>137/267</td>
<td>300/300</td>
<td>300/300</td>
<td>370/370</td>
<td>100/120</td>
<td>200/250</td>
<td>$f_T = 70$</td>
<td>200/250</td>
<td>200/250</td>
</tr>
<tr>
<td>Phase resolution [bit]</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>12</td>
<td>9</td>
<td>11</td>
<td>9</td>
<td>9</td>
<td>24</td>
</tr>
<tr>
<td>Amplitude resolution [bit]</td>
<td>7</td>
<td>7</td>
<td>5</td>
<td>7.5</td>
<td>8</td>
<td>10</td>
<td>8</td>
<td>7</td>
<td>10</td>
</tr>
<tr>
<td>Frequency modulation [bit]</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>9</td>
</tr>
<tr>
<td>Phase modulation [bit]</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>9</td>
</tr>
<tr>
<td>Maximum clock [GHz]</td>
<td>9.2</td>
<td>13</td>
<td>32</td>
<td>24</td>
<td>12.3</td>
<td>8.6</td>
<td>6.0</td>
<td>2.9</td>
<td>5.0</td>
</tr>
<tr>
<td>SFDR [dBc]</td>
<td>&lt;30</td>
<td>26.67</td>
<td>21.56</td>
<td>30.7</td>
<td>20</td>
<td>33</td>
<td>17</td>
<td>38(narrow)</td>
<td>45(narrow)</td>
</tr>
<tr>
<td>Power consumption [W]</td>
<td>15</td>
<td>5.42</td>
<td>9.45</td>
<td>19.8</td>
<td>1.9</td>
<td>4.8</td>
<td>0.308</td>
<td>2.0</td>
<td>4.7</td>
</tr>
<tr>
<td>Die area [mm²]</td>
<td>8×5</td>
<td>2.7×1.45</td>
<td>2.7×1.45</td>
<td>5.0×3.3</td>
<td>3×3</td>
<td>4×3.5</td>
<td>1</td>
<td>2.5×3.0</td>
<td>3.7×3.0</td>
</tr>
</tbody>
</table>

Fig. 17. Measured DDS output with $FCW = 7$ phase modulated by a phase step of $\Delta FCW = 0\times800$ causing an 180° phase shift. The output frequency is 1.251 kHz with a 3.0 GHz clock.

Fig. 18. Measured DDS narrowband SFDR versus output frequency within a 50 MHz bandwidth.

which its output spectrum purity and its dynamic performance are much better than what can be obtained in other frequency bands. Fig. 15 gives an example of an 82 dBc SFDR in 50 MHz bandwidth.

The die photo of the DDS is shown in Fig. 19. This DDS design is quite compact with an active area of 3.0 × 2.5 mm² and a total die area of 3.7 × 3.0 mm². Table I compares ultrahigh-speed DDS RFIC performances with over-GHz output frequency. Although the DDS reported here has relatively low frequency when compared with others, it is the first over-GHz output frequency implementation with direct digital FM and PM capabilities. Some commercial parts have the direct digital FM and PM capabilities, but all the parts only work up to 1.0 GHz with an output of less than 500 MHz [17].

VI. CONCLUSION

This paper presented a 24-bit 5.0 GHz DDS RFIC with direct digital modulation capabilities, developed in a 0.13 μm SiGe BiCMOS technology for pulse compression radar applications. A 24-bit RCA accumulator and a 12-bit RCA are implemented for the use of modulator designs with over-GHz frequency output. For high-speed DDS implementation, adder delay is mainly dominated by the wire delays. A comparison between the RCA and CLA adder has been performed in this paper. Compared to a CLA adder, the RCA has a simple ripple architecture, which can be layed out in a cascaded format one bit after another, resulting in a very compact layout with short wire interconnections between stages. Thus, the RCA actually ends up with higher operation frequency than the CLA adder.

This 24-bit DDS has more than 20,000 transistors and achieves a maximum clock frequency of 5.0 GHz. The measured worst case SFDR is 45 dBc under a 5.0 GHz clock.
frequency and within a 50 MHz bandwidth. The best Nyquist band SFDR is 38 dBc with a 469.360351 MHz output using a 5.0 GHz clock frequency. This DDS represents the first implemented RFICs with direct digital modulations at over-GHz output frequency.

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REFERENCES


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Dr. Dai served as Guest Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS in 2001, 2009, and 2010. He served on the technical program committee of the IEEE Symposium on VLSI Circuits from 2005 to 2008. He currently serves on the technical program committees of the IEEE Custom Integrated Circuits Conference (CICC) and the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM). He received the Senior Faculty Research Award for Excellence from the College of Engineering of Auburn University in 2009.

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He joined Bell Telephone Laboratories as a Member of the Technical Staff in 1967 and was made a Supervisor in 1968. He joined Auburn University in 1969, became head of the Electrical Engineering Department in 1973, and served in that capacity for 36 years. He is now the Earl C. Williams Eminent Scholar in the College of Engineering at Auburn University, where he is currently a Professor in electrical and computer engineering. His research interests include VLSI circuits for digital, analog, mixed-signal and RF applications, ultrahigh-frequency direct digital frequency synthesis (DDS) and digital to analog converters (DAC).
Richard C. Jaeger (S’68–M’69–SM’78–F’86–LF’09) received the B.S. and M.E. degrees in electrical engineering in 1966 and the Ph.D. degree in 1969, all from the University of Florida, Gainesville.

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