

A 5.2GHz Variable Gain Low Noise Amplifier RFIC with Adaptive Biasing for Improved Linearity

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Abstract — This paper presents a 5.2-GHz adaptively-biased variable gain- low noise amplifier (VG-LNA) using SiGe BiCMOS technology. Usage of bias and gain control simultaneously to achieve high input-referred third-order intercept point (IIP3) is demonstrated. A charge pump is used to transform the RF output signal of LNA to dc control signal. Measurement results show that with 3.3V power supply, the LNA exhibits a tunable bias from 3mA to 10.85mA with gain tuning range of 13dB, and a 14.5dBm IIP3 improvement. In the high gain mode, the noise figure of 2.82 of the LNA is achieved.

Index Terms — LNA, charge pump, WLAN, adaptive biasing, variable gain, IIP3.

I. INTRODUCTION

In modern integrated RF transceivers for mobile communications, the low-noise amplifier (LNA) is one of the most critical building blocks since its NF and gain contribute significantly to the overall signal-to-noise ratio (SNR) of the receiver. It is included in the receiving chain and directly connected to the antenna or placed after the radio frequency (RF) bandpass filter (i.e., the image rejection filter). It must enhance input signal levels at gigahertz frequencies while preserving the SNR and avoiding inter-modulation distortion. Since in most RF receivers the input power ranges from -20 to -110 dBm, noise figure and linearity are very important parameters of LNA's. Design of LNA involves trade-off between noise figure (NF), matching, stability, gain, and input-referred third-order intercept point (IIP3) etc [1].

To improve the linearity of the LNA, we tune the bias and gain of the LNA simultaneously. The basic bias or gain control network of LNA needs a control signal, the amplitude of which should be proportional to the input RF magnitude. One of the popular methods of controlling the bias and gain of the LNA is by introducing an external control signal from baseband. This scheme of gain control needs the baseband processor detecting the power of the receiver output and feedback the control voltage to the LNA. Generally, this control scheme is complicated and digital. However, the control scheme proposed in this paper doesn't need any other external signals from baseband and realizes the gain control totally by the LNA itself. Any more, it can tune the gain of the LNA continuously. In the design, charge pump is used to convert the output RF signal of LNA to a dc signal, the amplitude of which is proportional to the input RF power of the LNA. The advantage of this control scheme is its simplicity and the analog control of the bias and gain. On the other hand, due to the charge time for the charge pump to convert the RF signal to dc signal, there will be some time of lag in the control. However, in the Wireless LAN application,

usually the received signal varies slowly, and this variability is often due to the change of environment (such as temperature), the transfer between far and near transmitter-receivers or the slow decline of the receive signal in the transmission. Considering the slow variability of the signal to be received, this novel control scheme is a feasible and effective control technology.

II. LNA CIRCUIT DESIGN WITH ADAPTIVE BIASING AND VARIABLE GAIN

The block diagram of the adaptively biased and variable-gain LNA is shown in Fig. 1. It consists of two negative feedback control networks, one of which is designed to tune the collector bias current of the first stage of the LNA. When the input power is high, the collector bias current of the LNA is tuned to be greater. According to the relationship of collector current density with IIP3 of the LNA, we get higher IIP3 at greater collector bias current [2]. On the other hand, the gain control network helps to reduce the gain for high input power, which also results in improved linearity when LNA input power is high.

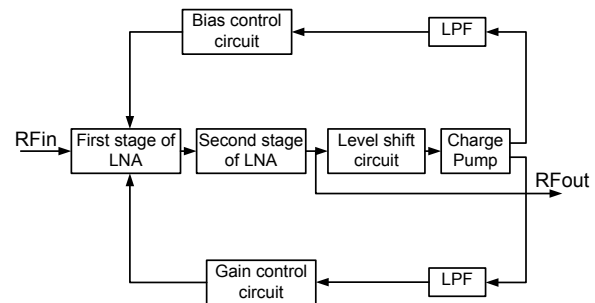


Figure 1. The LNA block diagram with the adaptive biasing and variable gain.

In Fig. 1, the first stage of the two-stage LNA adopts cascode architecture with inductors at the base and emitter of the input transistor Q0, which, respectively are used for input matching at the desired frequency. A load inductor at the collector of the cascode transistor Q1 is used as shown in Fig. 2 [3]. The cascode architecture seems to be the best basic structure for a good isolation between input port and output port, and also a good trade-off between low noise, high gain, high linearity and stability [4], [5]. In Fig.2, the resistor Rf and capacitor Cf, which are connected between the output node and the input node of the second stage of the LNA, used as a shunt feedback, linearize the circuit and lower the

output impedance of the LNA. This makes the LNA easy to drive the off-chip 50ohm resistance of test equipment.

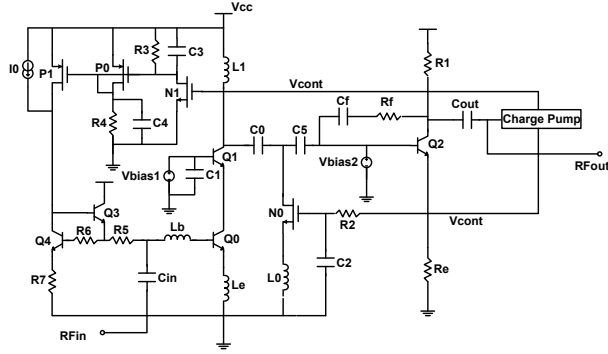


Figure 2. The circuit diagram of the adaptively biased LNA with variable gain.

The function of the level-shift circuit in Fig. 1 is to make the charge pump control the MOSFET N0 and N1 effectively and realize the bias and gain variability in an enough range (Fig. 2). Since the input of the charge pump comes from the output of the LNA, which usually is very weak, in the conversion scope of the charge pump, considering that the threshold voltage of the MOSFET used in this paper is more than 550mV, without a dc-level-shift circuit, it will be difficult to make the MOSFET N0 and N1 work in the triode region in the scope of input power and get enough control range.

A. LNA Output Level Check-Up Circuit—Charge Pump

The output signal of LNA is RF signal at 5.2 GHz, which cannot be used as feedback to control the gain of the LNA itself, or there will be serious positive feedback and the closed feedback circuit may not work properly. So, we introduce a kind of AC-DC converter — charge pump, which can be used to convert RF signal into dc signal. AC-DC charge pump usually consists of capacitor-diode network, as shown in Fig. 3. In order to improve the output voltage of the charge pump and increase the conversion speed as much as possible, the voltage on the diodes should be as small as possible. Thus, in this design, Schottky Barrier Diode (SBD) with smaller forward active resistance is used.

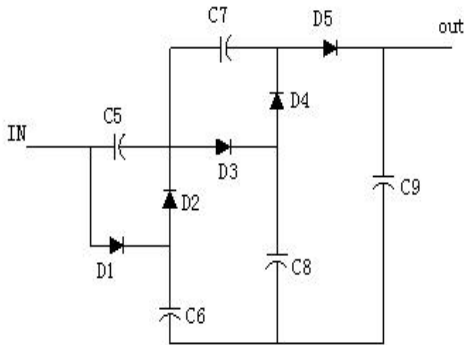


Figure 3. Circuit schematics of the charge pump.

In Fig. 3, all SBDs work as forward active resistors, and capacitors C5, C7 operate as ac coupling capacitors. The

multiplying capacitors C6, C8, C9 are respectively treated as independent dc voltage sources. The voltage of these voltage sources are decided by the input power, the charge time of the charge pump and the active resistance of the SBDs at the same time. At the beginning, the input signal will charge up the circuit comprising D1 and C6, and get a dc signal in the positive end of D3. Then this dc signal combined with the RF signal, which is coupled by C5 from the input port, charges up the circuit comprising D3, C8. After multilevel charge-ups and coupling actions, the input RF signal is nearly totally converted into dc signal at the output. The output voltage of the charge pump is expressed as follows:

$$V_{charge_pump} = n(V_i - V_d). \quad (1)$$

where n is the number of the diode in the circuit. V_i is the input voltage at level i and V_d is the voltage drop on the corresponding diode. In the charge pump, the multiplying capacitors and the area of the diodes will both influence the building time of the output voltage, which is expressed as follows:

$$T_{rise} = \frac{C_{load} V_{charge_pump}}{I_{diode}} \propto \frac{C_{load} V_{charge_pump}}{A_{diode}} \quad (2)$$

where I_{diode} and A_{diode} are the average current through the diodes and the junction area of the diodes respectively. C_{load} is the multiplying capacitor of the last level. From (2), we can get the reasonable building time of the output voltage by setting the value of C_{load} and A_{diode} . And when the charge pump has enough charge-up levels, and the building time is long enough, in the range of input RF magnitude, we will get the reasonable dc control signal as we want at the output of the charge pump.

B. Adaptive Biasing for IIP3 Boosting

In Fig.2, The control signal generated by charge pump is connected to the gate of the MOSFET N0 and varies from 550mV to 1.13V. R3, C3, and R4, C4 act as two pairs of low pass filters (LPFs) respectively. P0 and P1 constitute a current mirror, which mirrors the current generated by N1 to the drain of the MOSFET P1. This current in parallel with the current source I0 controls the collector current of the first stage of the LNA. When the input power is low, the control signal V_{cont} generated by charge pump will be low and the current in the drain of P1 be small. Hence, the first stage of the LNA works at a low collector current bias and we get a relatively low IIP3 which will satisfy the need of the linearity at low input power. On the other hand, when the input power is high, we get high collector current in the first stage of the LNA. Then, high IIP3 will be attained to satisfy the need of the linearity at high input power. When the input power changes continuously, we realize controlling the bias and the IIP3 of the LNA continuously [2]. The bias in this design ranges from about 3mA to 10.85mA, as shown in Fig. 4.

According to those discussed above, we get that we can improve the linearity of the LNA by increasing the bias of it. So, when input power changes from -50dBm to -20dBm, we can improve the IIP3 of LNA from -15dBm to -0.54dBm, as shown in Fig.5.

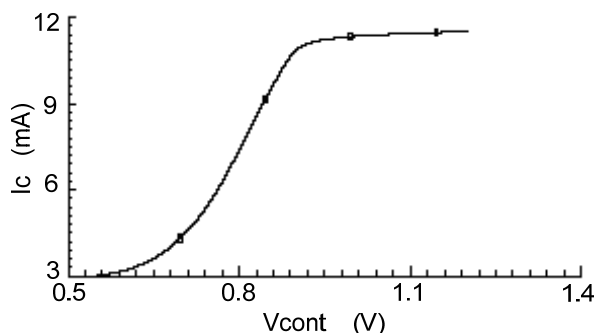


Figure 4. Simulated LNA bias versus the control signal V_{cont} .

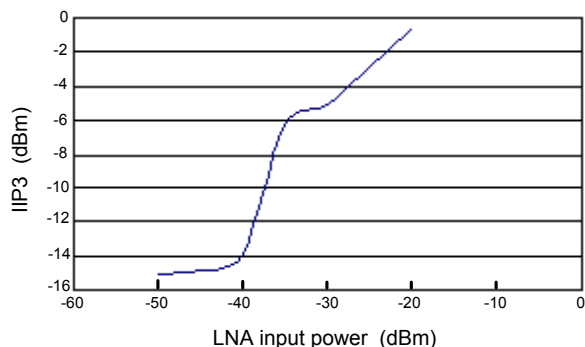


Figure 5. Measured IIP3 as a function of LNA input power.

C. Gain Control Network

In high input power, we need very small gain in LNA, and also, when we control the bias of the LNA, the gain will change as bias changes, so we design a gain control circuit to decrease the gain in high input power of the LNA. As shown in Fig. 2, The transistor N0 in series with the inductor L0, connected between the output node of the first stage to ground, is designed to reduce the output impedance of the first stage of the LNA[6], [7]. The gate control voltage is varied from 550mV to 1.13V (outputted by charge pump). When V_{cont} varies from 550mV to 1.13v, N0 works in the triode region, in which the channel between source and drain of MOSFET can be expressed as a voltage-controlled linearized resistor with the value of:

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \quad (3)$$

where μ_n is the average mobility of the electrons in the channel, C_{ox} is the gate oxide capacitance per unit area, W/L is the ratio of the width to the length of the gate. V_{GS} is the gate-source voltage of N0, which is equal to V_{cont} , and V_{TH} is the threshold voltage of the transistor. As predicted by (3), R_{on} is inversely proportional to V_{cont} , and then the total load

resistance of the LNA is inversely proportional to V_{cont} . Hence, the gain of the LNA is inversely proportional to the control signal V_{cont} . When $V_{cont} = 550\text{mV}$, the gain control circuit offers high impedance. Then, the whole LNA operates in High Gain mode. When $V_{cont} = 1.13\text{V}$, N0 will offer low impedance, which reduces the gain of the first stage of the LNA. We can see the gain variation as control signal changes in Fig.6.

After the charge pump, there follows a LPF, consisting of R2, C2, which are designed to remove the weak RF signal in the output of the charge pump. Generally, the automatic gain control circuit should have a low-pass characteristic, that is to say, the closed circuit should have no response to change of signals which have a higher frequency than specified, but only respond to the slow change of signals which have a lower frequency than specified. For example, the closed circuit of a communication receiver always has an upper-limit frequency of about 10~20Hz.

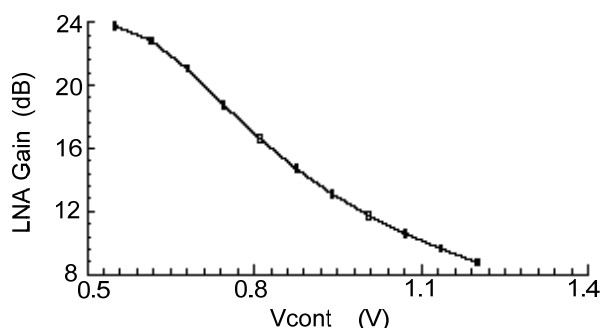


Figure 6. Simulated LNA Gain versus the control signal V_{cont} .

III. EXPERIMENTAL RESULTS

The adaptively biased and gain control LNA is implemented using standard 0.5um SiGe BiCMOS technology. The presented LNA with adaptive biasing has been tested and the performance is almost consistent with the simulation results with SpectreRF in Cadence environment. When the input power is as big as -20dBm, getting rid of the 550mV provided by the dc level shift circuit, the charge pump can get an output dc voltage of about 590mV. The slight deviation from simulation results is the noise in the input of the charge-pump which amplifies the charging effect and level up the output voltage. From the above analysis, in this condition the LNA is working in the Low Gain Mode. When the input power is lower than -20dBm, the dc level charged up by the charge pump will be lower than 580mV, thus the gain will become bigger. Until the signal drops to be lower than -40dBm, due to the voltage drop on the diodes, the charge pump has little conversion effect. In this condition, the gain of the LNA will be the highest.

The test results are summarized in TABLE 1, in which the performances of LNA in different input power are listed for comparison. About 7.8mA bias control and 13dB gain control are realized. In the high gain mode, the noise figure is a bit higher than the simulated value, due to the gain reduction of the LNA. If the influence of test equipment is removed, the result will consistent well with the simulation

results. And from low input power to high input power, IIP3 is improved by almost 14.5dB. As shown in TABLE 1, at high input power, the NF of the first stage of the LNA is greater than that at low input power, which is caused by the bias adjustment. FuKui showed that the minimum achievable NF for a bipolar device in a common-emitter configuration when matched to its optimum noise figure source impedance is given by:

$$NF_{\min}(J_C) = 1 + \frac{n}{\beta_{DC}} + \sqrt{\frac{2J_C}{V_T} (r_e + r_b)_u \left(\frac{f^2}{f_T^2} + \frac{1}{\beta_{DC}} \right) + \frac{n^2}{\beta_{DC}}} \quad (4)$$

where J_C is the dc collector current density. Almost all parameters in (4) (except for V_T) are bias dependent, i.e., they are a function of J_C . Consequently, it is useful to plot the NF_{\min} versus collector current density (or the NF_{\min} versus collector current at the fixed transistor size, as shown in Fig. 7), very carefully taking the bias dependencies into account. And we can see that NF_{\min} has indeed an absolute minima when J_C is assigned a certain value. As shown in Fig.7, no matter bigger or smaller than this certain value of J_C , as long as deviating from this point, the NF_{\min} will become higher. Consequently, when J_C increases as input power increases, the NF_{\min} will become higher, resulting in a worse noise performance in high input power [2].

TABLE I. SUMMARY OF MEASURED RESULTS

LNA input power(dBm)	≤-50	-40	-30	-20
1 st stage bias current(mA)	3.015	3.4	10.5	10.85
Gain(dB)	20.84	19.1	10.04	7.9
NF(dB)	2.82	2.87	4.15	4.61
IIP3(dBm)	-15.08	-13.59	-5.08	-0.54

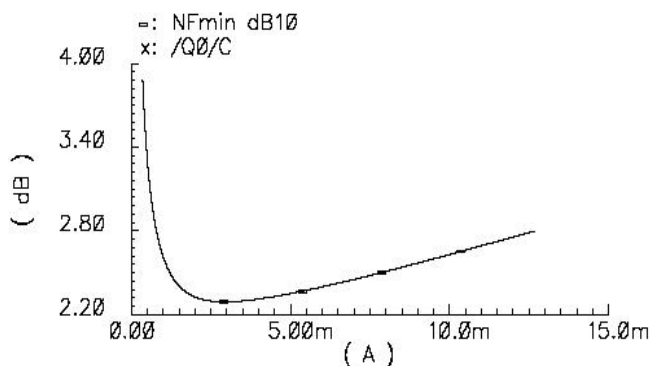


Figure 7. Simulated NFmin versus collector current

IV. CONCLUSIONS

In this paper, the adaptively biased and variable gain LNA using the charge pump as a level check-up circuit in the output of the LNA to generate the control signal and control the bias and gain of the LNA is introduced for the first time. This scheme realizes the independent and continuous bias and gain control of the LNA simultaneously. Not only a range of 7.8mA bias current control is attained, but we get about 13dB gain control at the first stage of the LNA. Hence, the linearity of the LNA is improved greatly. The LNA and its associated 5GHz WLAN receiver front end was implemented in a 47GHz SiGe technology. The LNA with the adaptive biasing circuits occupies 0.4 mm² die area as shown in Fig. 8.

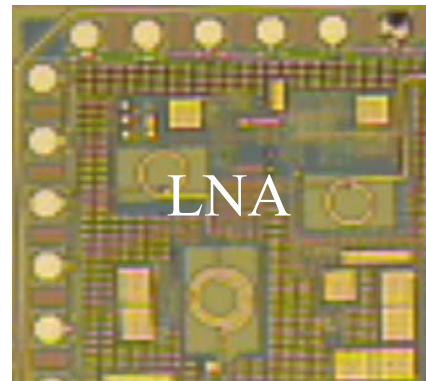


Figure 8. The die photo of the LNA with adaptive biasing.

REFERENCES

- [1] B.Razavi, "RF Microelectronics", PTR: Prentice Hall, 1998.
- [2] Giovanni Girlando and Giuseppe Palmisano, "Noise Figure and Impedance Matching in RF Cascode Amplifiers", *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, Vol.46, No.11, Nov. 1999.
- [3] D.K.Shaeffler and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol.32, No.5, May 1997.
- [4] Osama Shana'a, Ivan Linscott and Len Tyler, "Frequency-Scalable SiGe Bipolar RF Front-End Design", *IEEE Journal Of Solid-State Circuits*, Vol.36, No.6, June 2001.
- [5] John Rogers and Calvin Plett, "Radio Frequency Integrated Circuit Design", PRT: Artech House, Inc., 2003.
- [6] E.Sacchi, I.Bietti, F.Gatta, F.Svelto and R.Castello, "A 2 dB NF, Fully differential, Variable Gain, 900 MHz CMOS LNA," *Symposium on VLSI Circuits*, June, 2000.
- [7] M.Kumarasamy Raja, Terry Tear Chin Boon, K.Nuntha Kumar and Wong Sheng Jau, "A Fully Integrated Variable Gain 5.75-GHz LNA with on chip Active Balun for WLAN", *IEEE Radio Frequency Integrated Circuits Symposium, 2003*