

# A 3-Dimensional Vernier Ring Time-to-digital Converter in 0.13 $\mu\text{m}$ CMOS

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**Abstract**— A 3-dimensional Vernier ring time-to-digital converter (TDC) is presented for the first time that greatly improves the measurement time and power consumption and achieves large detectable range and fine resolution simultaneously. The TDC prototype chip achieves 16.5-ps resolution and an 8-bit detectable range with 0.16 mm<sup>2</sup> die area in a 0.13 $\mu\text{m}$  CMOS technology. The power consumption for the entire TDC is only 4.5mW with 1.5V power supply at 15MSps sample rate.

## I. INTRODUCTION

Time resolution, detectable range, measurement time, power consumption and die area are most important concerns in TDC designs for all-digital phase-locked loop applications. Shrinking the time resolution has fueled the exploration of various TDC architectures recently [1-3]. Time-amplifier based two-step TDC amplifies the time residue and then quantizes it with a delay-line based coarse TDC [1]. Various Vernier TDCs have been implemented with fine resolutions. However, they all struggled with low efficiency, long testing time and high power consumption for measuring large time intervals. Recently a 2D Vernier structure was developed to reduce the number of delay stages required by linear TDCs [2]. Vernier ring TDC re-uses the hardware by placing the delay stages in a ring format and thus extends the detectable range without compromising the resolution [3]. To further improve the Vernier ring TDC (VR-TDC), this paper presents a 3-dimensional Vernier ring TDC that re-uses two delay rings and a comparator matrix. The proposed TDC greatly improves the measurement time, efficiency and power consumption. Moreover, it can achieve large detectable range without compromising the resolution.

To explain the concept of the proposed 3-D Vernier ring TDC, Fig. 1 illustrates a delay-space that is composed of a slow-ring with 7 slow delay stages, a fast-ring with 5 fast delay stages and Z planes formed by comparator matrix. As shown, two delay axes with a comparator matrix form a 2-D delay plane. While the delay plane can be extended to a 3-D delay space by adding more 2-D delay planes, we implemented the 3-D space by connecting the Vernier delay chains to form Vernier delay rings and reusing comparator matrix. The propagation delay per stage in the slow and fast rings are  $t_s$  and  $t_f$  respectively. The exemplary 3-dimensional Vernier ring TDC evolves from a 5-stage VR-TDC [3] by extending the slow-ring to 7-stages and adding two comparator columns to the

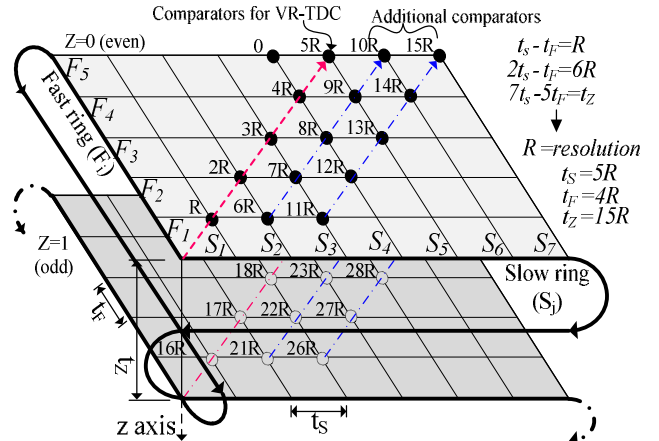


Fig. 1 Conceptual view of 3-D Vernier delay-space.

right-side of the existing comparator line (labeled with red) to form a 2-dimensional comparator matrix. The 2D placement of the comparator array extends the detectable range from 5R to 15R comparing to conventional Vernier TDC, where  $R = t_s - t_f$  is TDC time resolution.

Assuming two input signals start their propagations from the origin on the plane  $Z=0$  along two rings. The 2D comparator array compares the edges of two signals in fast- and slow-rings every lap. If the lag signal propagating along the fast-ring doesn't catch up with the lead signal propagating along the slow-ring after one lap of propagation, i.e., the input time interval is larger than  $15R$ , the race goes into the 2nd lap with re-use of the delay rings and the comparators. In this scenario, the race in the 2nd lap is represented in the delay-space using another plane denoted  $Z=1$ , where the detectable range goes from 16R to 30R. The re-use of hardware will continue until the catch occurs and the delay-space can theoretically contain any number of planes. Similar to Vernier ring TDC, a large time interval is first interpolated with coarse resolution, i.e., the period of slow-ring prior to the arrival of the lag signal at TDC input. After lag signal arrives, the residue of the coarse interpolation will be automatically quantized with a fine resolution, which is the delay difference between fast- and slow-stages. Thus, the maximum detectable range of the proposed TDC can be infinitely large without sacrificing the fine resolution. The delay difference detected by a comparator located at  $(i, j, z)$  in delay-space is given by

$$D(i, j, z) = j \cdot t_s - i \cdot t_f + z \cdot (7t_s - 5t_f) = i \cdot R + (j-i)t_s + z \cdot t_z \quad (1)$$

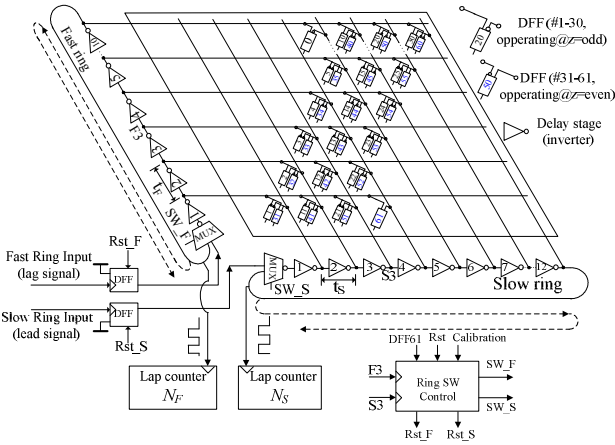


Fig. 2 Block diagram of the proposed Vernier ring TDC core

where  $i, j, z$  are the coordinates in exemplary delay-space.  $R$  is the minimum time interval and  $t_z = 7t_s - 5t_f = 15R$  is the maximum time interval detected by the comparator array on the same  $Z$ -plane. The delay difference in all  $Z$ -planes becomes a monotonic function without overlap when  $2t_s - t_f = 6R$  and  $7t_s - 5t_f = 15R$ .

## II. CIRCUIT IMPLEMENTATION

### A. Vernier ring TDC core

Based on the concept proposed above, we implemented a novel Vernier ring TDC chip that contains 10 fast stages, 12 slow stages, two MUXs and 62 DFF comparators, as shown in Fig. 2. DFF1 to DFF30 works in the odd laps while DFF31 to DFF61 operates in the even laps since output of each delay stage toggles between rising and falling edges when two signals are propagating in two rings lap by lap. The implemented Vernier TDC chip can detect a minimum time interval of  $R$  that is set by the delay difference of two Vernier rings and can be programmed to a very small delay. Without increasing the delay stages and comparators, this TDC can measure very large time intervals as long as the counters have sufficient number of bits to hold the data. Unlike the conventional Vernier TDC that requires large testing time to measure large time interval, the measurement time for the proposed 3-dimensional Vernier ring TDC has been reduced. For instance, the time taken to measure the time interval of  $30R$  requires only propagating 12 delay stages instead of 30 stages needed by a conventional Vernier TDC.

Also included in the TDC core are two input-DFFs, a ring switch control unit, a fast-ring lap counter ( $N_F$ ) and a slow-ring lap counter ( $N_S$ ). Initially control signal  $SW_S$  and  $SW_F$  switch two MUXs to feed input lead signal and lag signal into the slow ring and fast ring, respectively. After around 3 inverter-delays, rising edges at  $F3$  and  $S3$  trigger two MUXs to switch to the outputs of the last stages of two rings to close two rings. This enables two input signals to propagate in the rings lap by lap until the lag signal catches up with the lead signal. When the catch occurs, two MUXs are switched back to the ring inputs to break two rings. Meanwhile, two input-DFFs are also reset by the first rising edges at  $F3$  and  $S3$ . The

propagating signals then stop at the end stages of two rings and the TDC core are ready for the next measuring cycle. To avoid causing unexpected toggle of delay stages when two MUXs switch back to the initial positions, the output of two DFFs need to be reset to “zero” before breaking two rings. Two input DFFs are used to isolate two delay rings from the input signals when two rings are cut off.

The mechanism of breaking two rings will greatly simplify the design and save power. For the ring delay structure, counting the lap number is a challenge to the design. The delay variation between the triggering signal and stop signal of a counter may cause the miscoding of lap number. For instance, the triggering signal of the slow-ring lap counter ( $N_S$ ) is from  $S12$  while the stop signal is activated by detection of the catch-up. The catch-up could occur at any stage in the slow ring. Breaking two rings can simplify the redundant circuitry to avoid miscoding [3].

As we know in the conventional Vernier delay line TDC, two signals will propagate same number of delay stages before the lag signal catches up with the lead signal. In the proposed Vernier TDC, two lap counters ( $N_F$  and  $N_S$ ) record the number of laps that the signals have propagated in each ring before the catch-up happens. The number of laps that two signals have propagated during the fine interpolation should be equal since the two rings are disconnected immediately after the catch-up is detected. Therefore, the difference between two counters, namely  $N_S - N_F$ , is the number of propagation laps in the coarse interpolation while the  $N_F$  is the number of propagation laps in the fine interpolation. Detecting the catch-up before two signals passing the MUXs is critical for the design. We find the delay difference between delay stages  $F1$  and  $S4$  is equal to the one between  $F1$  and  $S1$  in the next lap. DFF61 is connected to the outputs of  $F1$  and  $S4$ . A “01” transition at DFF61 output indicates the catch-up happens at the very lap and the detection is 9 fast-stages ahead of the switches, which relaxes the timing requirement of the ring-switch-control unit. Thus DFF61 can be used to monitor the catch-up of the two signals.

As discussed above, a quantitative relationship between the delay-per-stage of two rings,  $t_s$  and  $t_f$ , need to be guaranteed to ensure that there is neither overlap nor gap in detectable range ( $DR$ ) between two adjacent comparator columns. For example, the dateable range of the first and second columns of the comparator array are  $(t_s - t_f) \leq DR_1 \leq 10(t_s - t_f)$  and  $2t_s - t_f \leq DR_2 \leq t_s + 10(t_s - t_f)$ , respectively. Thus  $t_s = 10(t_s - t_f) = 10R$  and  $t_f = 9R$  where  $R = (t_s - t_f)$ . The validity of these equations might be dependent on the process, voltage and temperature variation. Hence calibration is necessary for the proposed Vernier TDC. DFF0 is employed to calibrate the delay-per-stage in the fast-ring [2] to ensure that  $9t_s = 10t_f$ . Consequently, as shown in Fig. 3,  $t_s = 10R$ ,  $t_f = 9R$  and  $t_z = 12t_s - 10t_f = 30R$ . The period of the slow-ring is  $24t_s + 2t_{sw}$ , which is the coarse resolution of the TDC.

Fig. 3 (a) depicts the block diagram of the proposed Vernier TDC chip. The pre-logic unit determines the lead and lag signals from the reference clock and feedback signal, then switches the lead signal to the slow ring and the lag signal to the fast ring, and outputs a sign bit [3]. The splitter generates

differential signals for the use of the following differential TDC core. The outputs of 61 DFFs (1-61) are combined into a 61-bit thermometer code to find the location where the “01” transition happens.

Similar to any other thermometer-code-encoding circuits, the disturbance in the circuit and the variation of delay-per-stage in either fast or slow ring may cause the bubble pattern, for instance “...00010111...”, in the thermometer code. The bubble correction circuit built with the following logic equation will not only get rid of the erroneous encoding, but also detect the real “01” transition and output “one” at the corresponding bit.

$$BC_{(i)} = (DFF_{(i-1)} \oplus DFF_{(i+2)}) \cdot (DFF_{(i)} \oplus DFF_{(i+1)}) \quad (2)$$

Then the outputs of bubble correction circuit are converted to a 6-bit binary code  $TH$ .

Fig. 3(b) shows the timing diagram of the 3-dimensional Vernier ring TDC. This diagram indicates the measured input time interval consists of two parts. The first part is coarse interpolation result  $(N_S - N_F)(240R + 2t_{SW})$  while the second part is the fine interpolation result  $(60N_F + TH)R$ . Thus, the input time interval can be represented by

$$t_{IN} = \pm[(N_S - N_F)(240R + 2t_{SW}) + (60N_F + TH)R] \quad (3)$$

where the polarity is determined by the sign bit of pre-logic unit and the  $t_{SW}$  is the propagation delay of the MUX.

### B. Circuits of the main building blocks

Fig. 4-6 gives the circuits of the main building blocks of the TDC. The circuit of pre-logic unit is shown in Fig.4(a). The comparator in the pre-logic unit determines whether the reference signal leads or lags behind the feedback signal and outputs the sign bit. The comparator then is reset after both reference and feedback signals arrive at end stages. Fig.4(b) shows the circuit of splitter which converts a single-ended signal to a differential signal. The transmission gate can compensate the delay of the first inverter in lower delay line. Two Schmitt trigger circuits are embedded in the splitter to increase noise immunity.

Fig.5 shows circuits of delay stage and differential DFF. The pseudo-differential inverter is employed as delay stage to suppress the common mode power supply noise. Also the DNL due to unmatched strength between pull-up and pull-down in the delay stage will be improved since each stage outputs both rising and falling edges. The inverter delay can be fine tuned by  $V_{ctrl}$  and  $V_{bias}$ , or coarsely adjusted through  $E1$ - $E2$  turning on or off binary-weighted current sources and sinks. For testing purpose, we brought tuning voltages  $V_{ctrl}$  and  $V_{bias}$  off-chip for tenability. As shown in Fig.5(b), the differential DFF operates as the phase error comparator in the proposed TDC. Compared to the arbiter structure in the Vernier ring TDC, this differential DFF does not need be reset every lap when determining the sequence of arrival, which greatly simplified the design of TDC. The presented differential DFF also features a matched delay between two complementary signals.

Fig. 6 depicts the simplified circuit and symbol of the ring switch control unit. Two DFFs are used to keep the status of MUX-control-signal  $SW_F$  and  $SW_S$ . In every operation cycle, these two DFFs will be reset by a global reset signal “ $Rst$ ” before lead and lag signals come to the inputs of TDC

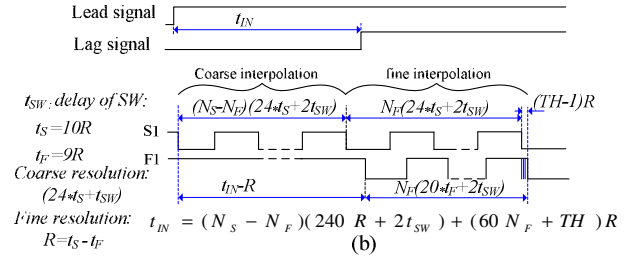
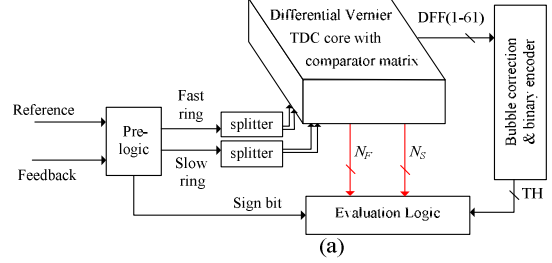


Fig. 3 (a) Block and (b) timing diagrams of the proposed TDC chip.

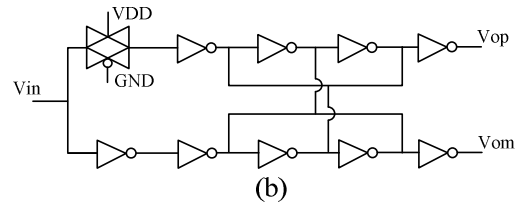
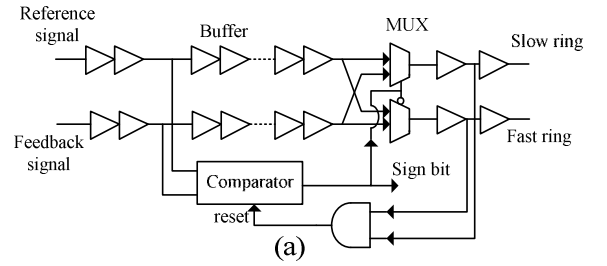


Fig. 4 Circuits of (a) pre-logic and (b) splitter.

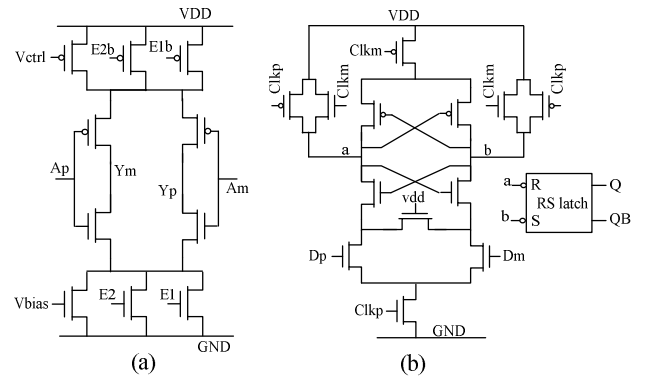


Fig. 5 Circuits of (a) delay stage and (b) differential DFF

core. After the lead and lag signals first time arrives at the 3rd delay stage of each ring, the rising edge of the 3rd delay stage output ( $S_3$  or  $F_3$ ) will trigger the corresponding DFF. These DFFs will output “one” to close the rings when the “calibration” is disabled (set to logic “zero”). In addition, the “01” transition at the DFF61 will reset the two DFFs in the switch control unit therefore break two rings to terminate the propagation of both lead and lag signals. When TDC works in the calibration mode, the two rings are always cut off since two DFFs will output “zero” all the time.

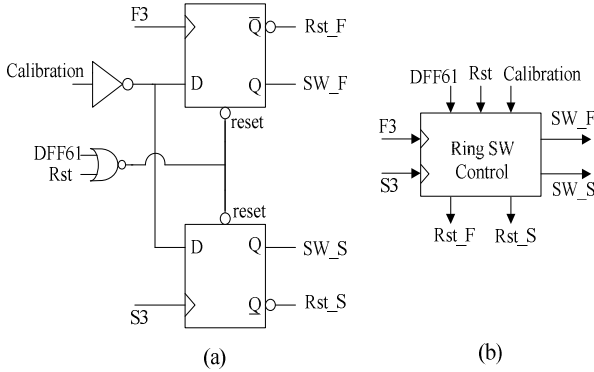


Fig. 6 (a)Simplified circuit and (b)symbol of ring switch control unit

### III. MEASUREMENT RESULTS

The prototype of the TDC was implemented in  $0.13\mu\text{m}$  CMOS technology. Fig.8 shows the chip photo of the proposed TDC. The TDC core occupies  $0.11\text{ mm}^2$  while TDC total area is  $0.16\text{ mm}^2$ . The TDC chip consumes only  $4.5\text{mW}$  under a  $1.5\text{V}$  power supply while operating at  $15\text{ MSPS}$ . Compared to the Vernier ring TDC [3], the proposed 3-dimensional Vernier TDC improves measurement efficiency, area and power consumption. Compared to 2D Vernier TDC [2], the proposed TDC also extends the detectable range by employing Vernier rings for hardware re-use.

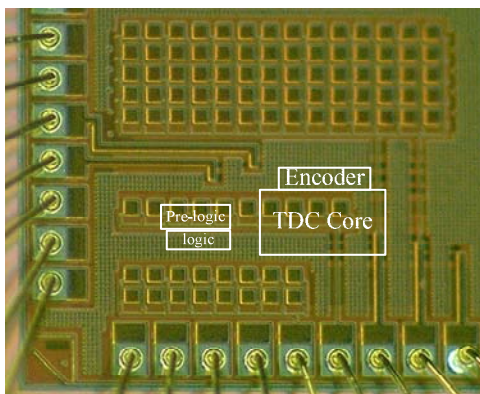


Fig. 7 Chip photo of the proposed TDC

Fig.8(a, b) shows the measured TDC output code distributions for two inputs with constant delays. The standard deviation of two distributions (code 209 and 210), each with total 8096 hits, are  $0.49\text{LSB}$  and  $0.37\text{LSB}$ , respectively. The

distributions indicate a good stability of the proposed structure. Fig.9 shows the measured TDC transfer characteristics with a time resolution of  $16.5\text{ps}$ . A ramp of phase differences between two input signals, with a step size of  $2\text{ps}$ , was fed into the proposed TDC to generate a ramp of TDC output codes. Note that the measured TDC characteristic curve is affected by the noise coupled from PCB board and the jitter of the available test equipments. The proposed Vernier TDC is capable of measuring a very large time interval almost without extra hardware cost. According to (3), the detectable range is mainly determined by the bit number of the slow-ring lap counter ( $N_S$ ). The proved detectable range shown in Fig.9 is greater than 8 bits.

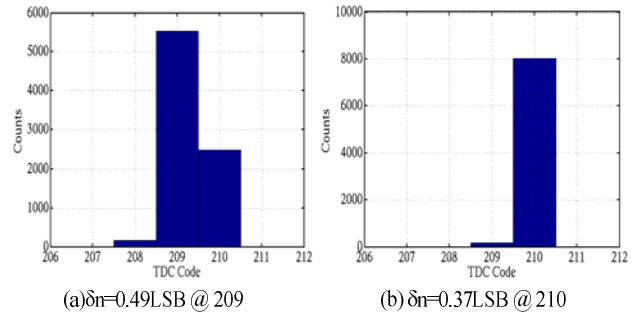


Fig. 8 Measured TDC output code distribution.

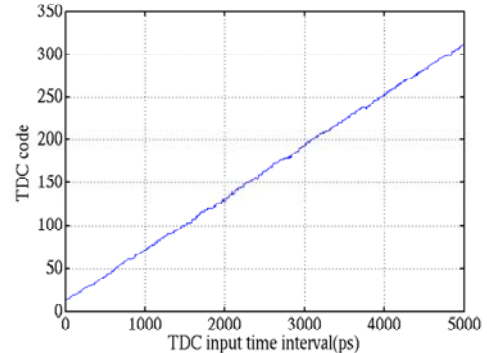


Fig. 9 Measured TDC characteristics

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