

A 2.4GHz front-end with on-chip balun in a 0.13um CMOS technology

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Abstract

A 2.4GHz receiver front-end with on-chip balun implemented with 0.13um CMOS technology is presented in this paper. Based on direct-conversion architecture, the front-end comprises a two-stage LNA (low noise amplifier) with optimized on-chip transformer and quadrature passive mixer. The g_m -boosting technique is employed in 1st stage of LNA to achieve low noise and low current simultaneously. In 2nd stage of LNA, g_m compensation is used for linearity improvement. The front-end draws 26.6mA from 1.2V and simulation result shows a DSB NF of 3.5dB with 52 dB conversion gain.

1. Introduction

In recent years, wireless communication market boom leads to a great demand for wireless connectivity devices. Due to the technology scaling, fully integrated low power wireless transceiver becomes the mainstream of state of art. As a critical building block in the receiver, the performance of RF front end determines the sensitivity and linearity of the system.

Direct-conversion architecture is prevalent in receiver designs. Moreover, an off-chip balun is widely used for a fully differential LNA. However, it increases system cost and reduces the sensitivity at least 1 dB.

In this paper, a 2.4GHz RF receiver front end using zero-IF direct conversion architecture with 0.13um CMOS technology is presented. The architecture includes a two-stage variable gain LNA, a quadrature passive mixer and a TIA (transimpedance amplifier) buffer. For fully integration and cost savings, on-chip transformer and inductors are designed and optimized for input and output matching. The Front-end achieves a voltage gain of 52dB, 3.54dB DSB noise figure and -31dBm IIP3 at high gain mode. The front-end can provide 60 dB gain variation range while drawing 26.6mA from 1.2V supply.

2. Front-end Architecture

Zero-IF architecture is used to achieve high level integration and to avoid the interference of image signal. The single-ended input signal at 2.44GHz is converted to differential by an on-chip transformer. After that, the differential signal is amplified by a two-stage LNA and

subsequently down-converted to baseband signal by a quadrature passive mixer. The mixer commutates only the RF current supplied by a transconductance stage. Mixer linear switches carry no DC current in this structure. The down-converted current is delivered to a TIA buffer which is also a current to voltage converter. The whole front-end has a 60dB variable gain range with 6dB/step. Fig.1 depicts the architecture of front-end for 2.4GHz receiver.

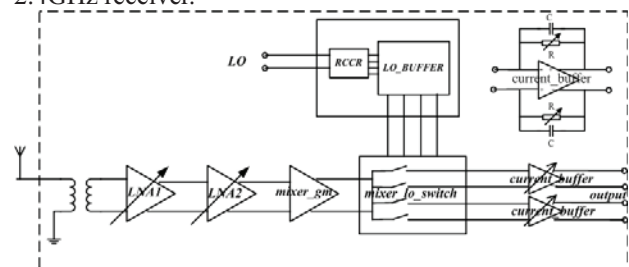


Figure 1 Architecture of the 2.4GHz RF front-end

3. Circuit implementation

3.1 optimization of transformer and inductors

An on-chip balun is designed to achieve high integration and low cost. Further reducing chip area, all transformers and inductors used in this chip are optimized for area efficiency and high Q characteristics.

In order to obtain high Q value inductors, the differential planar spiral inductor is used. Fig. 2 a) shows one of the 3-D inductor layouts and Fig. 2 b) is 3-D layout of on-chip transformer. The transformer is optimized to minimize its coil resistance by stacking multilayer metal. The primary and secondary coils are partially overlapped to get a higher coupling coefficient value and lower parasitic capacitance.

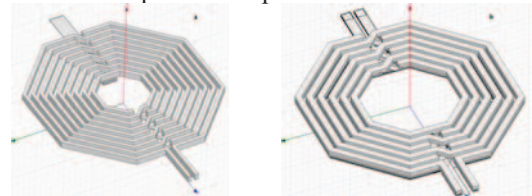


Figure 2 a) 3-D view of one inductor
b) 3-D view of integrated transformer T1

The comparison between simulated and measured results of inductor is shown in Figure 3. The error of L is less than 10% at 2.44GHz as expected. The simulated and measured value of Q differs by 10.3%.

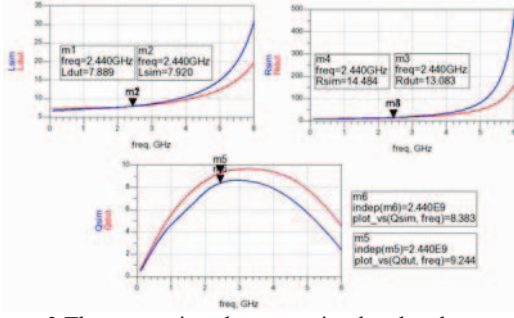


Figure 3 The comparison between simulated and measured characteristics of inductor

3.2 LNA design

3.2.1 first stage of LNA

The LNA consists of two stages. Although common source input stages is adopted more widely, it degrades the linearity and increases the sensitivity of input matching. To get better linearity and more easily matching, the first stage of LNA employ a common-gate topology.

The conventional common-gate LNA (CGLNA) [Fig. 4(a)] matches the input impedance ($1/g_m$) to 50Ω [1]. Ignoring the effects of gate noise, the minimum noise factor is

$$F = 1 + \frac{4kT\gamma g_{d0}\Delta f}{R_s\Delta f} \left(\frac{1}{G_{m,eff}R_s} \right)^2 = 1 + \frac{\gamma}{\alpha} \frac{g_m}{1} \left(\frac{1}{G_{m,eff}R_s} \right)^2 \approx 1 + \frac{\gamma}{\alpha} \quad (1)$$

When $G_{m,eff} = g_m = 1/R_s$.

To optimize the NF of a common-gate input stage and reduce the power consumption, a general g_m -boosting technique is used as shown in Fig. 4 (b). The V_{gs} of M3 is enlarged by the anti-phase signal between source and gate, so that the effective transconductance of M3 is boosted as follows

$$G_{m,eff} = \left(\frac{C_{gs} + 2C_g}{C_{gs} + C_g} \right) g_m \quad (2)$$

Where $cg1 = cg2 = C_g$. g_m is the small-signal transconductance of the MOSFET.

Thus, the noise factor of CGLNA-CCC now becomes

$$F_{CGLNA-CCC} = 1 + \frac{\gamma}{2\alpha} \quad (3)$$

When $C_g \gg C_{gs}$, $G_{m,eff} = 2g_m = 1/R_s$. The effective transconductance is doubled and the noise factor is reduced.

As shown in Fig. 4 (b), the input signal of the first stage, which is based on capacitive cross coupled common-gate LNA (CCC-CGLNA) structure, is coupled from the antenna by the on-chip transformer. Compared with other CCC-CGLNA structure [1], the proposed architecture saves a differential source inductor.

In the design, the capacitor C11 is variable for tuning the tank to minimize the loss of transformer at

2.44GHz. The center tap of secondary coil provides a DC path for the common gate transistors M3 and M4. M1 and M2 are cascode transistors to obtain better reverse isolation. In the meanwhile the gain can be changed by current steering with different size of cascode transistors. Fig.4 c) illustrates the change of the noise figure vs. the small-signal transconductance. The noise performance has a lowest point as the transconductance is increased.

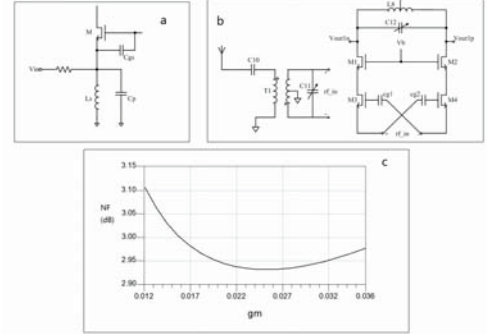


Figure 4 a) the conventional CGLNA
b) CCC-CGLNA integrated with transformer
c) NF of the CCC-CGLNA vs. gm

3.2.2 second stage of LNA

The second stage of LNA aims at achieving high linearity. However, the conventional common gate structure can not meet the demands of high linearity with low power consumption.

For small signal input, the drain current of the simple common source transistor is

$$i_{ds} \approx g_m V_{gs} + g_m' V_{gs}^2 + g_m'' V_{gs}^3 \quad (4)$$

Where $g_m = \frac{\partial i_{ds}}{\partial V_{gs}} \Big|_{V_{ds, const}}$, g_m' is the second derivative of drain

current and g_m'' is the third derivative of drain current.

The better linearity can be attained when g_m'' is closer to zero. A higher V_{gs} is needed for higher linearity in saturation region. However, V_{gs} is limited by the power consumption.

It is known that

$$\begin{cases} g_m'' < 0 & \text{in saturation} \\ g_m'' > 0 & \text{in subthreshold} \end{cases} \quad (5)$$

When changing the bias voltage of MOSFET from saturation to subthreshold, g_m'' of the transistor can be moved from a negative value to a positive value. Thus, the negative value of g_m'' can be compensated with a positive value by two paralleled transistors which are biased in saturation and subthreshold region respectively.

The proposed g_m'' cancelling circuit, which is called the multiple gated transistors (MGTR) [2], is presented in Fig. 5 (a). The linearity can be improved by adjusting the bias and transistor size. Fig.6 shows the compensated result that g_m'' is close to zero in a very wide voltage

range. The second stage of LNA based on the MGTR structure is illustrated in Fig. 5 (b).

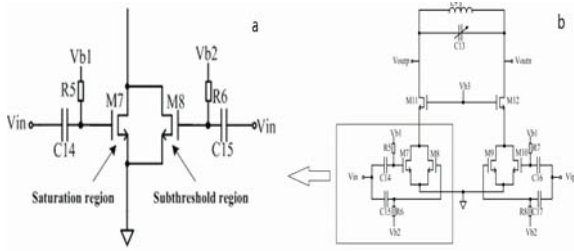


Figure 5 (a) the MGTR (b) the second stage of LNA

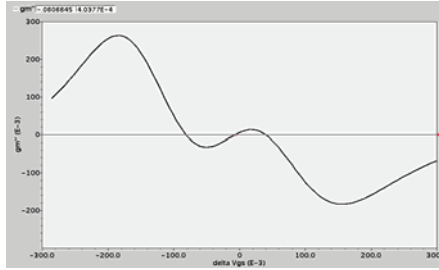


Figure 6 Linearized g_m range of the MGTR

3.3 Mixer design

A quadrature mixer includes a transconductance stage, passive mixing switches, RCCR, LO buffer and TIA buffers as described in Fig. 1. A common transconductance stage, which uses the same architecture as the 2nd of LNA, is used for both IQ paths to reduce power consumption. In order to reduce the flicker noise of mixer, passive linear switches are proven to be a good choice. However, a large amplitude of LO signal is required for passive mixing, which needs more power consumption to guarantee lower flicker noise. The linear switches can be biased in subthreshold region to reduce the current of LO buffer. The LO signal is converted from differential to orthogonal locally by using a RCCR circuit. It achieves a good performance even for long RF signal lines in layout.

Following the quadrature mixer, there is a TIA buffer in both I and Q paths, which is a current to voltage converter and also a 1st order low pass filter.

The gain of mixer can be adjusted in IQ paths respectively by changing the size of resistors in the current buffer (Fig. 1), and the bandwidth of mixer can be adjusted by tuning the capacitor in the current buffer too.

4. Simulation results

The front-end is fabricated in 0.13um CMOS technology with a 1.2V supply. The two-stage of LNA achieves a power gain of 23dB, 3.0dB noise figure and -11.5dBm IIP3 at 2.44GHz. For the whole front-end, resonance is achieved at 2.44GHz with 52dB conversion gain. Figure 7 illustrates the DSB NF of 3.5dB and -31dBm IIP3 at -48dBm input power. The total power

consumption of the front-end is 26.6mA with a 1.2V power supply including the current of LO buffers. The front-end layout floor-plan is shown in Fig. 8, and the die size of front-end is about 880um by 830um.

5. Conclusion

This paper presents a 2.4GHz receiver front-end with on-chip balun implemented with 0.13um CMOS technology. A g_m -boosting technique is presented that achieves a lower NF compared to a conventional CGLNA and consumes less power with on-chip transformer. At the same time, quadrature passive mixer and highly linear LNA adopting g_m compensation by multiple gated transistors are described. The front-end draws 26.6mA from 1.2V and attains a simulated DSB NF of 3.5dB, a conversion gain of 52 dB and IIP3 of -31dBm.

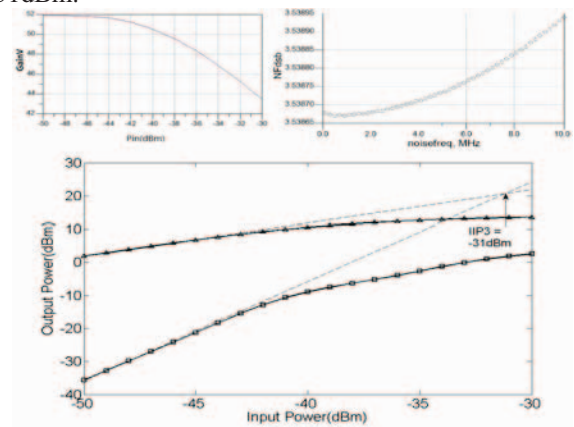


Figure 7 The performance of RXRF

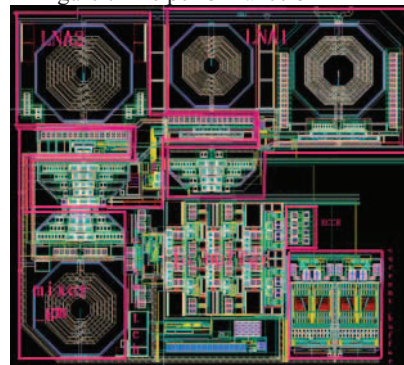


Figure 8 the front-end layout

References

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