

A 12-bit Interleaved OpAmp-Sharing Pipeline ADC for Extreme Environment Applications

Yuan Yao, Desheng Ma and Foster Dai, *Fellow IEEE*
Dept. of ECE, Auburn University, Auburn, AL 36849-5201, USA

Abstract—This paper presents a 12-bit 5MS/s pipeline analog-to-digital converter implemented in a 0.5 μ m CMOS technology for aerospace extreme environment applications with cryogenic and radiation tolerant capability. It is capable of working under ultra-wide temperature range from -180°C to +120°C and at ultra low temperature of -230°C. To achieve higher sampling rate and lower power, time-interleaved architecture and operational amplifiers sharing technique are used. The cryogenic ADC chip consumes only 30.4mW at -230°C from a 3.3V supply voltage. Experimental results show that the proposed ADC can operate under aerospace extreme environment with low power and good robustness.

I. INTRODUCTION

With the development of aerospace exploration, the modular, expandable, and reconfigurable human and robotics systems for aerospace missions clearly requires electronic components and integrated packaged electronics modules which can operate robustly without external thermal control [1]. Thus, in order to remove the bulky protective “warm boxes,” newly-designed electronics systems must robustly operate in extreme environments for aerospace applications, in the ultra-wide temperature (UWT) range from -180°C to +120°C and even the ultra low temperature (ULT) -230°C as well as radiation exposure environments.

High-speed high-resolution Analog-to-Digital Converters (ADC) are crucial building blocks in many of the SoC designs in aerospace applications such as sensors, communication transceivers and controlling systems [2]. However, current ADCs cannot properly operate when exposed to extreme temperature and radiation environments due to the limits of characteristics of fabrication material, model accuracy in cryogenic conditions, and design difficulty in the UWT range. There is an urgent need for ADCs which can robustly operate under extreme temperature environments and radiation exposure. Therefore, this paper presents a cryogenic lower-power 12-bit pipeline ADC capable of operating over the UWT range and under radiation conditions for aerospace extreme environment applications. To achieve higher sampling rate and lower power consumption, time-interleaved architecture and operational amplifiers (OpAmp) sharing are used.

The organization of this paper is as follows. In section II, circuit design details and technical analyses for the proposed 12-bit ADC are presented. The measurement results of the ADC chip in the UWT range are given in section III. Finally, conclusions are drawn in Section IV.

II. ADC ARCHITECTURE

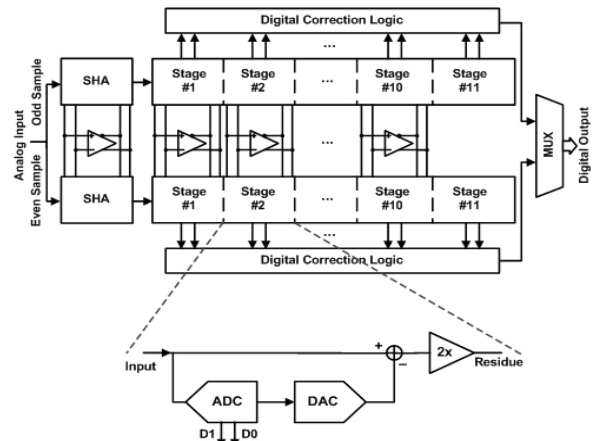


Fig.1 Block diagram of proposed cryogenic pipeline ADC.

The block diagram of proposed cryogenic pipeline ADC is shown in Fig. 1. It consists of two eleven-stage 1.5-bit/stage time-interleaved pipeline ADCs. One pipeline processes the even samples, while the other pipeline works on odd samples. For both pipeline ADC channels, two clock phases, multiplying and sampling, are used and complementary for each other. However, the OpAmp only works in multiplying phase for every single channel, which is half of one complete clock cycle. Therefore, both pipeline ADCs are capable of sharing their OpAmps by only using corresponding multiplying clock phase. This makes a large power saving since OpAmps are the most power-consuming blocks in pipeline type of ADCs. Besides, it can also help to minimize offset and gain mismatches between pipelines that could degrade the ADC’s performance [3]. Note that there is no OpAmp required in last stage which only uses comparator to generate two LSBs.

Each pipeline stage includes a 3-level flash sub-ADC, a 3-level sub-DAC, and a residue doubler. In operation, each stage initially samples and holds the output from the previous stage and the held input is then converted into a low resolution digital code by the sub-ADC and back into an analog representation by the sub-DAC. Finally, the OpAmp residue doubler amplifies the difference between the held analog signal and the reconstructed analog representation to give the residue for the next stage. As shown in Fig. 2, the sharing of the OpAmp is realized by adding controlling switches between OpAmp inputs and outputs. When upper pipeline stage is in sampling phase, the

OpAmp is not needed to finish the input signal sampling action on both C_1 and C_2 which can be done by switching on S_2 and S_3 . Meanwhile, S_{op1} and S_{op2} switch shared OpAmp to lower stage to multiply the residue. In next half clock phase, shared OpAmp is switched back to upper stage for multiplying and lower stage goes into sampling phase. S_2 and S_3 are also switched back to OpAmp circuit to realize residue doubling according to generated digital code.

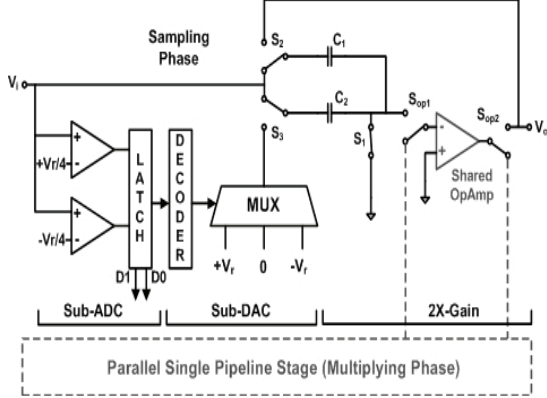


Fig. 2 Simplified schematic of each pipeline stage. Upper stage is sampling the input signal while lower stage is multiplying the residue.

For pipeline ADCs, OpAmps need to provide good open loop gain to assure the accuracy of residue amplifying so that theoretically the whole ADC doesn't generate error code throughout all pipelined stages. The minimum open loop gain of OpAmp used in residue doubler is determined as a function of the ADC resolution. The ideal output voltage of each pipeline stage is

$$V_o = 2V_{in} - S_o V_{ref} \quad (1)$$

where S_o is sub-DAC input selection which ranges among -1, 0, +1. Taking into account the finite OpAmp gain,

$$V_o' = \left(\frac{1}{1 + 1/A_0\beta} \right) (2V_{in} - S_o V_{ref}) \quad (2)$$

where A_0 is OpAmp open loop gain and the feedback factor β is given by $\beta = \frac{C_1}{C_2 + C_1 + C_{in}} \approx \frac{1}{2}$, where C_{in} is the

OpAmp input capacitance. Usually A_0 is very large, so

$$V_o' \approx (1 - 1/A_0\beta)(2V_{in} - S_o V_{ref}) \quad (3)$$

The difference between V_o and V_o' is the multiplying error for each pipeline stage, $V_e = V_o' - V_o$. When $V_{in} = V_{ref}/4$, V_e can have largest error which is

$$\begin{aligned} V_{e_max} &= \left| V_o - V_o' \right|_{V_{in} = \frac{V_{ref}}{4}} \\ &= \frac{1}{2} \frac{1}{A_0\beta} V_{ref} \end{aligned} \quad (4)$$

For a N-bit ADC, first stage multiplying error will be amplified by N-3 stages (error amplification starts from

second stage and no amplification in last stage), so the total multiplying error due to the finite OpAmp gain for the whole N-bit pipeline ADC is

$$V_{e_all} = 2^{N-3} \cdot V_{e_max} \quad (5)$$

In order to avoid code error in last stage, V_{e_all} should be less than half of LSB in last stage which is $V_{ref}/4$.

$$V_{e_all} = 2^{N-3} \cdot V_{e_max} < V_{ref}/4 \quad (6)$$

Finally, the OpAmp open loop gain requirement in the first stage for an N-bit pipeline ADC can be obtained as

$$A_o > 2^{N-1} \quad (7)$$

More generally, for the OpAmp open loop gain requirement used in the i -th stage, it has

$$A_{o_ith} > 2^{N-i} \quad (8)$$

Note that above derivation doesn't count any settling and capacitor mismatch effect which also significantly contributes to pipeline ADC's inaccuracy. Therefore, the required minimum open loop gain for each stage should be increased or even doubled to give more design margin to alleviate those effects, so it has

$$A_{o_ith} > 2^{N+1-i} \quad (9)$$

For proposed 12-bit pipeline ADC, the minimum OpAmp open loop gain in first stage needs to be larger than 72dB.

Among extreme environments in aerospace applications, UWT operation range and high-energy particle radiation are major challenges for proposed pipeline ADC. Device threshold voltage has a significant variation when temperature changes in UWT range. For N-type MOSFETs,

$$\phi_F = kT \ln(N_D / n_i) \quad (10)$$

where N_D is the N-type doping density and n_i is the intrinsic carrier density. With the decrease of temperature, ϕ_F is increased. This effect gives rise to an increased V_{TH} for low temperatures, which also happens for PMOSs. Thus, in cryogenic condition, analog circuits in ADC suffer from smaller transconductance, reduced gain and larger multiplying error. This requires larger gain and better loading capability for OpAmps used in proposed ADC to compensate above degradation. Similarly in layout, wider routing metal and larger area vias can be used to provide larger loading capability and smaller conducting resistance.

On the other hand, aerospace radiation can cause significant offset and inaccuracy in most analog building blocks in pipeline ADC such as OpAmps, switches, capacitors, etc. All these errors are uncorrectable and usually lead to the degradation of ADC's performance. Large W/L transistors are used here to improve radiation-tolerant capability. By providing better matching characteristics, large W/L transistors can overcome threshold shift and gate oxide capacitance increase caused by radiation trapped holes. Meanwhile they reduce not only the

possibility of device invalidation but also the cumulative change in device characteristics due to total dose effect. In order to prevent the single event upset latch-up caused by the positive feedback formed in the parasitic transistors, some special radiation hardened by design (RHBD) layout rules are applied in our design to reduce the well/substrate parasitic resistance and reduce the gain product of the parasitic NPN/PNP pairs. The RHBD rules include: active N+ (P+) guard rings are added around PMOS (NMOS); n-well and p-sub contacts are generously and frequently used; deep trench rings are added for isolation between PMOSs and NMOSs; keep n-well and n+ source/drain far apart if possible.

III. EXPERIMENTAL RESULTS

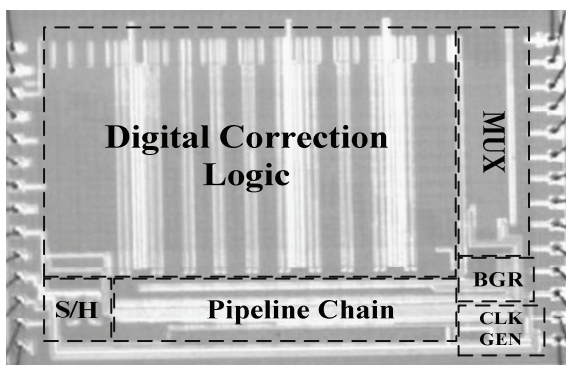


Fig. 3 Micrograph of the 12-bit cryogenic pipeline ADC.

The proposed cryogenic ADC has been implemented in a 0.5 μ m CMOS technology, as shown in Fig. 3. To test the cryogenic ADC, an airproof chamber with electrical heating and liquid Nitrogen cooling is used. The temperature inside the chamber can be controlled from -230 $^{\circ}$ C to +120 $^{\circ}$ C. A cryogenic 12-bit current-steering DAC [4] is used to reconstruct the input signal from ADC's output. During test, both the proposed cryogenic ADC and DAC are placed into the chamber and wired out to test equipments. In order to avoid possible damages in ULT condition, other supporting electronic components and equipments are placed outside the chamber and connected to the ADC through cryogenic-resistant cables.

Figure 4 gives the measured sinusoidal output waveforms and its corresponding spectrums by ADC-DAC test setup pair with 5MHz clock at -230 $^{\circ}$ C for a 50kHz input signal. The SFDR for 50kHz output at -230 $^{\circ}$ C is 53dBc. The spectrum result is measured with a single-ended output only. The measured SFDR also includes the nonlinearity of current-steering DAC, thus ADC may suffer from a degraded dynamic performance when tested with ADC-DAC pair. The total power consumption with 3.3V power supply voltage is only 30.4mW at -230 $^{\circ}$ C. Measurement results have showed that the proposed cryogenic ADC can robustly operate over the complete UWT range from -230 $^{\circ}$ C to +120 $^{\circ}$ C. Table I gives a summary for measured cryogenic ADC performance.

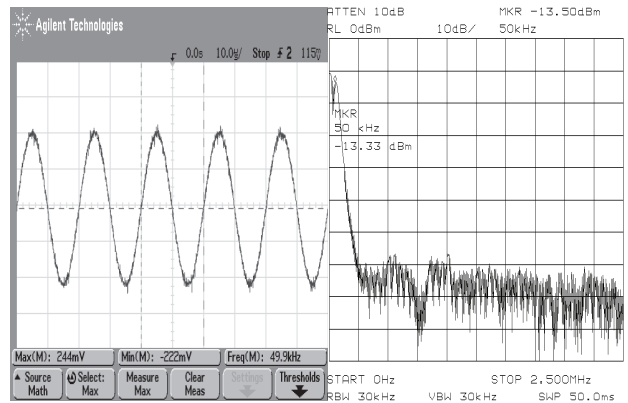


Fig. 4 Measured reconstructed sinusoidal output waveform and its spectrum by ADC-DAC pair for $f_{in}=50$ kHz and $f_{clk}=5$ MHz at -230 $^{\circ}$ C.

TABLE I
SUMMARY OF MEASURED ADC PERFORMANCE

Parameter	Performance
Technology	0.5 μ m CMOS
Temperature Range	-180 $^{\circ}$ C ~ +120 $^{\circ}$ C and -230 $^{\circ}$ C
Resolution Bits	12
Differential full-scale input	-0.5V ~ +0.5V
ADC-DAC Pair SFDR	53dBc@50k,5MS/s, -230 $^{\circ}$ C
Power Supply	3.3 V
Power dissipation	30.4mW@-230 $^{\circ}$ C@5MS/s
Active Die Size	5.2 \times 3.4 mm ²

IV. CONCLUSION

In this paper, a 12-bit 5MS/s pipeline ADC was implemented in 0.5 μ m CMOS technology for aerospace extreme environment applications. The measurement results showed that the proposed ADC is capable of operating over the UWT range from the -180 $^{\circ}$ C to +120 $^{\circ}$ C and at ULT -230 $^{\circ}$ C. In order to achieve higher sampling rate and lower power, time-interleaved architecture with shared OpAmps are used. The ADC's total power consumption with a 3.3 V power supply is only 30.4mW at -230 $^{\circ}$ C at 5MHz clock. Experimental results have shown that the proposed ADC can operate under aerospace extreme environment with low power and good robustness.

REFERENCES

- [1] E.A. Gutierrez-D et al., "Low Temperature Electronics: Physics, Devices, Circuits and Applications," Academic Press, 2001.
- [2] T.N. Andersen et al., "A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18- μ m Digital CMOS," *IEEE JSSCC*, vol. 40, no. 7, pp. 1506-1513, Jul. 2005.
- [3] N. Kurosawa et al., "Explicit analysis of channel mismatch effects in time-interleaved ADC systems," *IEEE Trans. Circuits Syst. I*, vol. 48, pp. 261-272, Mar. 2001.
- [4] Y. Yao et al., "A 12-bit Current Steering Digital-to-Analog Converter for Cryogenic Applications," *IEEE ISCAS*, May. 2006.