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Test Time of Multiplier/Accumulator Based Output Response Analyzer in Built-In Analog Functional Testing

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***Abstract*—A Built-In Self-Test (BIST) approach has been proposed for functionality measurements of analog circuitry in mixed-signal systems. The BIST circuitry consists of a direct digital synthesizer (DDS) based test pattern generator (TPG) and multiplier/accumulator (MAC) based output response analyzer (ORA). In this paper we investigate and discuss the test time required by the ORA for analog measurements such as frequency response and 3rd order intercept point (IP3). We show that the test time can be greatly shortened if the ORA accumulation can be stopped at the right point. Three simple digital circuits are also proposed for such a purpose and their performance is simulated to show how the efficiency of the test time is improved.**

Keywords - BIST; analog functional testing; frequency response measurement, IP3 measurement; test time

I. Introduction and Background

In comparison with the rapid development of the computer automated design (CAD) of analog integrated circuit (IC) design, the testing and measurement of these analog ICs are still far behind, and typically performed manually. With the continuous increase in the operational frequency and complexity of the circuitry, it is even more difficult and expensive to perform test and measurements with traditional manual testing methodologies [1]. Therefore, it becomes attractive to automate the analog testing process with low-cost and built-in test circuitry. Furthermore, it is also most effective to consider testing in the product cycle as early as possible [2]. Therefore, it becomes more attractive to automate the analog testing process with low-cost, built-in test circuitry.

In order to perform a suite of analog functionality tests, such as linearity and frequency response measurements in a Built-In Self-Test (BIST) environment, the frequency spectrum of the signal coming from the device under test (DUT) must be obtained and analyzed by an output response analyzer (ORA) included in the BIST circuitry [3]. A few techniques have been proposed to perform on-chip frequency-domain testing of mixed-signal circuits in [4]–[7]. However, most of these approaches focus only on one or two simple parameter tests such as cut-off frequency of a filter and cannot perform complete analog tests such as frequency response and linearity measurements [1]. Reference [7] utilizes a Fast Fourier Transform (FFT) processor to perform spectrum analysis and has similar abilities to that of [1], but the hardware overhead and power consumption associated with [7] prevent it from being a competitive BIST approach unless the FFT is an inherent component of the system.

A mixed-signal BIST approach has been proposed which includes a direct digital synthesizer (DDS) based test pattern generator (TPG) and multiplier/accumulator (MAC) based output response analyzer (ORA) [1][3]. Because the signal is in digital form, it is easy to include different modulation capabilities in the DDS. Therefore, many analog functional tests, such as magnitude and phase response and 3rd order intercept point (IP3) can be performed with this architecture [1]. Some experimental results for IP3 and frequency response (both phase and gain) using this BIST architecture have been presented in [1] to demonstrate the feasibility and accuracy of the BIST approach.

In this paper, we discuss the test time required by the MAC-based ORA for analog measurements of frequency response and IP3. Both theoretical analysis and simulation results prove that the test time can be greatly shortened if the ORA accumulation can be stopped at the right point. In addition, three digital circuits are proposed to calculate that point and their performance is verified and compared through simulation. The paper is organized as follows. Section II gives an overview of the BIST approach. This is followed by a detailed discussion of the accumulation by the MAC-based ORA in Section III. Simulation results of the proposed circuits are presented in Section IV and the paper concludes in Section V.

II. Overview of BIST Architecture

The mixed-signal BIST architecture, illustrated in Fig. 1, is capable of accurate on-chip analog functional measurements of frequency response and IP3 [1]. The majority of the BIST circuitry resides in the digital portion of a mixed-signal system and includes a DDS-based TPG, MAC-based ORA, and a test controller. The test circuitry added to the analog domain provides loopback capabilities needed to facilitate one or more return paths for the test signals to the ORA. The number and location of these loopback capabilities determines the accuracy and resolution of tests and measurements associated with a given analog function [1].

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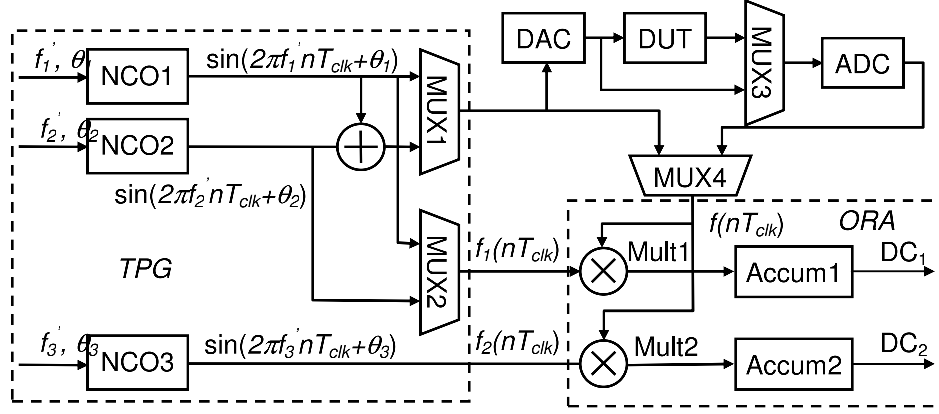

Fig. 1. General model of BIST architecture.

The DDS-based TPG consists of three numerically controlled oscillators (NCOs) and utilizes the existing digital-to-analog converter (DAC) from the mixed-signal system to complete the DDS. Fig. 2 shows a more detailed view of the NCO used in the TPG. The phase accumulator is used to generate the phase word based on the frequency word f and the initial phase word θ. Then the NCO utilizes a look-up table (LUT) to convert the truncated phase word sequence to a digital sine wave sequence. The frequency of the output sinusoidal wave can be determined as

$$f' = \frac{f \cdot f_{clk}}{2^n}, \quad (1)$$

where n is the word width of the phase accumulator. The digital sinusoidal wave serves two purposes. One purpose is to produce an analog stimulus to the DUT through the DAC. The other is to provide in-phase and out-of-phase test tones for the MAC-based ORA. The ORA consists of two sets of MACs. Each MAC receives the output from the DUT $f(nT_{clk})$. The other two inputs, $f_1(nT_{clk})$ and $f_2(nT_{clk})$, are two sinusoidal waves generated by the TPG and used by the MAC pair to perform the spectrum analysis at their frequency.

While performing frequency response measurement, the top branch of MUX1 and MUX2 in Fig. 1 is activated and the DUT is driven by an in-phase signal with a frequency of f_1. At the same time, the NCO_3 generates an out-of-phase signal at the frequency f_1. In this way the ORA is able to measure the DUT output's amplitude and phase response at frequency f_1. By sweeping the frequency f_1 over the bandwidth of interest, the DUT output's frequency response can be obtained.

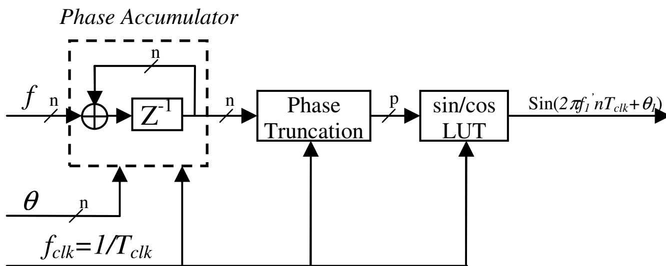

Fig. 2. NCO used in TPG.

On the other hand, while performing IP3 measurement, the bottom branch of MUX1 is activated and DUT is driven by a two-tone signal at frequency f_1 and f_2. Two accumulations are performed by the ORA to determine the spectrum at either frequency pair of f_1 and $2*f_1$-f_2 or f_2 and $2*f_2$-f_1. By doing so, the fundamental and 3rd-order inter-modulation (IM3) terms can be obtained. Then the difference ΔP (in dB) between these two terms can be determined and the input referred IP3 (IIP3) can be calculated by [1]

$$IIP_3[dBm] = \frac{\Delta P[dB]}{2} + P_{in}[dBm]. \quad (2)$$

III. ACCUMULATION BY ORA

The principle operation of the ORA can described as

$$DC_1 = \sum_n f(nT_{clk}) \cdot \cos(2\pi fnT_{clk}), \quad (3)$$

$$DC_2 = \sum_n f(nT_{clk}) \cdot \sin(2\pi fnT_{clk}), \quad (4)$$

$$A(f) = \sqrt{DC_1^2 + DC_2^2}, \quad (5)$$

$$\Delta\phi(f) = -tg^{-1}\frac{DC_2(f)}{DC_1(f)}, \quad (6)$$

where $A(\omega)$ and $\Delta\phi(\omega)$ are the amplitude and phase of the spectrum of the signal $f(nT_{clk})$ at frequency f.

A. Accumulation by Frequency Response Measurement

During a frequency response measurement, the DUT is driven by a single-tone signal and its output $f(nT_{clk})$ can also be modeled as a single-tone signal at the same frequency but with different amplitude and phase offset. Under such a condition, Equation (3) and (4) can be rewritten as

$$\begin{aligned} DC_1 &= \sum_{n=1}^{N} A\cos(2\pi fnT_{clk} + \Delta\phi) \cdot \cos(2\pi fnT_{clk}) \\ &= \frac{AN}{2}\cos\Delta\phi + \frac{A}{2}\sum_{n=1}^{N}\cos(4\pi fnT_{clk} + \Delta\phi) \end{aligned} \quad (7)$$

$$\begin{aligned} DC_2 &= \sum_{n=1}^{N} A\cos(2\pi fnT_{clk} + \Delta\phi) \cdot \sin(2\pi fnT_{clk}) \\ &= -\frac{AN}{2}\sin\Delta\phi + \frac{A}{2}\sum_{n=1}^{N}\sin(4\pi fnT_{clk} + \Delta\phi) \end{aligned} \quad (8)$$

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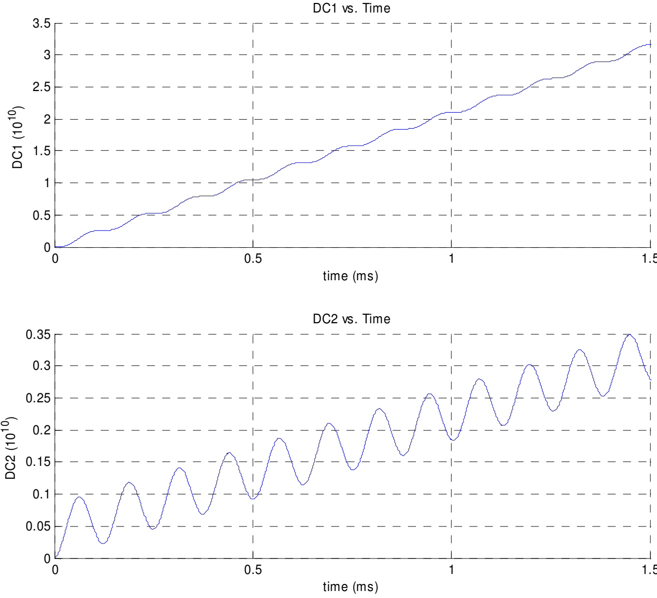

Fig. 3. DC1 and DC2 versus time.

It is obvious that Equations (5) and (6) only function correctly when the second terms in Equations (7) and (8) are negligible when compared to the first terms. This can also be visualized as in the Fig. 3 which shows DC_1 and DC_2 values with respect to the accumulation time when f=4 kHz. The linear components in the DC_1 and DC_2 curves represent the first terms in Equations (7) and (8), and the AC periodic components riding on the linear components represent the calculation errors introduced by the second terms. Since these AC components are bounded, it becomes negligible when the accumulation can be performed for a long period of time.

Another observation from Equations (7) and (8) is that the period of the AC components is *1/(2f)*, which can also be confirmed from Fig. 3. The period reading from the figure is around 125us, which is exactly 1/(2×4 kHz). Therefore, if the accumulation can be stopped at the integer multiple periods (IMPs) of *1/f*, the AC components will cross its zero point and perfectly cancel out the calculation error they would otherwise cause.

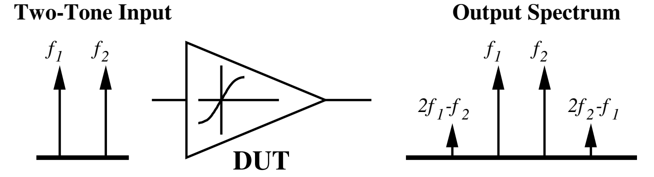

Fig. 4. Two-tone test for IP3 measurement.

B. *Accumulation by IP3 Measurement*

During an IP3 measurement, the DUT is driven by a two-tone signal which is located at two closely spaced frequencies of f_1 and f_2. Because of the DUT's nonlinearity, its output $f(nT_{clk})$ will appear at not only the fundamental frequencies of f_1 and f_2, but also at the IM3 frequencies, as illustrated in Fig. 4. Because the four frequencies are spaced very closely, it is feasible to assume that the spectral components at these frequencies experience almost the same phase delay. Therefore, the DUT's output $f(nT_{clk})$ for IP3 measurement can be modeled as Equations (9) and (10).

The ORA needs to go through two successive spectral analyses to obtain the spectrum of the DUT's output at either f_1 and $2f_1$-f_2 or f_2 and $2f_2$-f_1. And the DC_1 and DC_2 values obtained at these two frequencies can be derived as Equations (11) through (14). The first terms in these four equations are the DC values expected for the spectrum estimation. Therefore, the calculation error coming from the remaining periodic terms must be negligible when compared to the first terms. The most straightforward way to accomplish this is to accumulate long enough to get rid of the error introduced by these periodic terms.

$$f(nT_{clk}) = A_0\cos\left[(2\omega_1-\omega_2)nT_{clk}+\theta\right] + A_1\cos(\omega_1 nT_{clk}+\theta) + A_1\cos(\omega_2 nT_{clk}+\theta) + A_0\cos\left[(2\omega_2-\omega_1)nT_{clk}+\theta\right] \quad (9)$$

$$\Delta P = 20*\log_{10}A_1 - 20*\log_{10}A_0 \qquad \Delta\omega = \omega_2-\omega_1 = 2\pi(f_2-f_1) \quad (10)$$

$$\begin{aligned} \mathrm{DC}_1(f_1) = {} & \frac{A_1N}{2}\cos\theta + \frac{1}{2}\sum_{n=1}^{N}[(A_1+A_0)\cos(\Delta\omega nT_{clk}+\theta) + A_0\cos(2\Delta\omega nT_{clk}+\theta)] + \\ & \frac{1}{2}\sum_{n=1}^{N}\left[A_0\cos((2\omega_1-\Delta\omega)nT_{clk}+\theta) + A_1\cos(2\omega_1 nT_{clk}+\theta) + A_1\cos((2\omega_1+\Delta\omega)nT_{clk}+\theta) + A_0\cos((2\omega_1+2\Delta\omega)nT_{clk}+\theta)\right] \\ \approx {} & \frac{A_1N}{2}\cos\theta + \frac{A_1}{2}\sum_{n=1}^{N}\cos(\Delta\omega nT_{clk}+\theta) + \frac{A_1}{2}\sum_{n=1}^{N}\left[\cos(2\omega_1 nT_{clk}+\theta) + \cos((2\omega_1+\Delta\omega)nT_{clk}+\theta)\right] \end{aligned} \quad (11)$$

$$\mathrm{DC}_2(f_1) \approx -\frac{A_1N}{2}\sin\theta - \frac{A_1}{2}\sum_{n=1}^{N}\sin(\Delta\omega nT_{clk}+\theta) + \frac{A_1}{2}\sum_{n=1}^{N}\left[\sin(2\omega_1 nT_{clk}+\theta) + \sin((2\omega_1+\Delta\omega)nT_{clk}+\theta)\right] \quad (12)$$

$$\mathrm{DC}_1(2f_1-f_2) \approx \frac{A_0N}{2}\cos\theta + \frac{A_1}{2}\sum_{n=1}^{N}[\cos(\Delta\omega nT_{clk}+\theta) + \cos(2\Delta\omega nT_{clk}+\theta)] + \frac{A_1}{2}\sum_{n=1}^{N}\left[\cos(2\omega_1 nT_{clk}+\theta) + \cos((2\omega_1-\Delta\omega)nT_{clk}+\theta)\right] \quad (13)$$

$$\mathrm{DC}_2(2f_1-f_2) \approx -\frac{A_0N}{2}\sin\theta - \frac{A_1}{2}\sum_{n=1}^{N}[\sin(\Delta\omega nT_{clk}+\theta) + \sin(2\Delta\omega nT_{clk}+\theta)] + \frac{A_1}{2}\sum_{n=1}^{N}\left[\sin(2\omega_1 nT_{clk}+\theta) + \sin((2\omega_1-\Delta\omega)nT_{clk}+\theta)\right] \quad (14)$$

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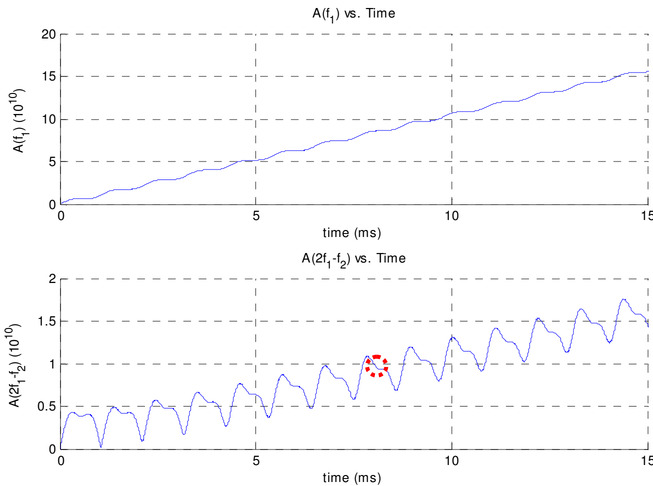

Fig. 5. $A(f_1)$ and $A(2f_1\text{-}f_2)$ versus Time.

Another observation is that the second terms in these equations have a frequency of Δf, which is usually much lower than the frequency of the third terms. This means that the AC calculation errors riding on the desired linear terms will have a period of $1/\Delta f$. Fig. 5 illustrates the simulated $A(f)$, as defined in Equation (5), at frequency of f_1 and $2f_1\text{-}f_2$, while given $\Delta f=f_1\text{-}f_2\approx 900$ Hz. The period of the AC errors read from the figure is also 900 Hz, which also confirms this conclusion. Therefore, if the ORA is able to stop at the periodic flat regions such as the ones circled in the dashed line in Fig. 5, most of the AC calculation errors can be cancelled out.

There is another possible approach for ORA to stop the accumulation at the right point. The DUT's output is a combination of the sinusoidal waveforms at four frequencies. For spectrum analysis at each frequency, the accumulation should be stopped at the IMPs of this frequency to remove the AC calculation errors associated with it. Thus, if the accumulation can be stopped at the place where both of the upper-band frequency pair (f_2 and $2f_2\text{-}f_1$) or lower-band pair (f_1 and $2f_1\text{-}f_2$) could reach their own IMPs, the ORA should be able to achieve a very accurate result.

IV. Experimental Results

Although it is possible to obtain accurate measurement results by having a free-running accumulation which is long enough to minimize errors, the elongated test time, especially for IP3 measurement, is undesirable. Therefore, techniques are proposed for the BIST architecture in Fig. 1 to make the ORA stop at IMP points so that the test time can be greatly reduced.

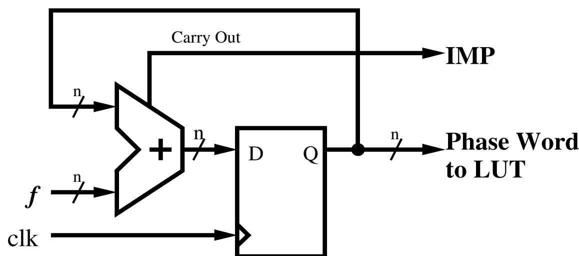

Fig. 6. Proposed IMP Circuit for Frequency Response Measurement.

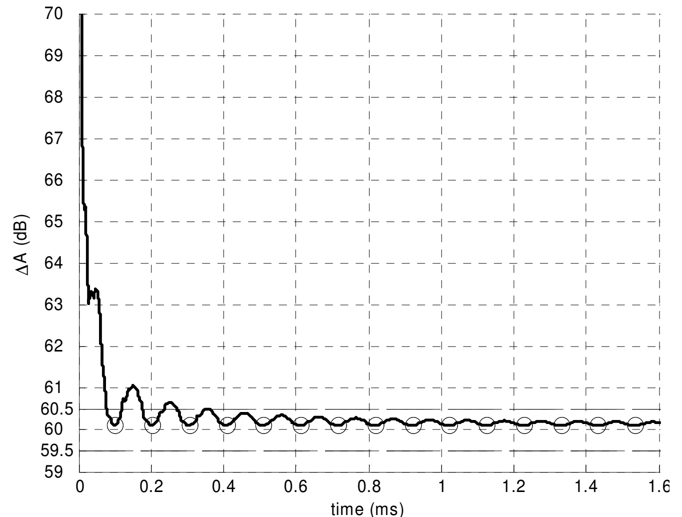

Fig. 7. Simulated ΔA versus Time

A. Test Time for Frequency Response Measurement

According to the analysis given in Section III-A, we know that the AC calculation errors can be removed if the ORA stops the accumulation at the IMP points of the frequency being measured. Therefore, the circuit shown in Fig. 6 is proposed to indicate when the ORA reaches an IMP point in the frequency response measurement and its IMP port will output a logic 1 at the appropriate point in time where the ORA should stop accumulation. Since this is actually the same function as the phase accumulator, there is no need to implement this additional circuit except for the addition of the carry-out bit from of the phase accumulator.

The proposed IMP circuit was simulated for its performance. In the simulation, the ORA was used to measure two DUT output magnitude responses at 10 kHz, one of which is 60 dB higher than the other one. In order to accurately differentiate these two responses, the difference between two measured $A(f)$'s, ΔA, should be fall between a tolerance band centered about 60 dB. The curve in Fig. 7 illustrates relationship of ΔA with respect to test time and the circled points represent the IMP points as indicated by the proposed circuit. According to the figure, the ORA can stop the accumulation at the first IMP point for a given measurement tolerance of +/-0.5 dB while the free-running strategy requires at least 3 times longer in terms of test time. The simulation also shows that this first IMP point relationship works perfectly for the frequencies up to almost half of the BIST clock frequency.

B. Test Time for IP3 Measurement

According to Section III-A, there are three possible ways to stop the accumulation in an IP3 measurement. The first is the free-running strategy. The second is the Δf-IMP strategy, which stops the accumulation at the IMPs of $1/\Delta f$ and can be accomplished with the circuit proposed in Fig. 8. The third is the single-side band IMP (SSB-IMP) strategy, which stops the accumulation at the IMP of either the upper-band frequency pair or lower-band pair and can be realized with the circuit

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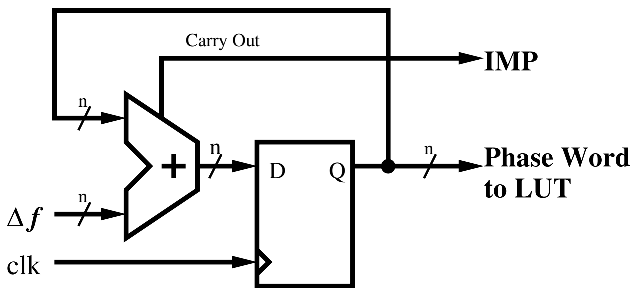

Fig. 8. Proposed Δ*f*-IMP Circuit for IP3 Measurement

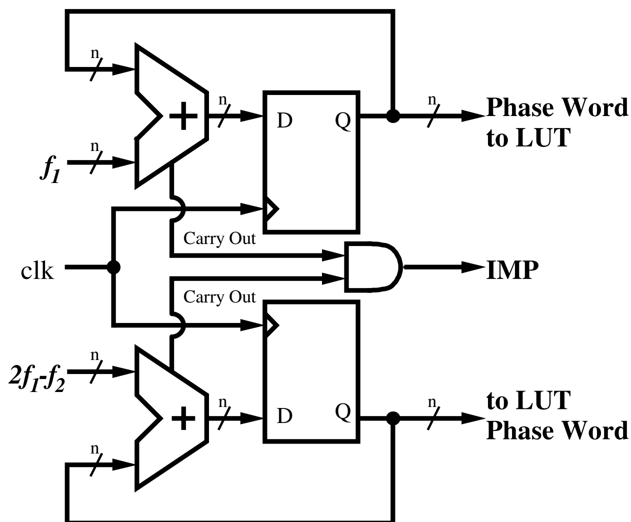

Fig. 9. SSB-IMP Circuit for IP3 Measurement

proposed in Fig. 9. Since the frequency word of the NCO_3 is set as $2f_1$-f_2, the SSB-IMP circuit can use the two accumulators from the existing phase accumulators in the TPG. Therefore, the hardware overhead of the SSB-IMP circuit is lower than the Δ*f*-IMP circuit even although the SSB-IMP one requires two accumulators.

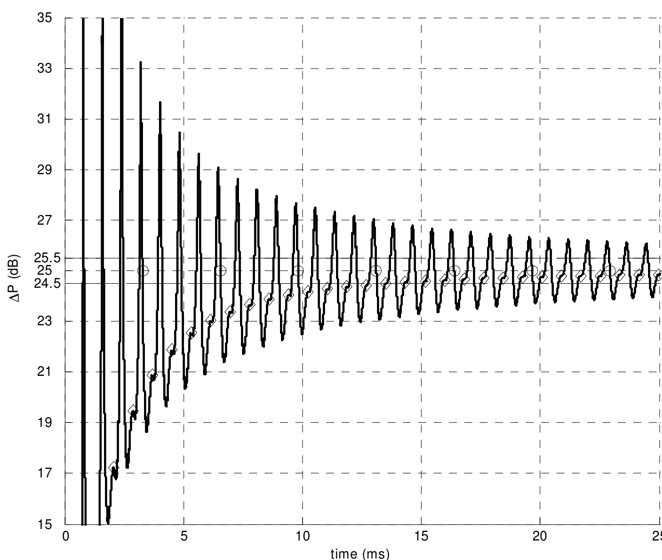

Fig. 10. Simulated ΔP Versus Time

The two proposed IMP circuits were simulated to determine their performance. In the simulation, the ORA was used to perform an IP3 measurement, where f_1, f_2, and ΔP are equal to 19.2_kHz, 22.4_kHz, and 25_dB, respectively. The curve in Fig. 10 illustrates relationship of ΔP with respect to the test time. The Δ*f*-IMP and SSB-IMP points picked by the two proposed circuits are indicated in diamond and round markers, respectively.

From the figure, it can be seen that the envelope of the curve drops fast at the beginning and then starts to flat out, which makes it very slow to converge into the tolerance band. The simulation also shows that the situation becomes even worse for larger ΔP. Therefore, the free-running strategy is very inefficient in term of total test time. The captured Δ*f*-IMP points basically follow the trend of the curve's envelope. But since they fall right at the flat regions between the peak and valley of the waveform, it enters into the tolerance band much faster than the free-running strategy such that the efficiency of the test time can be improved. However, the Δ*f*-IMP approach only works under the assumption of the same phase delay for the four frequencies; otherwise the moment of the first flat region varies, although the period remains as 1/Δ*f*. On the other hand, the SSB-IMP circuit does not have this issue and is able to identify the points where the measured values closely match to the expected result. This makes the required test time for IP3 measurement even shorter. However, this approach becomes unstable when the frequency of f_1 and f_2 reaches 1/10 of the clock frequency.

Conclusions

According to the theoretical analysis and simulation results presented, the MAC-based ORA must be able to stop the accumulation at the IMP points such that test time required by the BIST architecture can be shortened to increase its efficiency. Three IMP circuits are proposed for such a purpose. Using these circuits, the ORA is able to stop accumulation at the correct IMP points for measurements of frequency response and IP3 which makes the measurement results enter into the desired tolerance band much faster than any other approach.

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