A Fully Integrated Broadband Direct-Conversion Receiver RFIC for Satellite Tuner

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Abstract — This paper presents the circuit design and measured performance of a wideband receiver for direct conversion satellite tuner. The tuner RFIC is composed of a wideband front-end, a baseband low pass filter with on-chip automatic tuning circuit and a full integrated fractional-N synthesizer. A DC offset cancellation loop is also integrated without the use of external capacitors. The chip draws 140mA current from a 3.3V power supply. It achieves a sensitivity of -78dBm for 3/4 coding QPSK signal with 28.8MS/s symbol rate and 6.9dB C/IN. It is fabricated in a 0.35-μm SiGe BiCMOS technology and occupies a silicon area of 3.1mm².

Index Terms — direct conversion, satellite tuner, broadband, automatic tuning, fractional-N synthesizer, SiGe BiCMOS.

I. INTRODUCTION

With the ever-increasing demands of the digital multimedia applications market recently years, more and more interest is focused on digital TV, which may eventually take the place of its analog counterpart in the future. Satellite network, along with cable network and terrestrial network, is considered as one of the effect ways to deliver digital TV programs. The available digital satellite television standards include European standard DVB-S/S2, North American ATSC and Japanese ISDB-S. Recently China has developed its own satellite standard ABS-S. Among all these standards, DVB-S is the most popular in the world. In the DVB-S downlink, the low noise block (LNB) down-converts translate RF satellite signals from the Ku-band (10.7-12.75GHz) to L-band (950-2150MHz). This signal is then sent to a satellite TV set-top box through a coaxial cable, where tuner performs the final down conversion to baseband signal.

The paper describes a single-chip satellite tuner receiver which supports the DVB-S and ABS-S standards. It is organized as follows: Section II discusses the architecture of the satellite tuner. The implementation details are presented in Section III. Section IV presents the measured results and Section V is the conclusion.

II. OVERVIEW OF THE ARCHITECTURE

The system block diagram of the receiver is shown in Fig. 1. Direct conversion architecture is chosen for its compact construction and amenable to monolithic integration. The tuner operates in frequency from 950MHz to 2150MHz. It has a fully integrated synthesizer and a receiver chain, including voltage-controlled oscillators, a wideband frontend and on-chip baseband filters. Device configuration is accomplished by I²C-bus. For the multi-tuner usage, such as watch & record or picture-in-picture function, the LNA has a loop through output. It has separate control bits and can operate with the remainder of the device in power-down mode.

In contrast to the narrow-band wireless receiver, satellite tuner must receive RF carriers spanning more than 1GHz bandwidth. This makes the design become more challenge in two aspects: 1. Because of multiple channels at similar power levels, broadband LNA with stringent linearity should be realized to avoid in-band intermodulation products; 2. Implementation of wideband precise quadrature local oscillator signal generation with low phase noise, low LO emission and small silicon area.

Due to the gain variation of up-to-date LNBs, cable losses and weather conditions, the variation of the input signal level is usually larger than 65dB. Such a wide dynamic range requires the VGA with sufficient controllable gain. PVT compensation circuit and dB linearization circuit are used to achieve simple and accurate RSSI estimation.

Since the system channel date varies from 1 to 45MSps, the cutoff frequency of the channel selection LPF should be programmable to cut off the closely spaced unwanted neighbor channel interferences. An automatic tuning system is needed to maintain the precise filtering characteristics against process variation, temperature drift and aging.

As the IC uses direct conversion architecture, DC offset cancellation (DCOC) circuit is applied to keep the baseband stages from saturating. Considering the satellite tuner is a continuous-time system, DCOC is implemented by a low-pass filter placed in the feedback path, which causes high-pass filtering in the overall closed loop. The DCOC loop should have a very low corner frequency to avoid signal loss.
III. CIRCUIT BLOCK DESIGN

A. Broadband LNA

A simplified schematic of the proposed wideband LNA is depicted in Fig. 2. A cascode topology is utilized for improved frequency response and reverse isolation. The amplifier uses resistive load and shunt feedback to provide broadband operation. To enhance the linearity of the LNA, an improved distortion compensation technique is applied. Because the equivalent base–emitter DC resistance of Q3 decreases as the input RF voltage increases, the collector current of the transistor Q1 increases as the RF signal increase. It compensates the gain compression and the linearity is improved [1]. Unlike [1], simulation results show that small RO will result in over compensation. Thus a moderate RO of 1.4K Ohm is chosen in the design.

B. RF VGA & AGC

Current steering type VGA is chosen for its excellent linear gain in dB characteristic over a wide dynamic range. Its gain can be expressed by (1), where $g_m$ is the transconductance of the differential pair and $V_c$ is control voltage.

$$ G = g_m R \left( 1 + \exp \left( -\frac{V_c}{K} \right) \right)^{-1} \tag{1} $$

The VGA gain is highly temperature dependent and the characteristic is fairly linear-in-dB at high attenuations, but poor at high gains. When maximum gain is expected, compensation and linearization circuit is required, as shown in Fig. 3, where I1 is a PTAT type current and I2 is a constant current. Neglecting base current of Q3, the voltage $V_x$ can be written as (2), where $K$ is a constant independent of temperature. $V_x$ is proportion to absolute temperature, which cancels the factor $V_T$ in the denominator of (1).

$$ V_x = K_1 \frac{I_1}{I_2} \frac{I_{s1}}{I_{s2}} \frac{V_{AGC}}{2V_T} = K_1 V_{AGC} \tag{2} $$

The function of the rest circuit is dB linearization. Assuming transistors Q9 - Q12 have the same size and Q7, Q8 have the same size, output voltage $V_{ctrl}$ can be written as (3).

$$ V_{ctrl} = -V_T \ln \left( \exp (K V_{AGC}) - 1 \right) \tag{3} $$

If this voltage $V_{ctrl}$ is used as VGA control voltage $V_c$, from (1) and (3) we can get

$$ G(dB) = 8.7 K V_{AGC} + 20 \log_{10} \left( g_m R \right) \tag{4} $$

In this manner, linear gain in dB characteristic and temperature stabilization is achieved [2].

C. Quadrature Mixer

The quadrature mixer is formed by two Gilbert mixers with shared transconductance stages which improves image rejection ratio (IRR) by reducing phase error. Since linearity is of great concerned, more current is biased in the transconductor stage. Resistor degeneration is also used to further improve the linearity of the mixer. The switching quad transistors are sized so that they operate close to their peak $f_T$ at the bias current. The quadrature mixer, together with IF buffer and LO buffer, consumes about 20mA current [3].

D. Baseband Filter & DCOC

A 7th-order Butterworth leapfrog Gm-C filter topology is selected. The structure and component values of main filter are derived from the double terminated LC ladder LPF prototype by signal flow graph transformation. The resulted topology is drawn in Fig.4. Node scaling is performed by properly scale the individual Gm to optimize the dynamic range of the filter and to compensate for the inherent 6 dB loss of the LC prototype. The integrating capacitors are split as anti-parallel ones to keep the back-plate parasitic capacitances balance to the n/p signal lines. Values of the actual capacitors are modified by deducing that of CMFB compensating capacitors and the parasitic capacitances contributed by the Gm cells. The Gm cell used in the main filter is a modified multitanh doublet which has a signal capacity of 300mVppd for better than -40dB THD and preserves the translinear property of bipolar transistors [4]. As a result, Gm-C filter’s cutoff frequency, which is proportional to Gm/C, can be directly proportional to a control current and has a wide tuning range.
To guarantee accurate and stable filtering characteristic, an automatic frequency tuning system based on the master-slave scheme is designed with a matched current controlled filter (ICF) as the master. A phase locked loop (PLL) locks the pole frequency of the master to a reference clock signal. Since the Gm-C biquad ICF use the same Gm cell topology as the main filter, and the capacitors used in the ICF and those in the main filter can be matched very well, the control current of the biquad ICF can also be used to derive that of the main filter to maintain a stable main filter frequency response. The 7-bit linear current DAC is used for bandwidth programming. The output current of the DAC responding to the input digital bits is used to control the main filter; thus the cutoff frequency of the main filter can be programmed within the DAC's resolution.

The baseband VGA is digital controlled to facilitate the interface with the demodulator chip. To prevent propagation of DC offset due to LO leakage and device mismatches, a continuous DC cancellation loop operates around the baseband. The resulting high pass corner is sufficiently low to prevent signal degradation. To keep the cut-off frequency of the DCOC loop constant, a transconductor stage inversely proportional to baseband VGA is introduced.

E. VCO

The VCO frequency tuning range is targeting at 2.8GHz-4.35GHz. To save chip area, a single symmetric inductor together with a bank of switched capacitors composite the VCO tank. Two cross coupled NPN-transistors provide the negative Gm with a current consumption of 5.3mA. A commonly used capacitor switch is shown in Fig. 5(b). To minimize flicker noise contribution to phase noise, the size of the NMOS should be large enough, which, on the other hand, limits the available tuning range because of the added parasitic capacitance. This contradiction can be solved by using switches shown in Fig. 5(c). In each branch of switched capacitor path, a large NMOS can be completely turned off by a small inverter which isolates the coupling between the positive and negative sides of the tank. Simulation shows the turn-on resistance is less than 10 Ohm that should not greatly affect the resonator Q. The $K_{\text{VCO}}$ for each sub-band differs from 40MHz/V to 150MHz/V with the tuning range overlap about 30%-40%.

Although the tuning range overlap between adjacent sub-bands ensure the frequency continuity, it is possible that the frequency range will shift due to PVT variations. Therefore the measured frequency table under normal condition should be used as guidance rather than a precise control. In this work, an adaptive frequency calibration (AFC) mechanism is developed in case that the frequency tuning characteristics shift. A 3-bit analog-to-digital converter (ADC) is employed to monitor the $V_{\text{tune}}$ line with 000 represents lowest voltage around ground and 111 represents highest voltage around supply. When the AFC is activated, it samples $V_{\text{tune}}$ every count interval and judges the ADC output value. If this value stays at 000 for several counted cycles which is long enough for the PLL to pull in, the lower sub-band is selected.

On the other hand, if ADC output stays at 111, the upper sub-band will be selected. Otherwise the present sub-band is appropriate to lock in. The calibration procedure stands on the base of adjacent sub-band auto-selection if the VCO frequency shifts a little, so only one or two calibrating iterations are needed. With the wide loop bandwidth, AFC settling time is measured to be about 21μs.

F. PLL

To extend frequency range while keeping small $K_{\text{VCO}}$, we propose a digital split-tuned LC-VCOS architecture. The concept is to coarsely tune the VCO with bank of switched capacitors, while finely tune it with varactors. An automatic frequency searching algorithm is needed to select appropriate sub-band that can bring the PLL to lock under PVT variations. Thus, wide tuning range and low $K_{\text{VCO}}$ can be simultaneously achieved.

To generate I/Q quadrature LO carrier, the VCO output frequency can be divided by an even number. To maintain a continuously tuned frequency range, say 500MHz-2GHz, a divide-by-2/4 scheme requires a VCO with 2GHz-4GHz tuning range, which is beyond what a single inductor VCO can deliver due to the quality factor degradation over that wide range. To ease the design difficulty of the VCO (2.8GHz-4.35GHz), we develop a flexible frequency plan through a programmable division ratio of 2/3/4 that allows an overall frequency range of 700MHz-2.15GHz. The quadrature phase requirement for I/Q signal in divide-by-3 mode is achieved by utilizing a 3rd-order polyphase filter [5].

An integer-N frequency synthesizer would suffer high in-band phase noise because of a large division ratio. To improve the overall RMS phase noise performance, narrow loop bandwidth would be necessary which in turn slows down the PLL settling time. A fractional-N approach used in this design is preferred because it achieves low in-band noise and fast settling simultaneously. The fast switching digital gates in $\Sigma\Delta$ Modulator induce very large current spikes in supply line which could harm sensitive analog blocks such as VCO. A LDO is involved to suppress the digital noise on supply line.
IV. MEASURED RESULTS

The whole chip has been fabricated in a 0.35-μm SiGe BiCMOS process. It features four metal layers, a 43 GHz fT high performance NPN transistor and dual metal–insulator–metal (MIM) capacitors (4.1fF/μm²). A die photograph is shown in Fig. 6. It occupies a total die area of 3.1mm². The chip is assembled in a 28-pin QFN package. The receiver performance is tested with a baseband QPSK demodulator chip. For 3/4 coding QPSK signal with 28.8MS/s symbol rate and 6.9dB C/N, -78dBm sensitivity could be achieved.

Fig. 7 plots the normalized receiver voltage gain versus AGC control voltage. The RF input and LO frequencies are set at 1095MHz and 1090MHz respectively. The 3dB corner frequency of baseband filter is set at 10MHz. Four groups of data are measured at the temperature of 0°C, 25°C, 50°C and 85°C. It shows a high dynamic range over 70 dB with fair well linear gain-control characteristic except for the extremely low gain condition. Fig. 8 shows the measured filter frequency response. Combined the coarse and fine tuning bits, the filter’s cut off frequency can be tuned from about 3.98MHz to 39.6MHz. Fig. 9 gives the measured phase noise for channels that require the fractional-N mode. Table I summarizes the characterization results of the integrated tuner chip.

**TABLE I**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Measured results</th>
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<tbody>
<tr>
<td>Frequency Range</td>
<td>950MHz to 2150MHz</td>
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<tr>
<td>Power consumption</td>
<td>140mA (3.3V)</td>
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<tr>
<td>S11</td>
<td>&lt;-12dB</td>
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<tr>
<td>Noise Figure (DSB)</td>
<td>6dB @ Max. gain</td>
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<tr>
<td>IIP3</td>
<td>5dB @ -30dBm input</td>
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<tr>
<td>AGC Control Range</td>
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<tr>
<td>Filters Bandwidth</td>
<td>4M to 39M</td>
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<tr>
<td>LO Emission</td>
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<tr>
<td>DC Offset Voltage</td>
<td>&lt;50mV</td>
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<tr>
<td>Phase noise (E₀=1090MHz)</td>
<td>-99 dBc/Hz @10K</td>
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<td></td>
<td>-92 dBc/Hz @100K</td>
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REFERENCES


