IEEE 2009 Custom Integrated Circuits Conference (CICC)

A 430MHz-2.15GHz Fractional-N Frequency Synthesizer for DVB and ABS-S Applications

Peng Yu, Zheng Gong, Ming Gu, Yin Shi
Suzhou-CAS Semiconductors Integrated-Technology Research Center
Suzhou, Jiangsu, 215021, P.R.China

Fa Foster Dai
Department of Electrical Computer Engineering
Auburn University
Auburn, Alabama, 36849-5201, USA

Abstract - A 430MHz-2.15GHz wideband fractional-N frequency synthesizer RFIC for digital video broadcasting (DVB) and advanced broadcasting system-satellite (ABS-S) application is presented. A voltage controlled oscillator (VCO) with single inductor is coarsely tuned by banks of switched-capacitors and finely tuned by varactors to achieve both large frequency tuning range and limited VCO gain. A fast settling low dropout regulator (LDO) is employed to suppress the digital noise on supply line induced by the ΣΔ modulator. A divid-by-3 VCO divider is designed based on a 3rd-order polyphase filter to generate the quadrature local oscillator (LO) carriers. This PLL is fabricated in a 0.35µm SiGe BiCMOS technology. Measured result shows that the in-band phase noise is less than -96dBc/Hz and the integrated RMS phase error is less than 1°.

I. INTRODUCTION

Phase locked loop (PLL) is a key building block in modern digital TV tuner. The design of the PLL becomes more and more challenge due to the conflicting requirements of large frequency range, low phase noise, low spur level, fast settling time and low power consumption. Furthermore, consumer market need for multi-standard single chip receiver solutions. Satisfactory functionality and performance over process, voltage and temperature (PVT) variations have become ever challenging for integration of multi-standard DVB applications, such as DVB-T, DVB-S, DVB-S2 and ABS-S.

In this paper, we present a multi-standard fractional-N PLL that covers a very wide frequency band from 430MHz to 2.15GHz with low phase noise for digital video broadcasting (DVB) and advanced broadcasting system-satellite (ABS-S) applications. Fig. 1 illustrates the architecture of the PLL with wide tuning range and high performance. A digital plus analog tuned voltage controlled oscillator (VCO) with single inductor is introduced followed by a quadrature local oscillator (LO) carrier generator which is capable to provide division ratios of 2, 3, 4, 6 and 8. An adaptive frequency calibration (AFC) mechanism is adopted to calibrate frequency over PVT variations. A hybrid multi-modulus divider (MMD) consists of current mode logic (CML) and CMOS dividers is proposed along with an integrated ΣΔ modulator for noise shaping. A fast settling low dropout regulator (LDO) protects the supply line by suppressing in-band random noise caused by the fractional-N operation. To increase the loop in-band performance a fast reset phase frequency detector (PFD) is employed along with the current programmable charge pump (CP) which can be used to optimize the loop bandwidth to achieve fast settling and low phase noise. Measured result shows that the worst case in-band phase noise is less than -96dBc/Hz with a loop bandwidth of about 200 KHz and the phase noise at 1MHz offset is less than -110dBc/Hz.

This paper is organized as follows. In Section II, frequency synthesizer architectures for wide tuning range with low phase noise are compared. PLL building block circuit designs are discussed in Section III, and the measurement results are summarized in Section IV.

II. PLL ARCHITECTURE

There are various approaches of VCO architectures that can achieve wide tuning range. The traditional one is to design VCO with control voltage (V_{tune}) swing as large as possible. This scheme results in two problems. First, with the limited supply voltage, high gain VCO has to be used to obtain wide tuning range. However, large VCO gain (K_{VCO}) increases the control voltage sensitivity to both random and deterministic noise. It’s also difficult to design large V_{tune} swing due to the limited headroom at the output of the charge pump. An error amplifier could be added to the CP to alleviate the current matching issue but it worsens the in-band noise performance [1].

It is also feasible to stack inductors with different outer dimension vertically and activate one of these resonators by switching its Gm stage [2]. The advantage of such approach is the absence of switches with low loss in the resonator path. However, the coupled inductors and their resonators occupy extra chip area.

To extend frequency range while keeping small $K_{VCO}$, we propose a digital split-tuned LC-VCOs architecture. The concept is to coarsely tune the VCO with bank of switched capacitors, while finely tune it with varactors. An automatic frequency searching algorithm is needed to select appropriate sub-band that can bring the PLL to lock under
PVT variations. Thus, wide tuning range and low $K_{\text{VCO}}$ can be simultaneously achieved.

To generate I/Q quadrature LO carrier for down-conversion mixers, the VCO output frequency can be divided by an even number, such as divide-by-2 or divide-by-4. To maintain a continuously tuned frequency range, say 500MHz-2GHz, a divide-by-2/4 scheme requires a VCO with 2GHz-4GHz tuning range, which is beyond what a single inductor VCO can deliver due to the quality factor (Q) degradation over that wide range. To ease the design difficulty of the VCO (2.8GHz-4.35GHz), we develop a flexible frequency plan through a programmable division ratio of 2/3/4/6/8 that allows an overall frequency range of 430MHz-2.15GHz. The quadrature phase requirement for I/Q signal in divide-by-3 mode is achieved by utilizing a 3rd-order polyphase filter [3].

A traditional integer-N frequency synthesizer would suffer high in-band phase noise because of a large division ratio. To improve the overall RMS phase noise performance, narrow loop bandwidth would be necessary which in turn slows down the PLL settling time. The fractional-N approach in this design is preferred because it achieves low in-band noise and fast settling simultaneously.

III. CIRCUIT DESIGNS

A. VCO Circuits

The VCO frequency tuning range is targeting at 2.8GHz-4.35GHz. To save chip area, a single symmetric inductor together with a bank of switched capacitors composite the VCO tank. Two cross coupled NPN-transistors provide the negative $g_m$ with a current consumption of 5.3mA. A commonly used capacitor switch is shown in Fig. 2 (b). To minimize flicker noise contribution to phase noise, the size of the NMOS should be large enough, which, on the other hand, limits the available tuning range because of the added parasitic capacitance. This contradiction can be solved by using switches shown in Fig. 2 (c). In each branch of switched capacitor path, a large NMOS can be completely turned off by a small inverter which isolates the coupling between the positive and negative sides of the tank. Simulation shows the turn-on resistance is less than 10 Ohm that should not greatly affect the resonator $Q$. The $K_{\text{VCO}}$ for each sub-band differs from 40MHz/V to 150MHz/V with the tuning range overlap about 30%-40%.

Although the tuning range overlap between adjacent sub-bands ensure the frequency continuity, it is possible that the frequency range will shift due to PVT variations. Therefore the measured frequency table under normal condition should be used as guidance rather than a precise control. In this work, an adaptive frequency calibration (AFC) mechanism is developed in case that the frequency tuning characteristics shift. A 3-bit analog-to-digital converter (ADC) is employed to monitor the $V_{\text{tune}}$ line with 000 represents lowest voltage around ground and 111 represents highest voltage around supply. When the AFC is activated, it samples $V_{\text{tune}}$ every preset interval and judges the ADC output value. If this value stays at 000 for several counted cycles which is long enough for the PLL to pull in, the lower sub-band is selected.

On the other hand, if ADC output stays at 111, the upper sub-band will be selected. Otherwise the present sub-band is appropriate to lock in. The calibration procedure stands on the base of adjacent sub-band auto-selection if the VCO frequency shifts a little, so only one or two calibrating iterations are needed. With the wide loop bandwidth, AFC settling time is measured to be about 21µs.

B. LO Generator

In this design, there is a gap of tuning range between VCO frequency divide-by-2 and divide-by-4 that has to be filled up with divide-by-3. A Johnson counter divide-by-3 circuit with 50% duty-cycle output is used. The output of divide-by-3 is then fed to a 3rd-order polyphase filter to generate quadrature LO carrier (I/Q) as shown in Fig. 3. Note that by choosing three poles carefully, the flatness of magnitude response of the filter over 2.8GHz-4.35GHz can be guaranteed, which leads to a phase mismatch between I/Q being less than 1°. The polyphase filter does not degrade the phase noise performance since the resistors are small. To spread the frequency further down to 430MHz, divide-by-6 and divide-by-8 modes are realized by combining $\text{div}3*\text{div}2$ and $\text{div}2*\text{div}4$ respectively. The divider block is implemented using CML circuitry.

C. MMD

Compared with the NPN device in the 0.35µm technology, the MOSFET devices show disadvantage in terms of operation speed. While the CML circuit can work at several GHz, the CMOS logic circuit can only run under 300MHz. On the other hand the CML circuit consumes more current than CMOS. To utilize the advantages of both approaches, a hybrid MMD built up with CML and CMOS is developed to provide desired speed capability and to save current. Each stage of MMD consists of D-latches and AND-gates. In this work, a novel D-Latch with integrated AND operation is proposed. There already is traditional D-Latch with the same function as shown in Fig. 4 (a). The limited headroom in 3.3V supply voltage prevents the D-Latch in Fig. 4 (a) being used. We can reconstruct the D-Latch by relocating $Q_a$ and $Q_b$ from vertical to horizontal and save a $V_{BE}$ headroom as

Fig.2 (a) VCO Architecture, (b) Conventional switch with large parallel parasitic capacitance $C_p$, (c) Proposed switch with small size inverters to isolate parasitic coupling

Fig.4 (a) D-Latch, (b) Proposed MMD, (c) Traditional MMD
shown in Fig. 4 (b). When \( A_p \) and \( B_p \) are both high, \( I_N \) is larger than \( I_P \), and therefore, \( V_P \) is larger than \( V_N \). Notice that \( I_{\text{rise}} - I_{\text{fall}} \) decreases as \( R_E \) increases, so the value of \( R_E \) should be small. When either \( A_p \) or \( B_p \) is high, \( I_P - I_N \) increases as \( R_E \) increases. So \( R_E \) should be large to keep the difference between \( V_P \) and \( V_N \) large. This contradiction indicates that the value of \( R_E \) should be chosen carefully to meet requirements on both conditions. Fig. 5 shows the transient simulation result of the proposed D-Latch. The CMOS dividers working at low frequency provide a large range of division ratio.

D. ΣΔ Modulator and Regulator

A 3rd-order multi stage noise shaping (MASH) ΣΔ modulator has better in-band noise shaping effect compared to 3rd-order single stage feedforward (SSMF) structure, while MASH brings in more quantization noise out-of-band. Moreover, MASH has a wider spread output bit pattern that tends to increase the CP turn-on time making \( V_{\text{tune}} \) more sensitive to noise of substrate and injected current [4][5]. Consequently, the SSMF approach is a more suitable candidate than MASH.

The fast switching digital gates in ΣΔ Modulator induce very large current spikes in supply line which could harm other sensitive analog blocks like VCO and CP. A LDO is involved to suppress the digital noise on supply line. The LDO regulator with adaptively biased regulation scheme [6] was used to form a fast regulation loop and minimize the output voltage variation due to rapid and large load changes. When the load current is switched between 0mA and 30mA with rise and fall times of 10ns, the total output voltage variation is less than 6mV (0.2%\text{pp}) given \( V_{\text{out,nominal}} \) is 2.93V and the response time \( T_r \) [7] is 196ns.

E. PFD and CP

The characteristics of PFD and CP influence the PLL in-band noise dramatically. The reset time of the PFD should be short enough to cut off the current in CP from injecting into the loop filter. In this work, a TSPC DFF based PFD is utilized and simulation result indicates the reset time is 200ps.

As mentioned above, the \( K_{\text{VCO}} \) varies from 40MHz/V to 150MHz/V. Therefore to keep loop bandwidth constant, the source and sink current of charge pump is programmable in order to compensate the \( K_{\text{VCO}} \) variation.

IV. MEASUREMENT RESULTS

Fig. 6 shows the phase noise performance over 450MHz-2150MHz of the proposed frequency synthesizer. The worst case in-band PN@10kHz is -96dBc/Hz and RMS phase error is less than 1°. It can be seen that the RMS error roughly follows the in-band phase noise.

Fig. 7 and Fig. 8 give the measured phase noise for channels that require the fractional-N mode and integer-N mode, respectively. The in-band and out-of-band phase noise degrade in fractional-N mode due to the digital induced noise of ΣΔ modulator. The phase noise performance also degrades as division ratio increases in integer-N mode. Fig. 9 denotes the fractional spur at 1.09GHz is -56dBc @ 3.72 MHz offset.

Fig. 10 shows the variation of \( V_{\text{tune}} \) when a frequency change is demanded. The AFC is activated to choose a more suitable sub-band of the VCO with higher frequency. It can be seen that the \( V_{\text{tune}} \) first rose on the previous sub-band to search the frequency required until it hit the supply voltage. Then the sub-band was altered so the \( V_{\text{tune}} \) fell sharply and performed another searching on the new sub-band. The AFC phase took about 21μs, while the PLL phase took about 19μs.

Fig. 11 shows the die paragraph of the wide tuning frequency synthesizer RFIC with an area of 1.15 mm².

Summarized measurement results are given in Table I.
TABLE I. MEASURED PERFORMANCE SUMMARY

<table>
<thead>
<tr>
<th>Process</th>
<th>0.35µm SiGe BiCMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>3.3V (ΣΔ Modulator with 2.9V)</td>
</tr>
<tr>
<td>Current Consumption</td>
<td>50mA–60mA</td>
</tr>
<tr>
<td>Occupied Area</td>
<td>1.15 mm</td>
</tr>
<tr>
<td>Continuous Tuning Range</td>
<td>430MHz-2.15GHz (single inductor)</td>
</tr>
<tr>
<td>Reference Clock</td>
<td>27MHz</td>
</tr>
<tr>
<td>Loop Bandwidth</td>
<td>Programmable, nominal~200KHz</td>
</tr>
<tr>
<td>In-band Phase Noise</td>
<td>&lt;-96dBc/Hz @10kHz offset</td>
</tr>
<tr>
<td>Fractional Spur</td>
<td>&lt;-56dBc</td>
</tr>
<tr>
<td>Integrated RMS Phase Error</td>
<td>&lt;1°</td>
</tr>
<tr>
<td>Locking Time</td>
<td>~40μs (including AFC time)</td>
</tr>
</tbody>
</table>

V. CONCLUSIONS

We presented a fully integrated multi-band frequency synthesizer IC that covers a very wide frequency range with an overall tuning range of 131% using only one on-chip inductor. The PLL chip occupies only 1.15 mm\(^2\) die size in a 0.35µm SiGe technology. The AFC helps with the VCO sub-band selection against the PVT variations. The LDO suppresses the in-band and out-of-band noise generated by 3\(^{rd}\)-order ΣΔ modulator. The wide tuning range, fast settling time and low phase noise make the PLL IC suitable for numerous multi-band, multi-standard applications such as DVB and ABS-S.

REFERENCES