An 8 – 18 GHz Wideband SiGe BiCMOS Low Noise Amplifier

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***Abstract* — In this paper, an 8 – 18 GHz wideband low noise amplifier (LNA) with an active balun fabricated in a 0.13-μm SiGe BiCMOS technology was presented. The LNA achieves 16-dB of gain with 1.5 dB variation over the 8GHz to 18 GHz frequency band and a matched input with less than -9 dB of reflection. The minimum noise figure (NF) is 5 dB at 8GHz and increases to 6 dB at 18GHz. The measured IIP3 is -15-dBm with 17 mA total current consumption from 2.2V supply.**

***Index Terms* — Low noise amplifier, resistive feedback, wideband, SiGe, BiCMOS, linearity, X-band, Ku-band, active balun.**

I. Introduction

The development of modern radar, software defined radio and wireless applications necessitate next generation receivers with wideband frequency range. The 8 to 18 GHz frequency band is used by many radar and commercial communication systems such as X-band and Ku-band radars and software-defined radios [1]. The low noise amplifier (LNA) is one of the most critical building blocks in wideband transceiver designs since its NF, gain and linearity contribute significantly to the overall system performance.

The traditional cascode LNA with inductive degeneration shows low noise and good gain performance compared to other architectures, but it can only be matched in a narrow band. Recently, other millimeter wave LNA designs have employed an on-chip LC-ladder matching filter at the input of the LNA to broaden the bandwidth [2] [3]. However, this type of the LNA has several disadvantages, including enlarged die size, and worse noise figure due to the extra noise contributed by lossy on-chip inductors present in the LC filter network. On the other hand, distributed amplifiers can achieve the widest bandwidth, but their noise figure is typically large [4] [5]. The same problem exists in common-base LNAs [6].

Recently, silicon-germanium (SiGe) heterojunction bipolar transistor (HBT) technology, which utilizes bandgap engineering to improve transistor performance while maintaining compatibility with low cost, high integration CMOS manufacturing, attracts more and more attention in IC design. The wideband LNA present in this paper is implemented in a commercial SiGe HBT BiCMOS technology featuring with a 0.13 μm lithography, a peak cutoff frequency (f_T) of 200 GHz and a maximum oscillation frequency ($f_{\max}$) of 250 GHz.

This paper demonstrates the design of a wide-band LNA, which covers the entire X-band (8-12 GHz) and Ku-band (12-18 GHz). The LNA achieves 16dB gain, 5dB noise figure, and -15 dBm IIP3 over the entire X- and Ku-band. The LNA dissipates less than 38-mW power with a 2.2-V power supply.

II. Wideband LNA Design

In the design of wideband LNAs in modern receivers, there are several considerations including low NF of the amplifier, reasonable gain with sufficient linearity, a stable 50-Ω input impedance matching, and low power consumption, which is needed for portable systems. Satisfying all of the design goals for the wideband LNA over X-band and Ku-band is particularly difficult, because of the high operating frequency and the broad bandwidth compared to conventional LNAs. A few existing topologies can provide the flat gain over a wideband, as mentioned above [2-6]. However, achieving low noise over such wide band is not easy, especially at high operation frequency. Normally, the noise performance of a device at a certain bias condition degrades as frequency increase. Thus, the wideband topology must provide good input noise and power matching over the entire operating frequency range and sufficient gain at high frequency to compensate the degradation of the noise and gain as frequency increases.

Compared to other wideband LNA topologies, shunt feedback topology is a good candidate for its easy wideband input matching, smaller chip size and insensitivity to process variations with the use of precision resistors [7][8]. Although the feedback technique would degrade the noise figure for input matching and consume large amount of current, especially in the CMOS to achieve desired gain. However, the SiGe HBT offers the advantages of excellent noise performance and an improved transconductance over the CMOS devices. These major advantages could be employed to overcome the limitations of the shunt feedback topology. In the proposed LNA, the shunt feedback topology using SiGe HBTs, in conjunction with inductive compensation topology is chosen to achieve wideband input impedance matching with low NF and low power.

A simplified schematic of the proposed wideband LNA, which consists of three stages, is shown in Fig.1. The input stage of the LNA is a single-ended cascode amplifier to achieve simultaneous power and noise matching over the wide bandwidth. Three different feedback paths are provided in our design to achieve simultaneous noise and power matching: emitter degeneration feedback R_{e1}, local shunt feedback R_{f1} and global shunt feedback R_{f2}, as shown in Fig.1. Due to the

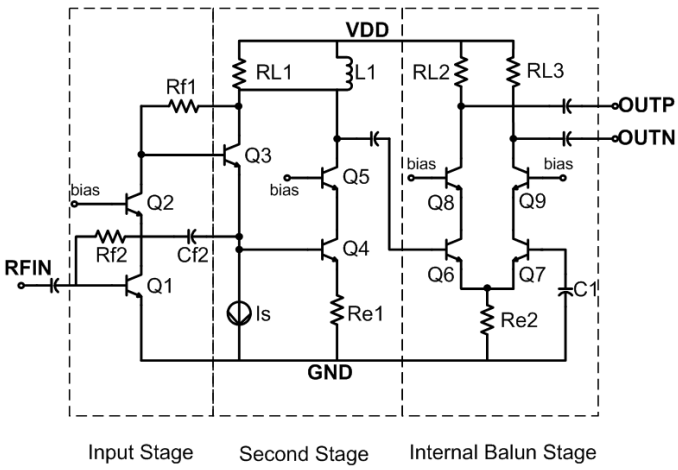

Fig. 1. Simplified schematic of the wideband LNA.

additional noise components of following stages, it becomes increasingly necessary to mitigate the noise effects of the input stage. Feedback resistor R_{f2} is the main component which not only determined the input impedance but also the overall noise figure of the amplifier. Neglecting the noise contribution of the following stages and the shot noise from the base and collector of Q1, the noise figure of the amplifier can be expressed as: [9]

$$NF = 1 + \frac{R_{EQ1}}{R_S} + \frac{R_S \times R_{EQ1}}{R_{f2}^2} \tag{1}$$

$$R_{EQ1} = r_{b1} + \frac{1}{2g_{m1}} \tag{2}$$

where R_S represents the source impedance and r_{b1} and g_{m1} represent the base resistance and transconductance of transistor Q1, respectively.

With this type of amplifier, it is advantageous to feedback to the input from the emitter of Q3 instead of the collector of Q2. It will provide some inductance to the input, which tends to make for a better match. With feedback, the input impedance of the amplifier is given by:

$$Z_{in} = \frac{R_{f2}}{1 + g_{m1}\left(R_{f1} + Z_{L1}\right) + \dfrac{R_{f2}}{Z_\pi}} \approx \frac{R_{f2}}{g_{m1}\left(R_{f1} + Z_{L1}\right)} \tag{3}$$

where Z_{L1} represents the parallel combination of $R_{L1}$and load inductor L1. Compared to the total impedance of R_{f1} plus Z_{L1}, the variation of Z_{L1} with frequency is very small. As equation (3) shown, both R_{f1} and R_{f2} play important roles for the input impedance. So input matching can be achieved by carefully choosing the value of those two feedback resistances.

The overall voltage gain of the amplifier is given by

$$A_V = \frac{g_{m6} \times Z_L \times \left(R_{L2} \| R_L\right)}{\left(R_S + Z_{IN}\right)} \times A_I \tag{4}$$

where g_{m6} represents the transconductance of Q6, R_L represents the external load of the amplifier and A_I is the overall current gain. The overall gain should be flat over the entire passband. Since the output current from the transistor rolls off inversely with frequency, the inductive load can equalize the voltage gain to a constant value across the passband. Then the bandwidth at high frequency can be widened. On the other hand, load inductor also helps reduce the DC current through R_{L1} to provide sufficient headroom. In addition, the parasitic capacitance around the inductor should be minimized to ensure self resonance beyond the operation frequency.

The second stage is combination of common-collector amplifier and cascode amplifier, which is very similar to common-collector-common-emitter configuration. With this configuration, current gain and input resistance of the basic transistor can be increased. With boosted current gain, the base shot noise of the second stage can be dramatically reduced. Then the overall noise figure of the wideband LNA can be improved.

The differential cascode architecture in the output stage operates as an internal balun, which transforms the single-ended signal to differential. As we known, the loss in the external balun, will directly suffer the noise performance of the whole receiver. Building an internal balun will greatly help reduce the noise figure of the receiver. A simplified schematic of internal balun stage is shown in Fig.2, where the collector-emitter currents (I_{ce6} and I_{ce7}) are labeled. Since resistor R_{e2}, can reject the common-mode signal, we are able to inhibit current flow between the emitters of transistor Q6 and Q7. Thus, AC current was forced to flow through Q6 and also Q7, thereby creating a roughly 180° phase shift in the differential paths. As the two branches are under the same bias conditions with the same AC current flow, roughly identical output amplitudes will be achieved.

Careful consideration during layout is important to ensure minimal parasitic through the amplifier. The internal balun stage was oriented symmetrically about the horizontal axis. And banks of decoupling capacitors were located at the termination of DC bias (like base of Q8) and power to filter out the noise from the reference.

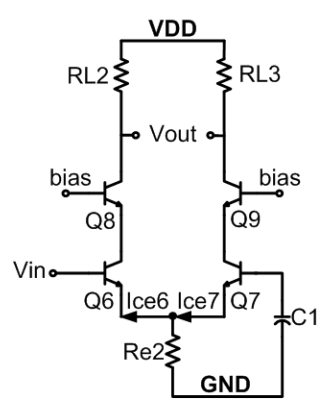

Fig. 2. Simplified schematic of internal balun stage

III. MEASUREMENT RESULTS

The wideband LNA was implemented in a commercially-available 0.13 μm 200-GHz f_T SiGe HBT BiCMOS technology, with a core size of 0.1 mm^2. The LNA characteristics were measured on wafer using Cascade Microtech wafer probes. The probes were used with an Agilent 8510C network analyzer and an N8975A NF analyzer to measure the small signal S-parameters and NF over the operating frequency range.

A. Direct current (DC) analysis

The measured result shows that, the total DC power consumption is 38mW with 2.2V voltage supply.

B. S parameter analysis

S-parameters are tested to verify the gain, isolation and input matching. As shown in Fig.2, the typical S21 is 16 dB with 3dB bandwidth from 8 GHz to 18 GHz. The S21 reaches its maximum 17.6 at 12.4 GHz. And reverse isolation is better than 34 dB over the entire band. The measured input reflection coefficient S11 is shown in Fig.4, and is well-matched to below -8.5 dB over the entire X-band (8 – 12 GHz) and Ku-band (12 – 18 GHz).

C. Noise figure analysis

Measured noise figure of the wideband LNA is shown in Fig.4. As shown, the noise figure varies from 5 dB at 8 GHz to 6 dB at 18 GHz. Compared to other work [2-7], the proposed LNA achieves better noise performance with coverage of the entire X-band and Ku-band. And also, active balun was included in our design, the noise figure of proposed LNA is much lower than total noise figure of other wideband LNAs plus external balun.

D. Linearity analysis

Two tone measurements are performed from 8 GHz to 18 GHz with step of 2GHz to measure the linearity of the LNA over the entire frequency band. The frequency spacing of two tones is 100 MHz. The measured input compression point (P1dB) and input third order intercept point (IIP3) at 8 GHz are –23 dBm and –14.2 dBm, respectively, as shown in Fig.5. The linearity is slightly degraded at around 12 GHz due to increased gain. However it again improves above 12 GHz because of the reduced gain. The IIP3 of –14.1 dBm and input P1dB of –24 dBm are measured at 18 GHz. The OIP3 is above 0 dBm over the entire frequency band. Since the device is biased at optimized noise performance, the power supply is low and gain is large, so the IIP3 and input P1dB are a little bit low.

Table I summarizes the measurement results and compares them with previously reported work. Compared to other wideband LNAs, which operate over X-band and Ku-band, proposed wideband LNA achieves lowest mean NF over wide frequency band. Fig.6 shows the die micrograph of the LNA with core size of 0.1 mm^2.

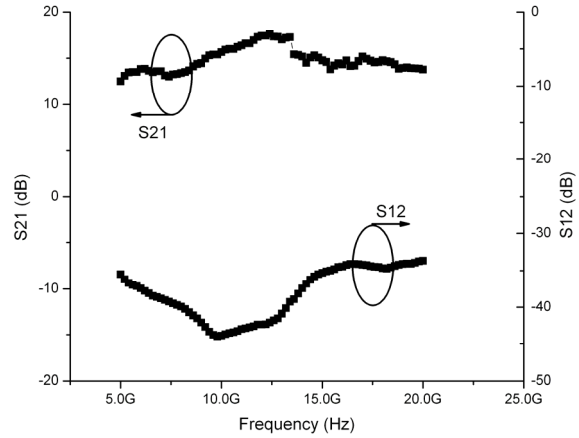

Fig. 3. Measured S21 and S12 of the wideband LNA.

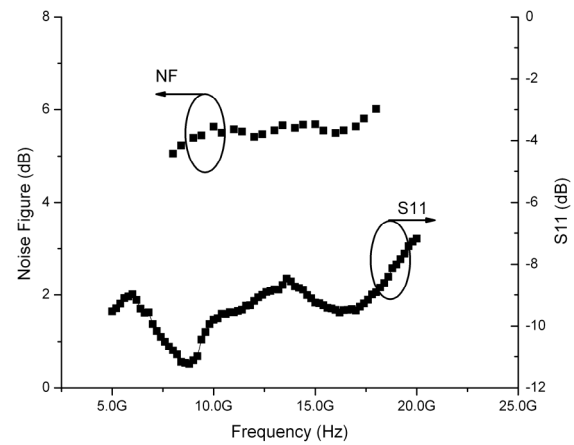

Fig. 4. Measured NF and S11 of the wideband LNA.

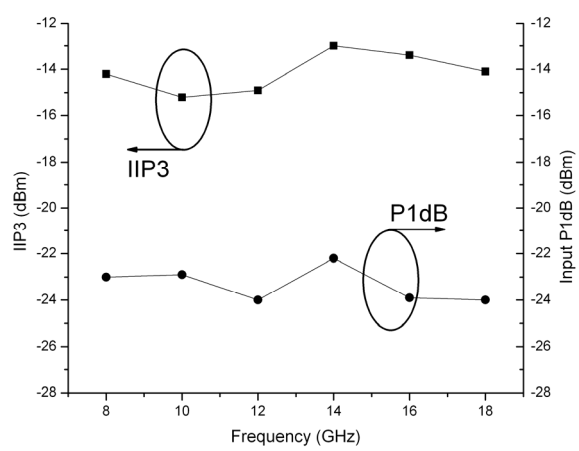

Fig. 5. Measured IIP3 and input P1dB of the wideband LNA.

TABLE I
PERFORMANCE COMPARISON WITH PUBLISHED WIDEBAND LNA

Reference	BW (GHz)	S11 (dB)	Gain (dB)	NF (dB)	IIP3 (dBm)	VDD (V)	Power (mW)	Topology	Process
[2]	3-10	-9	21	2.5–4.2	-5.5	2.7	30	LC- filter	0.18 µm SiGe
[3]	2.3-9.2	-9.9	9.3	4.0-7.0	-6.7	1.8	9	LC- filter	0.18 µm CMOS
[4]	0.5-14	-11	10.6	3.4-5.4	10	1.3	52	Distributed	0.18 µm CMOS
[5]	0.6-22	-8	7.3	4.3-6.1[1]	-	1.3	52	Distributed	0.18 µm CMOS
[6]	3.1-14.5	-1	22	2.7-3.9[2]	-32.5	-	13.2	Common base	0.25 µm SOI SiGe
[7]	2-10	-7	13	2.9-3.3	1.9	2.4	9.6	R feedback	0.18 µm SiGe
[8]	3-10	-7.2	18	1.8-3.1	2.1	3.3	26	LC – filter and R feedback	0.18 µm SiGe
This work	8-18	-8.5	16	5.0-6.0	-14	2.2	38	Proposed	0.13 µm SiGe

[1] 0.6-18 GHz, [2] 3-10 GHz

VII. CONCLUSION

A fully integrated wideband LNA, which covers the entire X-band and Ku-band, is designed and fabricated in a commercial SiGe BiCMOS technology. The design utilizes resistive shunt feedback and inductive load compensation topology to achieve a flat gain and low noise figure over the entire frequency band. The measured performance of the wideband LNA shows typical noise figure of 5.5dB over the whole band. The overall performance of the wideband LNA is comparable to the best-reported wideband LNA at similar operating frequency range, as shown in Table I, giving it a decided advantage for wideband applications.

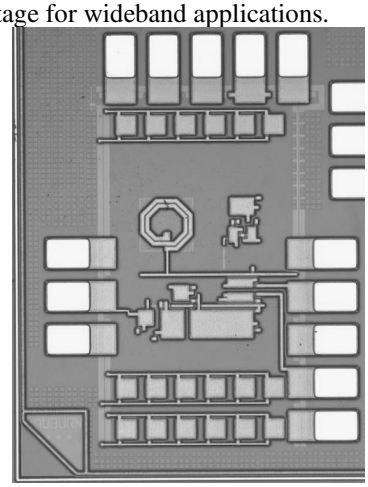

Fig. 6. Die micrograph of the SiGe wideband LNA.

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