

A Fully Integrated 900-MHz Passive RFID Transponder Front End With Novel Zero-Threshold RF–DC Rectifier

Yuan Yao, Jie Wu, Yin Shi, *Member, IEEE*, and Fa Foster Dai, *Fellow, IEEE*

Abstract—This paper presents a fully integrated CMOS analog front end for a passive 900-MHz radio-frequency identification (RFID) transponder. The power supply in this front end is generated from the received RF electromagnetic energy by using an RF–dc voltage rectifier. In order to improve the compatibility with standard CMOS technology, Schottky diodes in conventional RF–dc rectifiers are replaced by diode-connected MOS transistors with zero threshold. Meanwhile, theoretical analyses for the proposed rectifier are provided and verified by both simulation and measurement results. The design considerations of the pulsedwidth-modulation (PWM) demodulator and the backscatter modulator in the front end are also discussed for low-power applications. The proposed front end is implemented in a 0.35- μm 2P4M CMOS technology. The whole chip occupies a die area of $490 \times 780 \mu\text{m}^2$ and consumes only 2.1 μW in reading mode under a self-generated 1.5-V supply voltage. The measurement results show that the proposed rectifier can properly operate with a -14.7-dBm input RF power at a power conversion efficiency of 13.0%. In the proposed RFID applications, this sensitivity corresponds to 10.88-m communication distance at 4-W equivalent isotropically radiated power from a reader base station.

Index Terms—Backscatter modulation, charge pump, low power, low voltage, pulsedwidth modulation (PWM), radio-frequency identification (RFID), rectifier, RF–dc, zero-threshold.

I. INTRODUCTION

RADIO-FREQUENCY identification (RFID) technology is growing rapidly in many industrial applications such as automated data management, tracking of desired objects, highway toll collection, vehicle theft detection, manufacturing control, and automatic billing counter system [1]–[4]. Compared to conventional bar-code system, RFID has many advantages like longer reading/writing distance, more complicated data management, faster processing speed, more robustness and reliability under various difficult environments, etc. [5], [6]. Despite wider application scope and more advanced functionality, the development of RFID is still restricted by its high fabrication cost and weak process compatibility. In all popular automatic

identification (auto-ID) systems, the bar code has the best cost efficiency and product compatibility. It almost does not impose any extra expense on the target objects which need to be identified, and can be easily combined with almost all products in many material substrates such as paper, glass, plastic, metal, etc. However, the inherent communication demands of an RFID transponder for higher data transmission rate and longer operation distance necessitate a set of complete receiver/transmitter building blocks to accomplish the required complicated functionality, which inevitably increase the fabrication cost of RFID transponders. Thus, in order to improve transponders' worst cost efficiency, it has been an urgent and major task to RFID manufacturers and researchers for a very long time to simplify the transponder design and lower its overall cost.

Compared to battery-based active transponders, the passive RFID transponder has many advantages like much longer product life, smaller size, lower cost, etc. However, its disadvantages are also obvious and mainly arise from the fact that there is no stable external power supply for the whole chip. The batteryless characteristic of passive transponder not only makes the architecture design more complicated but also puts stringent low-power low-voltage design demands for all building blocks in the transponder. Apparently, a good power supply generating circuit, which is the so-called RF–dc rectifier, is needed most and becomes a prerequisite for all building blocks. In an RF–dc rectifier, the voltage multiplier, which converts the incident RF signal to a relatively stable power supply dc with a required certain amount of voltage level, is the most important key component. Meanwhile, the voltage multiplier should also improve the conversion efficiency as much as possible, which actually determines the reading/writing distance for the proposed transponders. Traditionally, the voltage multiplier employed in RFID transponders is composed of Schottky diodes and capacitors [7]–[9]. Due to their small series resistance, small junction capacitance, and low turn-on voltage, Schottky diodes are widely employed in rectifiers to lower substrate losses, shorten charging/discharging time, and enhance conversion efficiency. They are, however, often unavailable in standard CMOS technologies because of their unique device characteristics and manufacturing processes. This inevitably results in a high cost and consequently undermines their attraction in rectifiers. Therefore, this paper proposes to use diode-connected MOS transistors with zero threshold voltage, which is less expensive and more compatible with standard CMOS technologies than Schottky diodes, to improve technology

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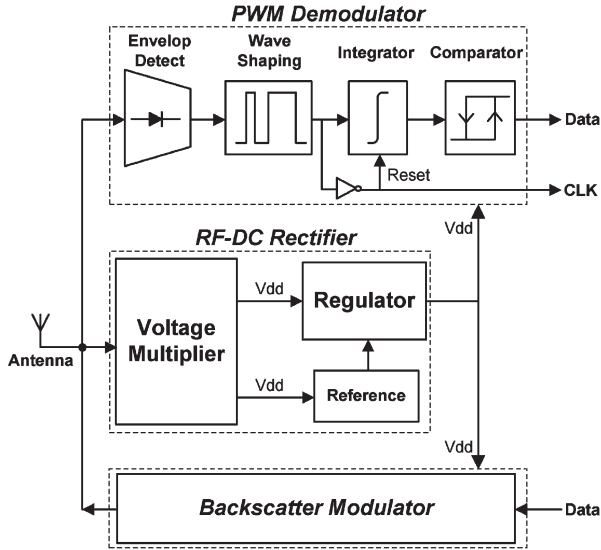


Fig. 1. Block diagram of the proposed UHF RFID transponder front end.

compatibility, increase conversion efficiency, and then eventually lower the transponder fabrication cost [10].

The operating frequencies for most auto-ID systems mainly fall into three categories, namely, low frequency [(LF)—125 kHz], high frequency [(HF)—13.56 MHz], and ultrahigh frequency [(UHF)—900 MHz]. With longer operating distance, faster transmission throughput, and smaller antenna size, UHF 900-MHz RFID systems are a much better candidate for next-generation auto-ID applications [11]–[15]. Thus, this paper focuses on the architecture and implementation of a fully integrated front-end circuit complying with industry standards for passive UHF 900-MHz RFID transponders. Fig. 1 shows a circuit block diagram for the proposed RFID transponder front end. It mainly consists of RF-dc voltage, pulsewidth-modulation (PWM) demodulator, and backscatter modulator. The individual block in this diagram is discussed in more technical detail in the following sections.

The organization of this paper is as follows. Section II mainly focuses on the theoretical analyses and design techniques of the proposed RF-dc voltage rectifier for improving both stability and conversion efficiency. In Section III, the PWM demodulator and backscatter modulator in this UHF RFID transponder front end are described with circuit details for low-voltage and low-power design considerations. In Section IV, the experimental measurement results of the transponder front-end chip are presented. Finally, Section V gives a summary and conclusion.

II. RF-DC RECTIFIER

A. Voltage Multiplier

As shown in Fig. 1, the voltage rectifier used in this passive transponder is composed of three blocks, i.e., zero-threshold NMOS voltage multiplier, reference, and regulator. Since the operating distance for transponders may significantly change in wireless applications, the incident RF signal power correspondingly varies a lot, which is on the order of several dozens of power ratio in decibels. Other than that, any amplitude modulation (AM) may also vary the average input power. Note that the

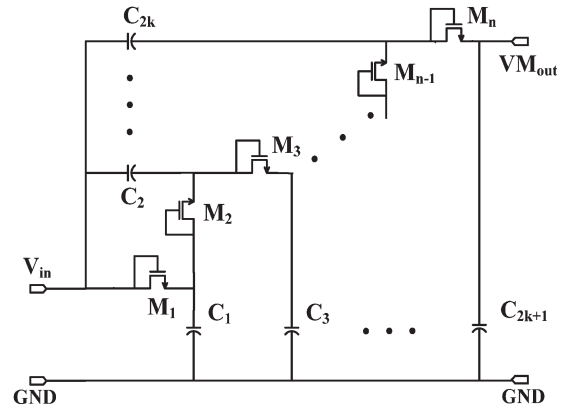


Fig. 2. Simplified schematic of the diode-connected zero-threshold NMOS voltage multiplier.

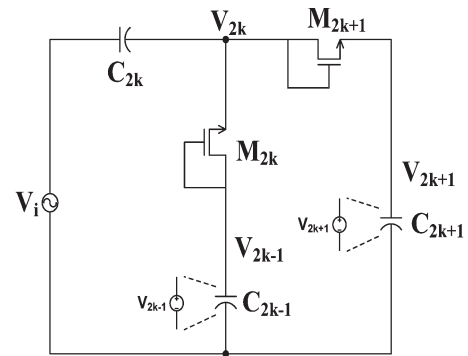


Fig. 3. Unit voltage multiplying cell.

input power change and AM inevitably lead to an unacceptable large fluctuation in the voltage multiplier output. A voltage regulation system is thus usually required to stabilize the output voltage so that other powerless circuit blocks in transponders can work in a correct and healthy mode. The regulator is connected in series with the voltage multiplier to eliminate the voltage ripple by using a low-power voltage reference. The circuit details of the RF-dc rectifier are described as follows.

Fig. 2 shows an odd-stage RF-dc voltage multiplier which utilizes diode-connected NMOS transistors with zero threshold. This odd-stage multiplier consists of n NMOS transistors and n capacitors, where n can also be formatted as $2k + 1$ for theoretical analysis convenience. It can be seen as a combination of unit voltage multiplying cells shown in Fig. 3. The multiplying capacitor C_{2k-1} can be thought of as a dc voltage source, and C_{2k} is an ac coupling capacitor that conducts both input voltage V_i and dc bias voltage V_{2k-1} on the following charging capacitor C_{2k+1} . At the same time, C_{2k+1} is also the dc voltage source for the next unit voltage multiplying cell. Suppose that $V_{d(2k)}$ and $V_{d(2k+1)}$ are the voltage drops on transistors M_{2k} and M_{2k+1} , respectively. V_{2k} is the dc voltage at the intersection node under steady-state condition. It is

$$V_{2k} = V_{2k-1} - V_{d(2k)} = V_{2k+1} + V_{d(2k+1)} \quad (1)$$

for the same charging current I_{ds} . If W/L_s for M_{2k} and M_{2k+1} are made the same, it leads to

$$V_{d(2k)} = V_{d(2k+1)}. \quad (2)$$

Regrouping (1),

$$V_{2k} = (V_{2k+1} + V_{2k-1})/2 \quad (3)$$

due to the coupling capacitor C_{2k} , the actual input signal for M_{2k+1} is the summation of dc and ac input voltages,

$$V_{2k_all} = V_{2k} + V_i. \quad (4)$$

Set ΔV as the unit voltage increment

$$\Delta V = V_i - V_d \quad (5)$$

where V_d is the voltage drop on the corresponding transistor, and according to (1),

$$\begin{aligned} V_{2k+1} &= V_{2k_all} - V_{dn} \\ &= (V_{2k+1} + V_{2k-1})/2 + V_i - V_{dn} \\ &= (V_{2k+1} + V_{2k-1})/2 + \Delta V. \end{aligned} \quad (6)$$

Regrouping (6),

$$V_{2k+1} = V_{2k-1} + 2\Delta V. \quad (7)$$

For the odd-stage voltage multiplier in Fig. 2, since the threshold V_{th} for all transistors is basically constant, the unit increment ΔV for every unit stage can also be regarded as the same. Then iterating the aforementioned formula, it has

$$V_{2k+1} = V_{2k-3} + 4\Delta V = V_{2k-5} + 6\Delta V. \quad (8)$$

Finally,

$$V_{2k+1} = V_n = n\Delta V = n(V_i - V_d) \quad (9)$$

where $n = 2k + 1$ is the number of NMOS transistors and voltage multiplier stages. Equation (9) is the mathematical expression for the proposed voltage multiplier output voltage. As shown in (9), in order to obtain a higher output voltage by a fixed input voltage, V_d should be minimized, and stage number n should be increased. It is the reason why zero-threshold MOS transistors are used in this design to improve the conversion efficiency. Although it seems that the larger the stage number n , the higher the output voltage, it is also apparent that large stage numbers with more device cost increase power consumption and then form a tradeoff between stage number n and conversion efficiency.

During the charging mode, all transistors are operating in the saturation region and have

$$V_d = V_{ds} = \sqrt{2I_{ds}/K} + V_{th} \quad (10)$$

where $K = \mu_n C_{ox} W/L$. For a fixed output power, the average charging current for the voltage multiplier is also constant. Obviously, for a constant output current I_{ds} , the bigger the W/L and the smaller the V_{th} , the lower the V_d . Therefore, in order to obtain a higher output voltage, small- V_{th} MOS transistor and large W/L should be employed. In this design, transistors with 23-mV ultralow threshold are used to improve the proposed voltage multiplier performance.

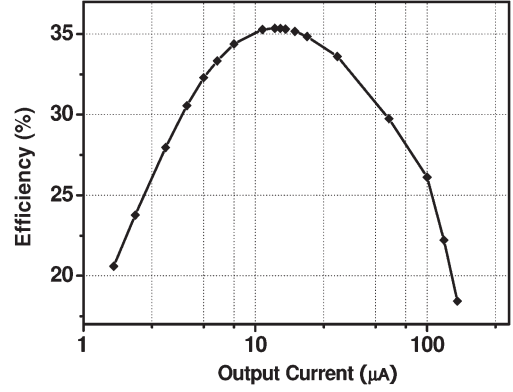


Fig. 4. Simulated curve of conversion efficiency versus output current. Efficiency reaches the peak value of 35.3% at 10.5- μ A output current.

Conversion efficiency is the most important parameter to evaluate voltage multiplier performance. It is defined as

$$\eta = P_o/P_i = 1 - P_{loss}/P_i \quad (11)$$

where P_i , P_o , and P_{loss} are the input power, output power, and circuit power loss, respectively. Conversion efficiency is actually the determinative factor for the operating distance of passive RFID transponders. The higher the η , the longer the distance that the transponder can operate in. As seen in (11), reducing the power loss in the conversion process can directly increase the conversion efficiency. If the parasitic resistances of capacitors are ignored, the power loss in the voltage multiplier mainly come from the NMOS transistors. In the process of multiplying, an NMOS transistor is charged in the positive half-period and discharged in the negative half-period. Because of the reverse block of the diode-connected NMOS transistor for discharging current, the power loss only occurs in the charging half-period. Meanwhile, for a UHF 900-MHz signal, all multiplying and coupling capacitors can be thought of as shorted and powerless. Each NMOS transistor can be roughly modeled as a channel resistance R_{ch} and a parasitic parallel capacitance C_p . It has

$$P_{nmos,loss} = I_{ch}^2 R_{ch} + I_{cp}^2 R_{ch} \quad (12)$$

where I_{ch} and I_{cp} are the average charging currents for channel resistance and parallel capacitance, respectively. Thus,

$$\begin{aligned} P_{nmos,loss} &= \frac{1}{2} \left(\frac{V_i}{R_c} \right)^2 R_c + \frac{1}{2} \left(\frac{V_i}{|Z_{cp}|} \right)^2 R_c \\ &= \frac{1}{2} V_i^2 \left(\frac{1}{R_c} + R_c \omega^2 C_p^2 \right). \end{aligned} \quad (13)$$

Note that $P_{nmos,loss}$ is smallest and η is largest when

$$R_c = \frac{1}{g_m} = \frac{V_{gs} - V_{th}}{2I_o} = \frac{1}{\omega C_p}. \quad (14)$$

It is evident that there is a tradeoff between output current and conversion efficiency for the voltage multiplier, and the optimal output current value exists to maximize η . According to the MOS transistor device model, $g_m = \sqrt{2KI_o} \propto \sqrt{W/L}$; thus, an optimal W/L also exists to obtain the best η . Fig. 4

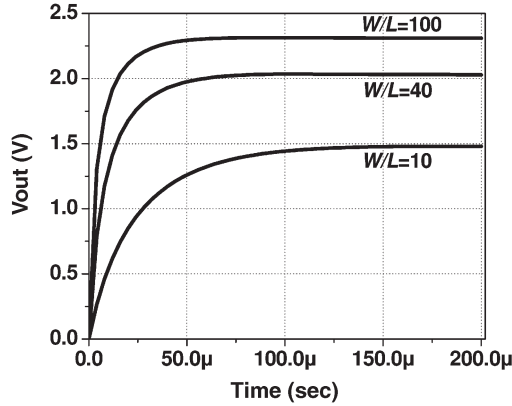


Fig. 5. Simulated transient response of the proposed voltage multiplier with different W/L ratios for zero-threshold transistors.

shows the simulation results for output current versus conversion efficiency of the proposed voltage multiplier. Meanwhile, Fig. 5 also shows its simulated transient response with different W/L 's. It can be seen that output voltage and setup time become larger and shorter with increased W/L , respectively. This mainly results from the fact that a larger W/L can conduct a larger charging current for the next multiplying cell and lower required V_{ds} . Although it seems that a large W/L should be used to obtain a high output voltage and a fast setup time, the value of W/L should be optimized for maximizing the conversion efficiency due to the batteryless fact of passive RFID transponders. In the proposed design, a nine-stage voltage multiplier with 32/0.35 W/L ratio is used to achieve the best overall performance based on device characteristics in the given fabrication technology.

B. Low-Power Voltage Reference and Regulator

The RF input signals with different input power levels and modulation indices inevitably cause fluctuation and instability in the output voltages of the voltage multiplier. This phenomenon is undesired for a stable-required power supply in passive RFID transponders. Thus, the regulator system, shown in Fig. 6, is used to eliminate the output ripple and provide a stable power supply for different output loads. This regulator system is in series with the voltage multiplier and consists of three blocks, i.e., diode regulator, voltage reference, and series regulator.

The diode regulator simply uses four series diodes to provide a preliminary regulating strategy, which only limits large output swing, which is on the order of dozens of tens of volts, to a relatively small swing. However, this coarse regulator is not effective enough to provide an acceptable stable power supply, and its output still has several hundred millivolts swing. Therefore, a reference-based regulator with high regulating accuracy is needed.

Because of its passive and fully integrated characteristic, the RFID transponder cannot have an external voltage reference. It means that all reference voltages must be self-generated, even the power supply voltage. As shown in Fig. 6, a 1.5-V power supply voltage is directly generated through a β self-biasing voltage reference, instead of using the conventional way to accurately amplify a pregenerated low reference voltage.

$M_5 - M_{10}$ build up a triple-cascode connection to increase output resistance, and all operate in the subthreshold region to minimize power consumption. In the subthreshold region, the drain-source current [16] is approximately

$$I_{sds} = I_{do} \frac{W}{L} e^{q(V_{gs} - V_{th})/(nkT)} \quad (15)$$

where

$$I_{do} = \mu_n C_{ox} \left(\frac{kT}{q} \right)^2 e^{1.8}. \quad (16)$$

If the W/L of M_9 is made Q times larger than that of M_{10} and both have the same L , the V_{gs} of M_9 and M_{10} can be rewritten in terms of the current I_{sds} as

$$V_{gs10} = n \frac{kT}{q} \ln \left[\frac{I_{sds} \cdot L}{I_{do} \cdot W} \right] + V_{th} \quad (17)$$

$$V_{gs9} = n \frac{kT}{q} \ln \left[\frac{I_{sds} \cdot L}{I_{do} \cdot Q \cdot W} \right] + V_{th}. \quad (18)$$

Meanwhile,

$$V_{gs10} = V_{gs9} + IR_r. \quad (19)$$

Solving for the subthreshold current I_{sds} using (15), (17), and (18), it becomes

$$I_{sds} = \frac{n \cdot kT}{qR_r} \ln Q \quad (20)$$

which is independent of the dc supply source and is much smaller, only on the order of several dozens of nAs, than the current operating in typical saturation region. With such a constant and small current, the voltage on the drain of M_6 can also be stable and independent of the power supply. To minimize the lowest workable RF input power for the whole transponder, such a reference is expected to operate under a power supply voltage as low as possible. The zero-threshold PMOS transistors $M_3 - M_4$ are used as the current mirror load to reduce the required V_{ds} voltage drops.

A series regulator simply uses a one-stage amplifier and a negative feedback NMOS transistor to make an output fixed on the given reference voltage. In order to achieve low-dropout regulation and ensure that M_{16} operates in the saturation region, the zero-threshold MOS transistor with large W/L is used. C_L is the loading capacitor to provide charge storage for the following circuit blocks and should be large enough to guarantee good loading capability for different output currents.

After the precise regulating system, the voltage multiplier output voltage with large swing is finally converted into a precise and stable 1.5-V power supply voltage with good loading capability. This proposed RF-dc rectifier successfully realizes the input independence and low power for the conversion from incident RF signal to stable dc voltage. Fig. 7 shows the transient simulation for the complete RF-dc rectifier with different input power levels. It can be seen that even for a wide input power range from -19.25 to 13.22 dBm, the output voltage can reach the required 1.5 V in a very short setup time, which is less

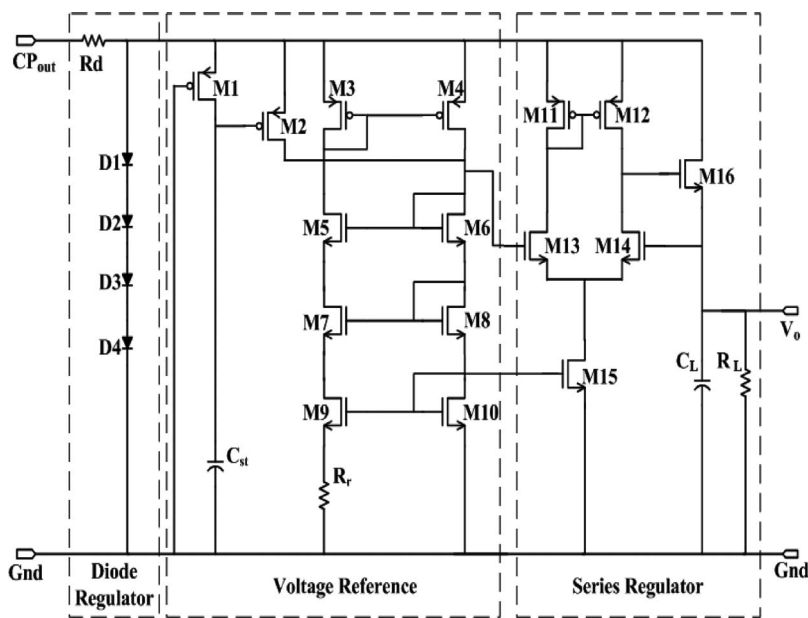


Fig. 6. Schematic of the low-power regulator system.

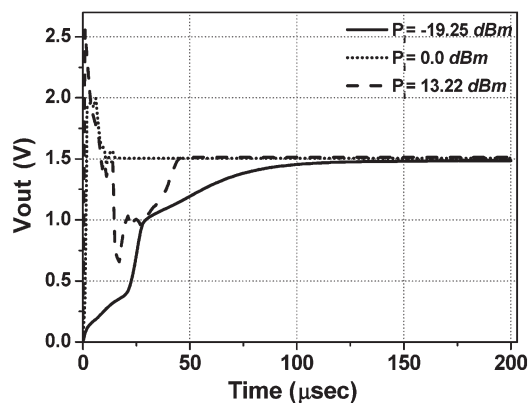


Fig. 7. Simulated transient analysis response of the proposed RF-dc rectifier with different input power levels.

than 125 μ s. The overall variation is smaller than 3%, which is already a good power supply for all building blocks in the RFID front end.

III. PWM DEMODULATOR AND BACKSCATTER MODULATOR

According to the universal RFID standard, PWM is used as the modulation scheme to communicate between the reader and the transponder [17], [18]. Compared to other modulations, the biggest advantage of PWM is its use in simplifying the demodulation block. By saving the usage of complicated demodulation circuits, PWM can make the RFID receiver channel a power saver and consequently improve the overall performance of the passive RFID transponder. As shown in Fig. 1, the interrogating signal received by antenna is first fed into the envelope detect block so that the PWM envelope signal can be obtained. The PWM signals with sharp transition curve are generated by using a waveshaping block, and at the same time, its reverting signal can also be used as the system clock and reset control signal for the following integrator. The integrator can generate different

voltages according to different duty cycles for logic “1” and “0” signals in PWM. Then, the voltage difference is converted into logic “1”s or “0”s by comparing them with a fixed reference. Finally, the PWM signals are demodulated into the required digital data which can be interpreted as the command data to control the operation of transponder or the information data to be written into the transponder ROM.

Another technique used to minimize the power consumption in the proposed transponder is to use backscatter modulation as the transmitting scheme [19]–[21]. The output impedance seen from antenna can be easily changed by simply adjusting the voltage drop on the output varactor according to the digital data previously stored in the transponder ROM. The variation in output impedance modulates the incident signal coming from the reader, and at the same time, the antenna backscatters the modulated signal back into the reader. Finally, the reader can demodulate the backscatter-modulated signal to get the required data stored in the RFID transponder. While conventional transmitters consumes much more power for complicated digital-to-analog converter, frequency upconversion, and power amplifier, the backscatter modulator uses the least device cost and power to realize the required communication from the transponder to the reader.

A. Envelope Detector

As discussed in the previous sections, the batteryless characteristic of the passive RFID transponder necessitates the fact that the front-end design needs to lower the required power consumption as much as possible. Thus, although it is more susceptible to noise and overmodulated input signal, the simple diode envelope detector is used to ensure low-power design. Fig. 8 shows the simplified schematic of the diode envelope detector. The capacitor stores up charge on the rising edge of the input signal and releases it slowly through the parallel resistor when the signal falls. The diode provides the backward isolation

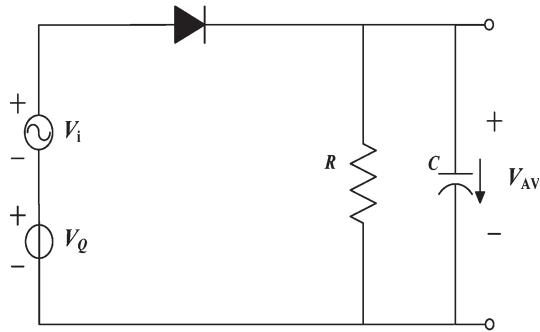


Fig. 8. Simplified schematic of the envelope detector of PWM.

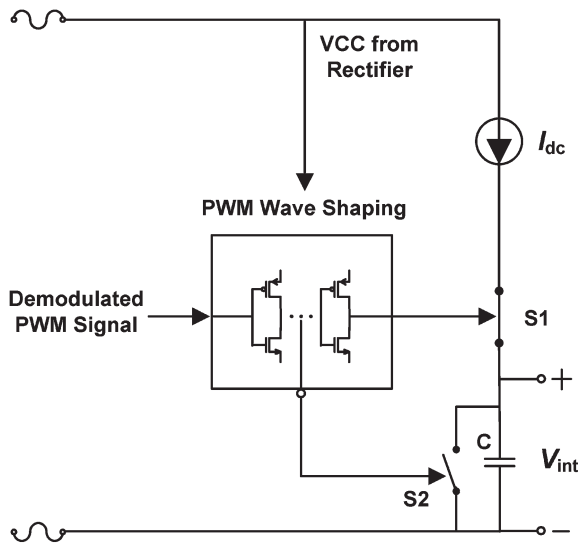


Fig. 9. Simplified schematic of the proposed integrator in integrating mode.

from the capacitor to the input. Similar to the aforementioned voltage multiplier, the diode-connected MOS transistor with zero threshold is used to lower the turn-on voltage drop and improve the process compatibility. In order to improve the detection accuracy and provide enough signal amplitude to the following blocks in the PWM demodulation channel, a three-stage voltage multiplier is put in front of the final diode to amplify the ac amplitude and dc bias of incident RF signals.

B. Integrator

The integrator utilized in this design is used to generate different output voltages according to different endurance times of high voltage level for different logic data in PWM signals. For the same power-saving purpose, a simple switch-controlled capacitor integrator is employed. The simplified schematic of the integrator for the integrating mode is shown in Fig. 9. During the integrating mode, switch S1 is turned on, and S2 is turned off so that the constant I_{dc} can be integrated into the current on the capacitor. When the integrating mode is over, S2 is turned on, and S1 is turned off, the voltage on the capacitor is reset to zero and is ready for the next integrating mode. The integrated voltage on the capacitor is proportional to the high-level endurance time in PWM signals that makes S1 turn on. Meanwhile, since the high-level endurance time for logic “1”s is longer than that for logic “0”s, the integrating output voltage

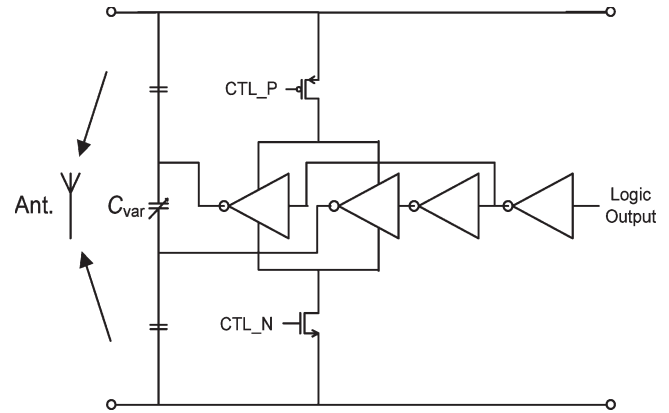


Fig. 10. Schematic of the backscatter modulator.

for “1”s is also larger than that for “0”s. Later, the difference in output voltage can be converted into digital data by the following comparator.

C. Backscatter Modulator

A backscatter modulator modulates the incident RF interrogating signal by changing the output impedance seen from antenna. The simplest way to make the output varactor change between its maximum and minimum capacitances is to switch the voltage drop on it between plus and minus V_{CC} . As shown in Fig. 10, the digital output from the transponder ROM is buffered by a chain of inverters. CTL_P and CTL_N are the bias control signals which can make the bandwidth of the backscattered signals comply with the regulations by adjusting the biasing current of output buffers [12]. The voltage drop on the varactor can switch between plus and minus V_{CC} according to logic “1”s and “0”s, respectively. With two capacitors in series, the varactor is connected to the antenna to correspondingly adjust the output impedance according to the logic data.

IV. MEASUREMENT RESULTS

The proposed UHF RFID transponder front end is implemented in a $0.35\text{-}\mu\text{m}$ CMOS technology. In addition to standard CMOS devices, this technology has zero-threshold MOS transistors which are particularly helpful for increasing the conversion efficiency of RF–dc rectifier in transponders. The high-density high-linearity MIM capacitors make the layout more compact and the rectifier more efficient. Deep-trench isolation is extensively used to achieve good signal crosstalk isolation within the whole chip. The die micrograph of the RFID transponder front-end chip is shown in Fig. 11. The size of the core area is $490 \times 780 \mu\text{m}^2$. In the layout of the RFID front end, since voltage multiplier and PWM demodulator use the same RF incident signal as input, they should be placed separately enough to ensure good isolation for possible signal interference. Fig. 12 shows the test setup for the passive RFID transponder front-end chip with tunable output load resistor which is used to better simulate the rectifier loading effect for different operation distances between the reader and transponders.

As shown in Fig. 13, the RF–dc rectifier generates a stable 1.52-V power supply output from a 0.75-indexed

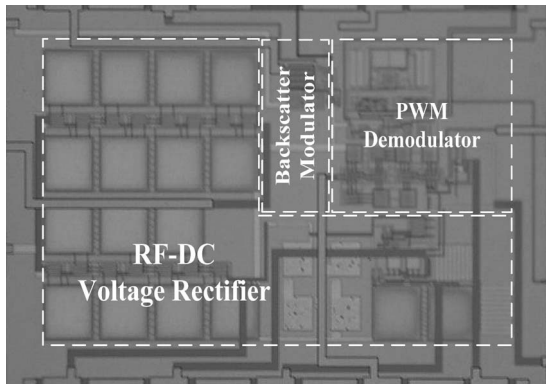


Fig. 11. Die micrograph of the passive UHF RFID transponder front end.

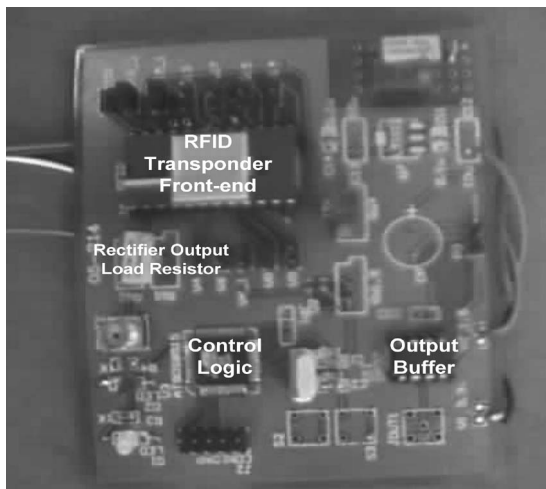


Fig. 12. Test setup for the passive RFID transponder front end with tunable output load resistor.

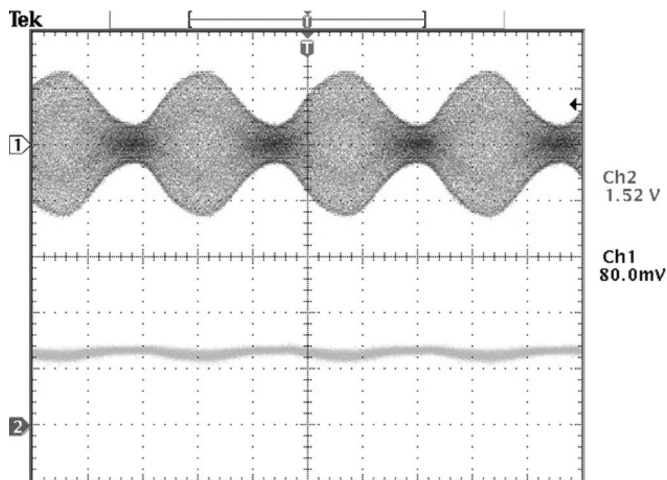


Fig. 13. Measured stable RF-dc rectifier output with modulated UHF input signal. The AM index is 0.75.

AM-modulated input signal with 80-mV input amplitude and 1-MΩ load resistor. Table I also gives the summary of the measured rectifier output voltages with different input power levels. Note that the output voltage cannot be set up in some certain cases of small input power and large output load current. This is because the voltage multiplier cannot provide enough

TABLE I
SUMMARY OF THE MEASURED RF-DC RECTIFIER OUTPUT

Input (mV)	80	90	100	125	150
R_{load} (kOhm)					
250	--	--	1.44	1.46	1.46
400	--	1.46	1.46	1.47	1.51
500	1.48	1.48	1.49	1.49	1.54
700	1.48	1.51	1.52	1.54	1.55
800	1.49	1.53	1.53	1.55	1.56
1000	1.52	1.53	1.53	1.55	1.58

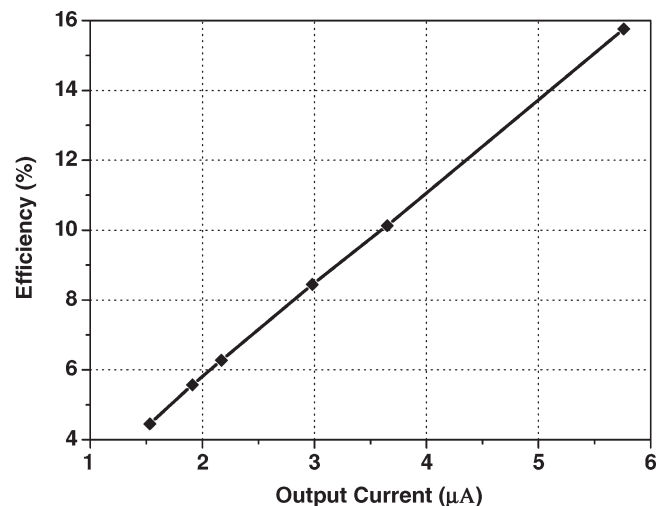


Fig. 14. Measured voltage rectifier efficiency for different output loading currents with 100-mV input amplitude.

loading current with a fixed small input signal, and it is very likely that the voltage multiplier in these conditions is unable to generate the required power supply voltage that is large enough to start up the reference and the regulator circuits. Fig. 14 shows the measured voltage rectifier conversion efficiency for different output loading currents with 100-mV input amplitude signal. The maximum efficiency that the proposed rectifier can reach is 15.76%. The efficiency is basically proportional to the output loading current since a larger output current means a larger output power for a constant input condition.

With 80-mV amplitude input signal and 500-kΩ load resistor, the conversion efficiency of the proposed voltage rectifier is 13.0%. Under specific measurement condition, the 80-mV amplitude input signal is equal to -14.7-dBm input power for the transponder front end. In the proposed RFID applications, this sensitivity corresponds to 10.88-m communication distance at 4-W equivalent isotropically radiated power (EIRP) from a reader base station. The total power for the proposed passive RFID transponder front end in reading mode is 2.1 μW. The summary of front-end performance is listed in Table II.

TABLE II
SUMMARY OF TRANSPONDER FRONT-END PERFORMANCE

Parameter	Performance
Technology	0.35 μm CMOS
Output Voltage	1.52 V @ 80mV input & 1Mohm load
Conversion Efficiency for Rectifier	13.0% for 500 kohm load
Power	2.1 μW in reading mode
Operation Frequency	900 MHz
Receiver Modulation	PWM
Transmitter Modulation	Backscatter
Threshold Voltage in Voltage Multiplier	23 mV
Die Core Area	$490 \times 780 \mu\text{m}^2$
Package	28 pin DIP

V. CONCLUSION

A fully integrated CMOS analog front end for passive 900-MHz RFID transponder was presented in this paper. Instead of conventional Schottky diodes, diode-connected MOS transistors with zero threshold are used as a power supply generator in the on-chip RF-dc voltage rectifier to improve the compatibility with standard CMOS technology. The simulation and measurement results have shown that the proposed voltage rectifier can provide stable power supply voltage with small input power and high conversion efficiency. In order to minimize the required power consumption, PWM demodulator and backscatter modulator are used to simplify the required circuit architecture. The proposed front end is implemented in a 0.35- μm 2P4M CMOS technology. The whole chip occupies a die area of $490 \times 780 \mu\text{m}^2$ and consumes only 2.1 μW in reading mode under a self-generated 1.5-V supply voltage. The measurement results also show that the proposed rectifier can realize an equivalent 10.88-m reading distance with 13.0% power conversion efficiency at a 4-W EIRP base station. Both the simulation and measurement results have proved that the proposed passive RFID transponder front end can properly operate under the condition of very low input power as well as complying with the universal RFID communication standard.

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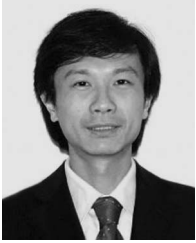
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