A Mixed Signal Wide-Band BiCMOS Frequency Synthesizer for DVB Application

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Abstract — This paper presents a BiCMOS frequency synthesizer covering frequency range from 500 MHz to 2175 MHz which is fully compatible with DVB-S application. The frequency synthesizer consists of monolithic VCOs, utilizing on-chip symmetric inductor, high speed CML divider built with high performance BJT, and can achieve -80 dBc/Hz, -100 dBc/Hz, -123 dBc/Hz phase noise at 1 KHz, 100 KHz and 1 MHz carrier frequency offset, respectively. The 4 VCOs, which can be tuned from 2 GHz to 4.3 GHz with 20 % tuning range each and a maximum kVCO of 200 MHz/V, is divided by two or four to synthesis the desired DVB-S L-band (0.95-2.15 GHz) or other UHF-band frequency. Measure results show that this design works well over a temperature variation from 0℃ to 85℃. The design is implemented with a 0.35 µm SiGe BiCMOS technology.

Index Terms — BiCMOS, CML, DVB, frequency synthesizer, PLL, SiGe, VCO

I. INTRODUCTION

Digital Video Broadcasting (DVB) techniques provide people with tremendous media of high quality and/or mobility. Consumer market trends, especially cost and size reduction, have resulted in digital satellite receivers using zero-IF architectures which allow a high degree of integration, especially because expensive IF filters are replaced by low-pass filters, which are relatively easy to integrate. The tuner ICs used in DVB-S set-top boxes down-convert UHF-band signal (0.95-2.15 GHz) coming from low noise block (LNB) or broadcaster to baseband signal fed into digital demodulator.

A key building block in such tuners is frequency synthesizer or phase-locked loop (PLL). PLL generates quadrature (I/Q) local oscillator signal (LO) to down-conversion mixer for a wide band frequency range. Some challenging tasks to cover the required frequency range include maximizing tuning range of the VCO and fulfilling necessary frequency resolution while maintaining phase noise low enough to meet Bit Error Rate (BER) specification as well as minimizing LO leakage to RF port to keep LO self reception as low as possible. Power consumption and die size are also crucial.

Fig.1 Block diagram of the PLL

This work, as will be discussed below, is capable to synthesize frequency within a range from 500 MHz to 2175 MHz using 4 low noise LC-Oscillators, one of which draws 5 mA from a regulated supply while the other 3 VCOs are power down to save current consumption and to avoid frequency interfering.

In Section II, strategy of the design and PLL characteristics are addressed. Section III highlights the blocks feature, and measurement results are summarized in Section IV.

II. PLL CHARACTERIZATION

The proposed PLL consists of, as shown in Fig.1, a crystal oscillator buffer, a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF) off-chip, a VCO array of 4 VCOs, a divide by 2 or 4 divider for I/Q LO signal generation, a P/P+1 current mode logic (CML) prescaler, a digital programmable divider and a bandgap providing process-voltage-temperature (PVT) irrelevant bias current to CML blocks. By utilizing high performance BJTs, CML divider works noiselessly at 2 GHz and above, which shows advantage prior to CMOS competitors of the same feature size. Efforts have been made for partitioning analog/RF blocks and digital blocks with different supply voltages, from a decreasing power consumption point of view and a noise or spurious signals isolation point of view. A regulator has been designed to supply 3.3 V shifted from 5 V for digital blocks as shown in Fig.1 as dashed border, while solid border represents analog/RF blocks with 5 V supply voltage.
III. BLOCK CHARACTERIZATION

A. VCO

One of some major challenges implementing this VCO is to cover the mentioned frequency range, which is from 500 MHz to 2175 MHz, with 4 VCOs. That means, through dividing by 2 or 4, VCOs should be tuning between 2 GHz and 4.3 GHz, and each VCO experiences a 20% tuning range. As a result, the VCO topology choice should be NPN transistor cross-coupled as shown in Fig.2, instead of its MOS candidate because MOSFET suffers parasitic capacitance which limits tuning range [1]. To maximize tuning range two approaches are involved.

The first approach is to extend valid vtune voltage range coming from CP output, which is from 0.4 to 4.4 V for a 5 V application. The second is to achieve large enough KVCO by using more varactors, thereby shrinking inductor size to decrease inductor value and save area. To couple varactor and inductor high density MIM capacitor CC1 and CC2 are used whose value and Q are large enough so as not to affect the total variable capacitance seen from inductor.

VCO is a key block in a PLL for its phase noise dominates the closed-loop phase noise performance outside the loop bandwidth. Special issues should be considered to obtain high spectrum purity. Utilizing on-chip symmetric inductor, with Q about 15, saves chip area and helps optimize a -120 dBc/Hz phase noise at 1 MHz frequency offset of a 4 GHz carrier, drawing 5.1 mA from a regulated supply. Simulation shows that bandgap current reference’s noise performance affects VCO phase noise dramatically. To minimize this influence bandgap should be designed carefully considering the low noise characteristics of BJT. Large KVCO can degrade closed-loop phase noise as resistor in loop filter must be small to obtain acceptable phase noise performance.

From Leeson’s equation

\[ P_{\text{noise}} = \left( \frac{\omega_0}{2Q\Delta\omega} \right)^2 \cdot \left( \frac{|N_P(s)|^2}{2P_S} \right) \]  

We know that phase noise \( P_{\text{noise}} \) decreases as carrier power \( P_S \) or oscillation amplitude increases. For this bipolar negative \( G_m \) oscillators, to increase signal swing beyond \( V_{\text{BE}} \), the collector and base of Q1 and Q2 are decoupled at dc with C1 and C2, omitting base bias voltage for both Q1 and Q2 in Fig.2 for simplicity. Value of \( R_{\text{b1}} \) and \( R_{\text{b2}} \) should be chosen large enough so as to not to affect the total variable capacitance seen from inductor.

To switch on one VCO out of four, a power controller is added to enable or disable the oscillator. When VCO_en is pulled up by digital control bit, the base and collector of Q4 are pull down to ground to secure that none current is drawn though its emitter and the VCO is powered off. Q4 is necessary in case for collector-emitter breakdown on Q1 and Q2.

B. VCO Buffer & Prescaler

Outputs from 4 VCO are assembled at the VCO Buffer which also performs a divide by 2 or 4 function. These dividers, as well as P/P+1 dual modulus prescaler, are constructed based on a high speed CML flip-flop as fundamental building cell. Fig.3 shows a CML D-Latch that can works at 5 GHz with a 400 µA tail current. Fast switching and low noise characteristics of this circuit come from its limited logic voltage swing range of 400 mV \( V_{\text{pp}} \). Two cascaded D-Latches compose a flip-flop and two or four cascaded flip-flops compose a divider with division ratio of 2 or 4 respectively. Quadrature I/Q LO signals are produced during such progress.

The P/P+1 prescaler also utilizes the flip-flop made of D-Latch as shown in Fig.3, with a modification that tail current in each cell of the last three stages of the prescaler is cut down to 100 µA to save power consumption.
C. PFD

The schematic of PFD and its building block of a CML NOR cell is shown in Fig.4. This PFD is built with a common used tristate structure that inserts pulses on the UP and DOWN output signal even when the phase error is zero between reference signal and divided signal coming from VCO. The dead zone problem is eliminated because of immediate response of CML cell and fast switching of CP. The NOR cells in Fig.4 (a) are simplified as single end input and output while they are all differential input and output as shown in (b).

D. CP

Charge pump is another key block besides VCO in PLL not only because the noise index of CP impacts in-band phase noise of the loop majorly, but also because it’s current mismatch makes up reference spur in carrier spectrum [3]. Thereby design consideration should be focused on minimize CP output noise and current mismatch.

Conventional CMOS CPs have some current mismatching characteristics due to unbalanced conditions between sourcing and sinking current. This mismatch generates phase offset ($\Phi_e$) which increase spurs in the output signal of PLL. The amount of reference spur ($P_r$) can be expressed as [4]:

$$\Phi_e = 2\pi \cdot \frac{\Delta i_m}{I_{CP}} \cdot \frac{\Delta V}{V_{in}} \cdot \text{rad}$$  

$$P_r = 20 \log \left( \frac{\Phi_e}{2\pi f_{fs}} \right) \cdot \text{dBc}$$  

From (3) and (4) we can see that $P_r$ increases as CP current mismatch increases.

To decrease $P_r$, a CP with improved current matching is presented in Fig.5 [2]. The output voltage of CP is sensed by an error amplifier at its negative input, which is followed by its positive input $V_i$. With sufficient gain and bandwidth, $V_i$ would follow $V_{ref}$ with acceptable precision and linearity. When $UP$ in Fig.5 is pull down to ground by PFD output signal, $M5$ and $M6$ share the same source, gate and drain voltage and thereby the same amount of current flow through $M5$ and $M6$ to $Q2$ and $Q3$ respectively when $DN$ is pull up to supply voltage. So $I_{Q3}$ and $I_{M6}$ should be exactly the same and no leakage current is injected to loop filter. Although transient analysis shows that these two current differ from each other slightly when the PFD output zero phase error pulses, matching of sourcing and sinking current improves dramatically compared to conventional CP without error amplifier.

As mentioned above, the tuning range of VCO is desired to be 0.4-4.4 V for a 5 V application. To extend valid CP output voltage range, the error amplifier is designed to be a rail-rail amplifier with 0.3-4.7 V input voltage range.

The presence of Q3 offers much less noise contribution compared to conventional NMOS configuration, for BJT experiences neglectable 1/f noise and thermal noise. PMOS transistor shows better noise performance when larger size is occupied, but at the expense of losing current matching performance because NPN transistor switches on and off much faster than large PMOS. Noise of error amplifier is blocked inside the CP when M1-M4 switch on instantaneous and then off.

The bias current flown into the CP is programmable to provide flexibility of changing loop bandwidth dynamically. Small bias current decreases the gain of CP and therefore narrows the loop bandwidth, while large bias current increases the loop bandwidth.

IV. MEASUREMENT RESULTS

The PLL was tested for frequency coverage, frequency variation over temperature and phase noise performance.

Fig.6 illustrates the frequency range that 4 VCOs covered with $v_{tune}$ range from 0.4 V to 4.4 V at 25°C. It shows a larger $K_{VCO}$ in low $v_{tune}$ than high $v_{tune}$ as expected, because the varactors behave less capacitance under deep reverse bias condition.
Fig. 7 illustrates frequency range of the VCO4 over a temperature variation of 0°C, 25°C, 50°C and 85°C, to testify that VCO could cover the desired frequency range even at extreme condition. Measured result shows that VCO frequency is proportional to temperature at a rate of about 1 MHz/°C, and the VCO is able to cover the wanted frequency range over varied temperature.

Fig. 8 illustrates the phase noise performance of VCO 4 when divided by 4 to generate a 1 GHz LO signal. Measured result denotes an in-band phase noise of a -80 dBc/Hz with loop bandwidth of 10 kHz, a -100 dBc/Hz at 100 kHz offset, and a -123 dBc/Hz.

Fig. 9 illustrates that the reference spur is -60 dBc at 1G Hz carrier.

V. CONCLUSION

The proposed mixed signal wide-band frequency synthesizer had been fabricated in a 0.35 μm SiGe BiCMOS technology, occupying 1.2 mm² die area as shown in Fig. 10. This PLL covers a wide frequency range of 500-2175 MHz with 4 VCOs and is fully compatible with DVB-S (0.95-2.15 GHz) and other UHF-band application while achieving a -123 dBc/Hz at 1 MHz offset.

REFERENCES