An X/Ku-Band Frequency Synthesizer Using A 9-Bit Quadrature DDS

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***Abstract*-This paper presents an X/Ku-band fine-tuning frequency synthesizer using a quadrature DDS implemented in a 0.18µm SiGe BiCMOS technology. The frequency synthesizer comprises a 9-bit quadrature DDS, an 11.7GHz quadrature VCO and image rejection mixers. The outputs of the quadrature DDS are down-converted to 9.4~11.7GHz and up-converted to 11.7~14.0GHz, respectively. The die area of the synthesizer is 3.0x3.0mm^2 and the power consumption is 2.6W under a 3.3V supply. The chip is measured with a 48-pin leadless free ceramic package and external cooling.**

I. Introduction

In the next generation radar system, there are emerging trends toward digitization in radar receiver designs by applying direct intermediate frequency-to-digital conversion (IF sampling) and direct digital synthesis (DDS). The digital radar receivers can obtain much higher precision, low noise, low power and better stability than analog counterparts. Moreover, it can retain the flexibility of digital techniques such as direct digital modulation and waveform generation. A DDS generates a digitized waveform of a given frequency by accumulating phase changes at a higher clock frequency. Microwave range DDS has been developed in both InP and SiGe technologies [1-3] with output frequency up to 10GHz. It's highly desirable to develop frequency synthesis means for X/Ku-band applications. By mixing the outputs of a quadrature DDS (QDDS) and a quadrature VCO, X/Ku-band waveform generation can be achieved.

This paper presents a 0.18µm SiGe BiCMOS X/Ku-Band frequency synthesizer, which consists a 9-bit quadrature DDS, an 11.7GHz quadrature VCO and image rejection mixers. The Nyquist output of the quadrature DDS for 4.6GHz clock input is 2.3GHz. With up-convert and down-convert mixers, 9.4~14.0GHz range can be covered. Packaged in a 48-pin ceramic leadless package, the MMIC occupies 3.0x3.0mm^2 and consumes 2.6W.

II. Architecture and Circuit Design

The conceptual diagram of the frequency synthesizer is shown in Fig. 1. The quadrature outputs from the local oscillator are mixed with the outputs of a quadrature DDS and the mixers outputs are summed and subtracted with each other, so the up-converted and down-converted sine waveforms are derived [4]. The local oscillator generates quadrature outputs with relatively fixed output frequency ω_0, which are mixed with the outputs of a quadrature DDS. Then the mixer outputs are summed and subtracted with each other, so the up-converted cosine waveforms with a frequency of $\omega_0+\omega$ or $\omega_0-\omega$ are derived. Assuming the local oscillator frequency is higher than the output frequency of the quadrature DDS, the above mixing scheme can be used to up convert the DDS output frequency to a higher frequency band.

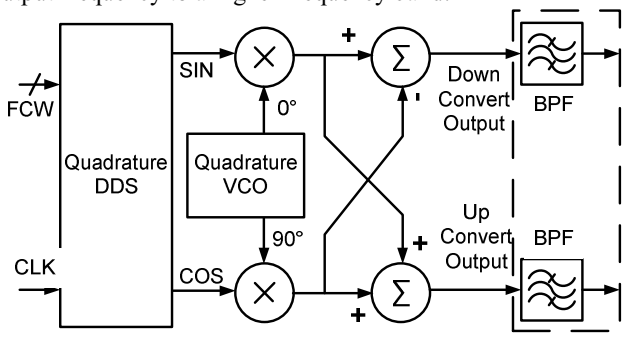

Fig. 1 Concept diagram of the frequency synthesizer.

Theoretically the output should be clean of alias images. However, in practice the DDS output contains harmonics and spurs that significantly deteriorate the purity of desired output waveforms. The imperfections of the mixers due to leakage and second order effects will introduce spurs and harmonics to the output signals. In the multiple GHz DDS design, this will be more complicated due to the impact post by large scale circuit and huge power dissipation.

The frequency synthesizer contains three major parts, the quadrature DDS, quadrature VCO and mixers. DDS can provide quadrature signals with accurate I/Q matching, as shown in Fig. 2. The quadrature DDS is formed by merging two sine-weighted current steering DACs and a 9-bit pipeline accumulator. The nonlinear DAC approach is still attractive for the microwave DDS design because it provides drastically speed improvement to the ROM based or algorithm based DDS design. To reduce the effect of the amplitude error introduced spurs in an ultra high speed DDS needs to be taking into account during the design. The phase truncation error introduced spurs have already minimized because only one bit of the phase accumulator output has been truncated.

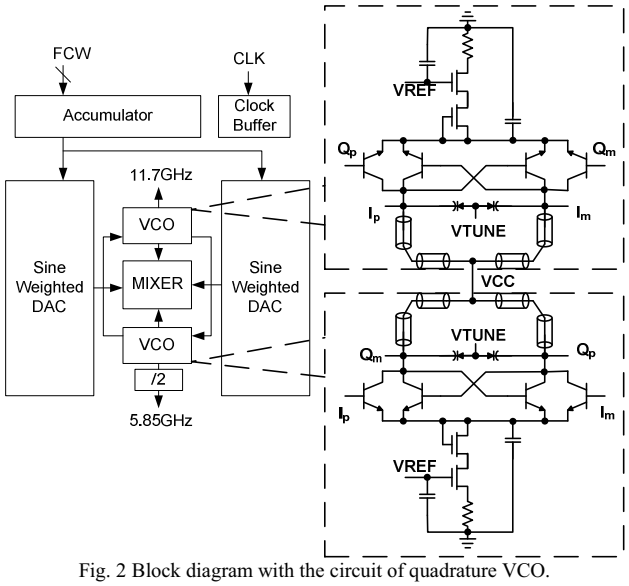

Fig. 2 Block diagram with the circuit of quadrature VCO.

The input frequency control word (FCW) specifies the output frequency of the quadrature DDS. The output of the quadrature VCO is tuned to 11.7GHz and is also divided by 2 to generate 5.85GHz for potential use as the DDS clock. The quadrature VCO design adopts a standard cross-coupled LC-VCO topology. The center tapped inductor in the LC-tank has been replaced by 4 transmission line inductors to facilitate a symmetrical and compact layout. However, the Q factor is relatively lower than typical spiral inductors, which needs to be accounted for in the design. To reduce the losses of the inductors, thick analog metals are used for the connections between the transmission line inductors. To produce the 90 degree phase word, binary number of '01' need to be added to the two most significant bits of the DAC input. Translating the add function into gate level, the output of the MSB is the results of an Exclusive-OR (XOR) of the first two MSB inputs and the output of the 2nd MSB is the inversion of the 2nd MSB input. Because all the digital logics have differential outputs, only one XOR gate is needed to be inserted at the inputs of the sine-weighted DAC to converter it to DAC with 90 degree output phase difference.

The essential building block of the nonlinear DAC is the sine weighted current source matrix. The smallest unit current of each current source is 0.1mA, which should provide the current switches with enough switching speed when toggling. The largest current in the current source is 0.7mA, which is composed of 7 identical current sources. The current switch contains two differential pairs, with minimal sized transistors, and a cascade transistor, to isolate the current sources from the switches, and improve the bandwidth of the entire group of switching circuits. In this ultra-high speed DDS design, the ROMless structure with two nonlinear current steering DACs is employed, and the sine/cosine mapping function is performed by a sine-weighted DAC instead of using the traditional ROM-based sine waveform look-up-table. By eliminating the ROM, speed of the DDS is improved and the power consumption is reduced. This quadrature DDS comprises a 9-bit pipeline accumulator and two 8-bit sine-weighted current-steering DACs. To produce the 90 degree phase, an XOR gate is inserted into the inputs of one sine-weighted DAC. Since the out frequency cannot exceed the Nyquist rate, an 8-bit frequency control word (FCW) is fed into a 9-bit pipeline accumulator with the MSB of the accumulator input tied to zero. The LSB of the 9-bit phase word is truncated, and its MSB is used to provide the proper mirroring of the sine waveform about the π phase point. Its 2nd MSB is used to invert the remaining 6-bits for the 2nd and 4th quadrants of the sine wave prior to the decoding logic. The outputs of 3:8 column-row decoders go to the switch matrix to control the switches in each DAC cell. The latch and switch matrices contain 64 cells.

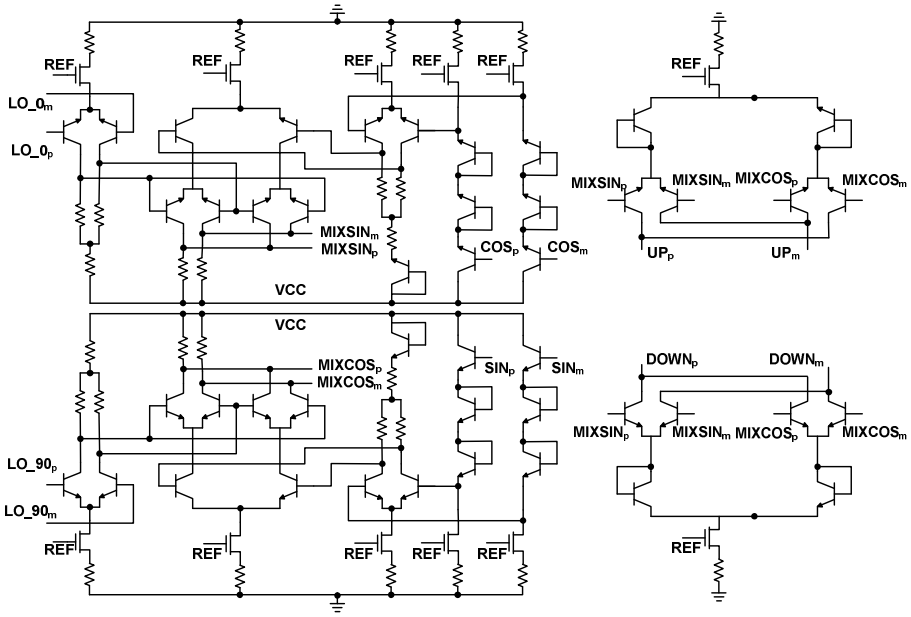

Fig. 3 Circuits of up-convert and down-convert mixers.

The implemented ultra-high speed DDS presents the first mm-wave quadrature DDS design reported so far. When compared with other single-phase mm-wave DDSs [1-3], it's more complex, yet more compact and has lower power, as shown in Table 1. The minimum size of the InP transistor is much larger than that of the SiGe transistor. Although the current density needed to achieve peak f_T frequency in InP and SiGe technologies are similar, the current required to operate the minimum size SiGe transistor is much less. It is for this reason that the SiGe DDS leads to a superior power efficiency performance.

TABLE.1 ULTRA-HIGH SPEED DDS PERFORMANCE COMPARISON. THIS WORK IS QUOTED FOR SINGLE-PHASE / QUADRATURE-PHASE.

Technology f_T/f_{max} [GHz]	InP 137/267 [1]	InP 300/300 [2]	SiGe 120/100 [5-6]
Emitter area of min npn [μm^2]	1.5x4	0.4x2	0.2x0.64
Current density at peak f_T [$mA/\mu m^2$]	1~1.2	5	6
Peak f_T current of min npn [mA]	7.2	4	0.77
Break down voltage B_{vceo} [V]	8	4	1.8
Accumulator size [bit]	8	8	9
DAC resolution [bit]	7	7	8
Max clock frequency [GHz]	9.2	13	9.6/6.3
SFDR [dBc]	30	26.67	30/26
Power consumption [W]	15	5.42	1.9/2.5
Number of Transistors	3000	1646	9600 /13500
Die size [mm^2]	8x5	2.7x1.45	2.3x0.7 /2.3x2.5
FOM[GHz/W/Phase]	0.5	2.4	5.1/5.04

To shorten the connections to the mixers and make the layout as symmetrical as possible, the mixers are placed in the center of the chip, and two VCOs and two sine-weighted DACs are placed at the opposite sides of the mixers. The die photo of the frequency synthesizer is shown in Fig. 4. The active area is approximately 2.5x2.5mm^2.

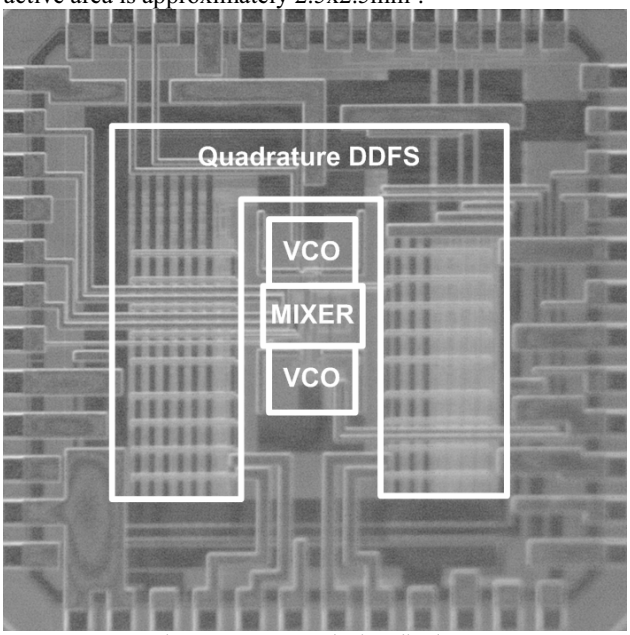

Fig. 4 Frequency synthesizer die photo.

III. MEASURED RESULTS

The test is performed on ceramic leadless free packaged chips. The test board was built using Rogers RO4003 laminate board, which has a loss tangent of less than 0.003 and good temperature stability. To convert the single-ended signal to differential clock inputs, a 180 degree 3dB hybrid coupler is employed at the clock input. For the differential outputs, a second hybrid coupler is inserted into the output path to covert them into single-end for testing. To ensure the chips working in the safe range, external air cooling is used. The measured I/Q waveforms with a digital oscilloscope confirm the 90 degree phase difference of the outputs of the quadrature DDS, as shown in Fig. 5. The measured amplitude imbalance is 5% and the phase imbalance is 2 degree.

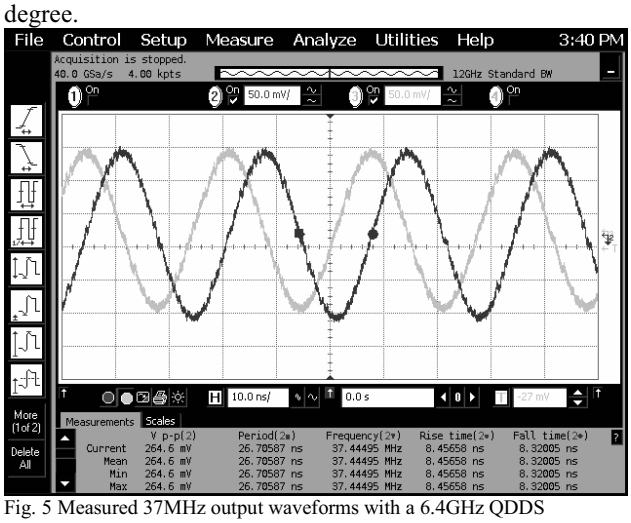

Fig. 5 Measured 37MHz output waveforms with a 6.4GHz QDDS

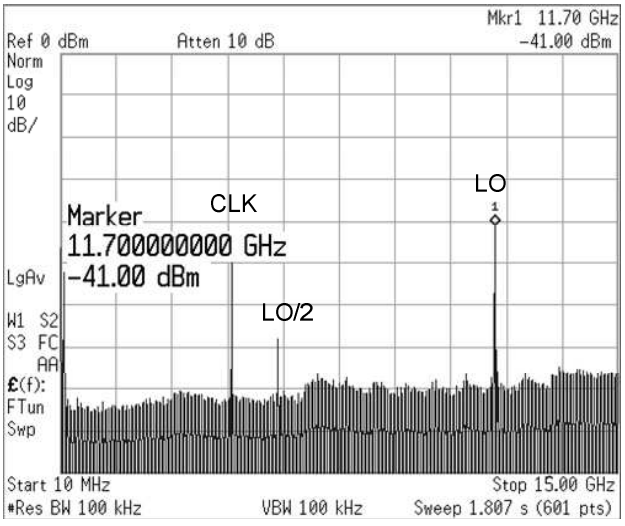

Fig. 6 Measured output spectra of 4.6GHz QDDS clock input and 11.7GHz LO output.

The spectra of the frequency synthesizer outputs shown in Fig. 6-8 are taken at the down-convert output side without calibrate the attenuation. Fig. 6 is the output spectrum of 11.7GHz VCO output and 4.6GHz DDS clock input when

DDS has been turned off. The leaked clock power to the mixer output is -50dBm and the power of leaked local oscillator is -41dBm. The spur at 5.85GHz is purely due to the leakage of the divide-by-2 output of the local oscillator, which contains built in divider for test purpose. The divided output of the local oscillator is attenuated by 27dB.

Fig. 7 shows the Nyquist output spectrum of the DDS with a 4.6GHz clock input when the local oscillator has been turned off. The output of the DDS is located close to 2.31GHz. Since the measurement is taken at the mixer output side, the DDS output power has been significantly reduced. The output power of the quadrature DDS with single output is approximately -53.75dBm.

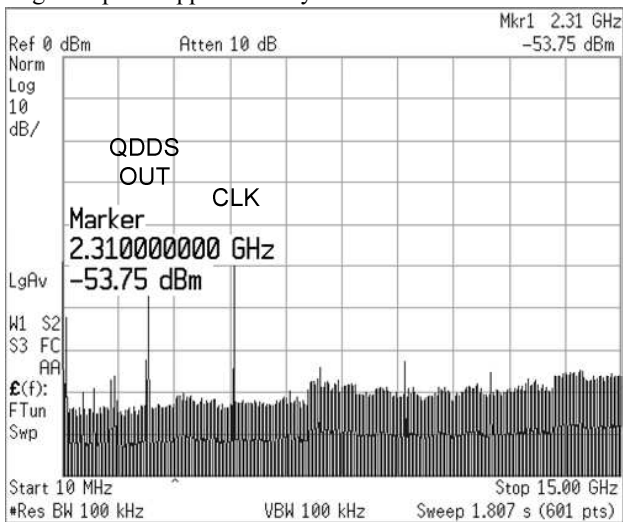

Fig. 7 Measured output spectra of 4.6GHz QDDS clock input and 2.3GHz QDDS output.

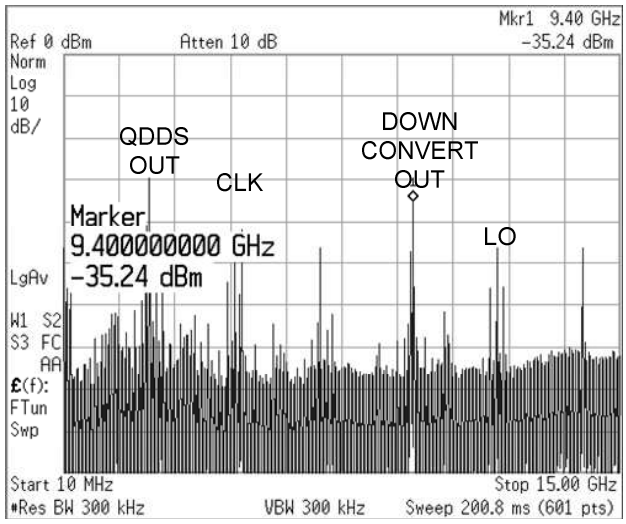

Fig. 8 Measured output down-converted 9.4GHz output.

In Fig. 8, the local oscillator and DDS are switched on and the output spectra of mixed outputs are shown. The frequency of the down-converted signal is 9.4GHz with a power of -35.24dBm and the up-converted 14.0GHz signal can also be noticed which has a power of -46dBm. During the measurement, one of the quadrature outputs of the quadrature VCO shows a strong distortion. One of the reason cause it can be explained as the interconnection wires connecting the transmission line inductors used in the LC tanks are possibly induce inductive peaking and drive some of the transistors into saturation. The single side band suppression has been also affect by the imbalance of the integrated quadrature VCO, which will be improved in the next version.

IV. Conclusion

In this work, a 0.18µm SiGe BiCMOS X/Ku-band frequency synthesizer has been implemented and tested. Containing a 9-bit quadrature DDS, an 11.7GHz quadrature VCO and image rejection mixers, this frequency synthesizer provides a solution for digital tuned and modulated signal generator over 10GHz area. Combined with single side band mixers, the design can cover 9.4~14.0GHz output range. The chip is packaged in a 48-pin ceramic leadless package and occupies 3.0x3.0mm^2 area. With a 3.3V power supply and 4.6GHz external clock input, the total power consumption of the chip is 2.6W.

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