

A 12 GHz 1.9 W Direct Digital Synthesizer MMIC Implemented in 0.18 μm SiGe BiCMOS Technology

Xuefeng Yu, Fa Foster Dai, *Senior Member, IEEE*, J. David Irwin, *Life Fellow, IEEE*, and Richard C. Jaeger, *Fellow, IEEE*

Abstract—This paper presents a 12 GHz direct digital synthesizer (DDS) MMIC with 9-bit phase and 8-bit amplitude resolution implemented in a 0.18 μm SiGe BiCMOS technology. Composed of a 9-bit pipeline accumulator and an 8-bit sine-weighted current-steering DAC, the DDS is capable of synthesizing sinusoidal waveforms up to 5.93 GHz. The maximum clock frequency of the DDS MMIC is measured as 11.9 GHz at the Nyquist output and 12.3 GHz at 2.31 GHz output. The spurious-free dynamic range (SFDR) of the DDS, measured at Nyquist output with an 11.9 GHz clock, is 22 dBc. The power consumption of the DDS MMIC measured at a 12 GHz clock input is 1.9 W with dual power supplies of 3.3 V/4 V. The DDS thus achieves a record-high power efficiency figure of merit (FOM) of 6.3 GHz/W. With more than 9600 transistors, the active area of the MMIC is only $2.5 \times 0.7 \text{ mm}^2$. The chip was measured in packaged prototypes using 48-pin ceramic LCC packages.

Index Terms—Direct digital synthesizer (DDS), frequency synthesis, millimeter-wave, SiGe, waveform generation.

I. INTRODUCTION

INTEGRATING a millimeter-wave (mm-wave) frequency synthesizer into a wireless transceiver that can accommodate multiple standards coexisting in communication systems has been a challenging task and attracted great interest in recent years. One conventional approach to cover the frequency bands for different standards is to use a phase-locked loop (PLL) based frequency synthesizer. However, multiband PLL synthesizers consume large die area and power. Digital synthesis of highly complex wideband waveforms at the highest possible frequency would considerably reduce the size, weight, power and cost of modern communication systems. Recent developments in communication and radar systems are placing increasing demands on low power consumption, high output frequency, fine frequency resolution, fast channel switching and versatile modulation capability for frequency synthesis. These requirements are surpassing the performance capabilities of conventional analog PLL synthesizers. It is difficult for the PLL-based frequency synthesizer to meet these requirements due to internal loop delay, low resolution, modulation problems and the limited tuning range of the voltage-controlled oscillator (VCO). In contrast, a direct digital synthesizer (DDS) generates

a digitized waveform at a desired frequency by accumulating the phase word at a higher clock frequency. DDS is a digital technique for frequency synthesis, waveform generation, sensor excitation, and digital modulation/demodulation. Since there is no feedback in a DDS structure, the DDS is capable of extremely fast frequency switching or hopping at the speed of the clock frequency. A DDS provides various modulation capability and many other advantages, including fine frequency tuning resolution, continuous-phase switching and the ability to provide quadrature signals with accurate I/Q matching. Furthermore, a DDS can generate arbitrary waveforms in the digital domain. The increasing availability of ultra high-speed DACs allows a DDS to operate at mm-wave frequency, providing an attractive alternative solution to conventional analog PLL synthesizers.

Recently, integrated DDS designs have been reported with clock frequencies from 8 to 32 GHz [1]–[4]. Most of these ultra-high-speed DDSs have been implemented in indium phosphide (InP) heterojunction transistor (HBT) technology, and the best power efficiency figure of merit (FOM) achieved is about 3.4 GHz/W [3]. The DDS described herein employs a 0.18 μm silicon germanium (SiGe) BiCMOS technology, which is less expensive, more compact and consumes less power than its InP counterparts. The peak f_t/f_{max} for the 0.18 μm SiGe HBT is 120/100 GHz and the peak f_t current for the minimum size transistor is less than 1/5 that of the InP device [2]. As a result, the DDS design presented in this paper achieves a maximum clock frequency of 12 GHz with a power consumption of only 1.9 W. Operating at the Nyquist rate, the DDS reaches a maximum clock frequency of 11.9 GHz, which corresponds to a record-high power efficiency FOM of 6.2 GHz/W [21].

This paper is organized as follows: Section II introduces the ultra-high-speed DDS architecture. In Section III, we briefly discuss the DDS spectrum purity. The circuit implementation for the DDS MMIC design is discussed in Section IV. Layout issues that have significant impacts on the DDS performance are addressed in Section V. In Section VI, the test platform and measured results are presented, and conclusions are given in Section VII.

II. ULTRA-HIGH-SPEED DDS ARCHITECTURE

A conventional DDS consists of three primary building blocks, a phase accumulator, sine/cosine mapping block, and digital-to-analog converter (DAC), which performs the digital amplitude to analog amplitude conversion [5]. A deglitch filter is normally added off-chip to smooth the waveform by removing the unwanted spectral components. The frequency control word (FCW) at the input of the phase accumulator

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The authors are with the Department of Electrical and Computer Engineering, Auburn University, Auburn, AL 36849-5201 USA (e-mail: yuxuefe@auburn.edu).

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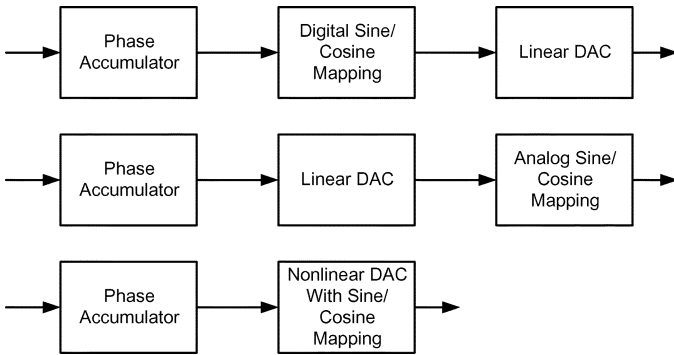


Fig. 1. DDS architectures.

determines the output frequency of the DDS. The sine/cosine block maps the accumulated phase to the sine or cosine amplitude.

Depending on the transfer characteristic of the DAC, a DDS can be characterized in three types, as shown in Fig. 1. The first type represents the conventional DDS that has a linear DAC, and the phase-to-amplitude conversion is done in the digital domain using a sine lookup table [5]. The second one also contains a linear DAC, but the sine/cosine conversion is performed in the analog domain by converting an analog triangle waveform to an analog sine waveform [6]. The third type is a ROM-less DDS that combines both the sine/cosine mapping and digital-to-analog conversion in a nonlinear DAC whose current sources are weighted with sine amplitude information [7], [8].

The first type of DDS has several variations, depending upon the different mapping methods employed in the phase-to-amplitude lookup table. In the traditional DDS, a sine lookup table is built using a ROM which stores the sine/cosine mapping information. However, the ROM size expands exponentially with phase resolution. The sine ROM lookup table occupies the majority of the DDS area, and also limits its maximum operation frequency due to delay through the phase decoders.

The simplest way to reduce the ROM size is to employ the quarter-wave symmetry of a sine function, reducing the ROM size by a factor of 4. Numerous ROM compression techniques have been proposed, including trigonometric approximation [9], [10], parabolic approximation [11], and interpolation [12]. Even though these compression methods partially alleviate the problem, the internal delay caused by retrieving ROM data still restricts the speed of the DDS.

Another approach employs series expansions, such as a Taylor expansion or polynomial expansion, to approximate the ideal curve. The coordinate rotating digital computer (CORDIC) method calculates the amplitude directly, based on the projection of a rotating vector in a polar axial system [13]. Both the series expansion and CORDIC approaches require a considerable amount of hardware, and the complexity limits the final speed, so these structures normally appear in DDS implementations below the multiple GHz range. Using improved differential CORDIC [18], the theoretical output of the ROM-based DDS can reach the GHz range, but its performance still needs proof-in-silicon. Implementing a GHz ROM simply consumes too much power and area. Ref. [18] implemented a linear-DAC DDS in 0.25 μm CMOS technology with 1.2 GHz

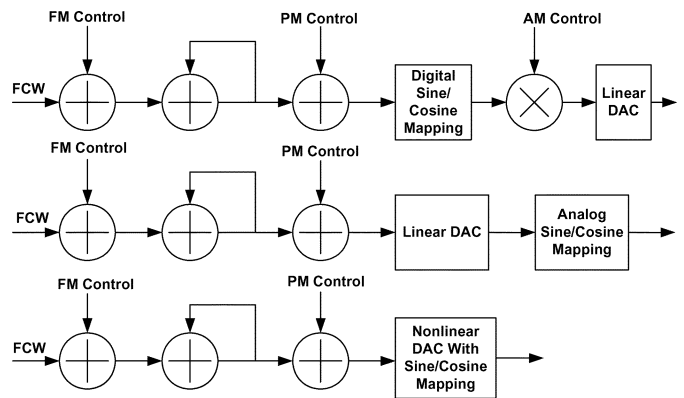


Fig. 2. Digital modulation capability in different DDSs.

clock speed. However, it is very difficult, if not presently impossible, to implement a ROM-based DDS with clock frequency beyond 10 GHz and amplitude resolution larger than 8 bits.

The second type converts a linear analog triangle waveform to an analog sine waveform. This technique utilizes bipolar differential pairs to perform the conversion task by choosing degenerating resistor values and biasing currents to fit the first two terms of a Taylor expansion. Theoretically, 0.1% total harmonic distortion can be achieved, which corresponds to a 30 dB signal-to-noise ratio, or 5 effective bits. Stringent current requirements in the differential pairs limit the usage of this method, particularly when the capacitive load that must be driven varies as a result of different applications.

The third type of DDS is a ROM-less DDS with a nonlinear DAC. The first two structures require a linear DAC, while in a ROM-less DDS, the ROM is removed, and a nonlinear DAC serves as the phase-to-amplitude and digital-to-analog converter. The sine weighted DAC eliminates the sine lookup table, which is the speed and area bottleneck for high-speed DDS implementations.

Our design employs the ROM-less structure with a nonlinear current-steering DAC. This structure combines the sine/cosine mapping block and the digital amplitude to analog amplitude conversion block, thus significantly improving the speed of the DDS. In the ROM-less DDS design, the current-steering DAC structure is an ideal candidate capable of generating a Nyquist output signal with excellent accuracy and high update rate.

Digital domain modulation can be easily implemented in a DDS, as illustrated in Fig. 2. Frequency modulation (FM), chirp, and phase modulation (PM) can be easily implemented in all three types of DDS. However the first type can implement amplitude modulation (AM) in a digital domain prior to the DAC, while the other two can implement AM only in the analog domain. Delta-Sigma ($\Delta\Sigma$) modulation can also be added in the DDS to improve the output spectral purity and to increase the effective number of phase bits [17].

Quadrature rotation can also be implemented in a DDS with quadrature outputs. A quadrature DDS consists of a shared phase accumulator and two DACs with sine and cosine outputs. If linear DACs are used, quadrature rotation can be implemented in the digital domain, since digital quadrature waveforms are available at the inputs of the DACs. For a

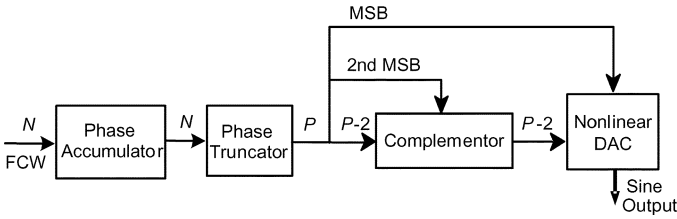


Fig. 3. Conceptual diagram of the ROM-less DDS.

ROM-less DDS, quadrature rotation can only be implemented in analog domain using mixers. A mm-wave quadrature DDS has been implemented in SiGe technology with clock frequency beyond 6 GHz [22].

III. DDS SPECTRAL PURITY

The conceptual block diagram of the ROM-less DDS, employing a nonlinear DAC, is shown in Fig. 3. In order to save die area and power, the phase accumulator output is normally truncated. For instance, the output of the phase accumulator is truncated into P bits, according to the signal-to-noise ratio (SNR) requirement of the DDS output. The two most significant bits (MSBs) are used to determine the quadrant of the phase accumulator output, according to the quadrant symmetry of the sine wave. The lowest $P - 2$ bits are fed through the complementor and converted to a sine waveform by the nonlinear DAC. The sinusoidal waveform data are programmed into the current source matrix of the DAC, and the output currents are summed from the DAC output. In the process of discrete phase accumulation and phase word truncation, spurs and quantization noise will be introduced at the DDS output spectrum as discussed below.

The N -bit FCW feeds a phase accumulator that controls the output frequency of the synthesized sine waveform as

$$f_{\text{out}} = \frac{\text{FCW}}{2^N} f_{\text{clk}} \quad (1)$$

where f_{clk} is the DDS clock frequency. Thus, the desired output period is given by $T_o = (2^N/\text{FCW}) \cdot T_{\text{clk}}$. For an N -bit discrete phase accumulator, there is another periodicity, i.e., $T_{\text{spur}} = (2^N/\text{GCD}(\text{FCW}, 2^N)) \cdot T_{\text{clk}}$, where $\text{GCD}(a, b)$ denotes the greatest common divisor of a and b . The accumulator repeats its value at the intervals of T_{spur} , which generates equally spaced spurious tones located at multiples of the frequency

$$f_{\text{spur}} = \frac{\text{GCD}(\text{FCW}, 2^N)}{2^N} \cdot f_{\text{clk}}. \quad (2)$$

When the input frequency word is a power of two, i.e., $\text{FCW} = 2^i$, there will be no spurs due to discrete phase accumulation. In this case, $\text{GCD}(\text{FCW}, 2^N) = \text{FCW}$, namely, the accumulator output repeats the same frequency after every overflow.

The phase truncation process also introduces spurs and quantization noise, which can be modeled as a linear additive noise to the phase of the sinusoidal wave. Phase truncation error is periodic [10]. If the P MSBs of an N -bit phase word are used to address the DAC or lookup table, the truncation resultant spurs

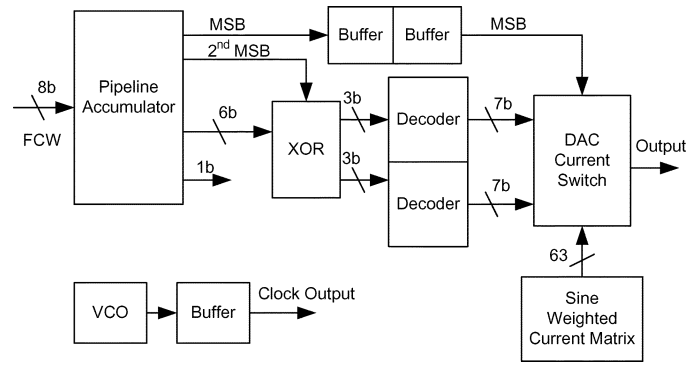


Fig. 4. Block diagram of the implemented DDS MMIC.

are mixed with the DDS output frequency generating spurs at multiples of the frequency

$$f_{\text{spur}} = \frac{\text{GCD}(\text{FCW}, 2^{N-P})}{2^{N-P}} \cdot f_{\text{clk}}. \quad (3)$$

Note the phase truncation causes errors only when the greatest-common-divisor $\text{GCD}(\text{FCW}, 2^N) < 2^{N-P}$. Otherwise, the $N - P$ least significant bits (LSBs) of the phase word vanish and the phase truncation does not cause any error.

In addition to the spurious components, the DDS output waveform will suffer AM distortion due to the finite number of levels that cannot accurately represent the output waveform. The envelope of the DDS output waveform is modulated by a sine wave with the frequency of

$$f_{\text{Envelope}} = \frac{2^{N-1} \bmod \text{FCW}}{2^{N-1}} f_{\text{clk}} \quad (4)$$

where $A \bmod B$ represents the integer residue of A modulo B . If $2^N \bmod \text{FCW} = 0$, no amplitude modulation will be observed. For a Nyquist output, the frequency of the amplitude modulation becomes

$$f_{\text{Envelope}} = \frac{2^{N-1} \bmod (2^{N-1} - 1)}{2^{N-1}} f_{\text{clk}} = \left(\frac{1}{2}\right)^{N-1} f_{\text{clk}}. \quad (5)$$

Therefore, the envelope of the DDS output waveform is modulated by a low-frequency signal except when the FCW is an integer power of 2 such that $2^N \bmod \text{FCW} = 0$.

IV. DDS CIRCUIT DESIGN

The implemented ultra-high-speed DDS MMIC is comprised of a 9-bit pipeline accumulator, and an 8-bit sine-weighted current-steering DAC, as shown in Fig. 4. Since the output frequency cannot exceed the Nyquist rate, an 8-bit FCW is fed into a 9-bit pipeline accumulator with the MSB of the accumulator input tied to zero. The output of the pipeline accumulator is a 9-bit phase word, whose LSB will be truncated before driving the 8-bit DAC. One bit truncation reduces the size and power consumption of the DAC with minimum spurious penalty. The MSB output of the phase accumulator is used to provide the proper mirroring of the sine waveform about the π phase point. The second MSB is used to invert the remaining 6 bits for the

second and fourth quadrants of the sine wave prior to the decoding logic. Each column-row decoder has a linear 3:8 operation. The outputs of the column-row decoders go to the switch matrix to control the switches in each cell [14]. The latch and switch matrices contain 64 cells, and each of the cells is comprised of a local decoder, latches, and switch pairs. The current switch outputs are summed at open-collector output nodes. Next, the circuit design of the DDS building blocks will be discussed.

A. Pipelined Accumulator

The speed of the DDS is often limited by the speed of the phase accumulator. The speed of the accumulator depends upon the N -bit adder design. The simplest way to construct an N -bit adder is to place N 1-bit adders in a chain starting with a 1-bit half adder followed by $(N-1)$ 1-bit full adders with the carry-in of the full adder connected to the carry-out of the previous bit. This ripple adder topology uses the least hardware, but operates at the slowest speed. The delay of a ripple adder is due to the propagation of the carry bit from the LSB to the MSB. The sum and carry-out of a full adder can be expressed as

$$\begin{aligned} \text{Sum} &= A \oplus B \oplus C_{\text{in}} \\ C_{\text{out}} &= A \cdot B + B \cdot C_{\text{in}} + C_{\text{in}} \cdot A \end{aligned} \quad (6)$$

where A and B are the input bits and C_{in} is the carry in of the adder. The delay of an N -bit ripple adder is given by

$$\text{Delay}_{\text{ripple}} = (N-1)T_{\text{carry}} + T_{\text{sum}} \quad (7)$$

where T_{carry} is the time for carry generation and is equal to twice the delay of an AND gate. Similarly, T_{sum} is the time for sum generation in a 1-bit adder and is about twice the delay of an XOR gate.

If the accumulator input is time-invariant, each bit of the input word and the adder output bits can be properly delayed so that a N -bit accumulator can operate at the speed of a 1-bit adder. This type of accumulator, called a pipelined accumulator [19], [20], uses the most hardware, but achieves the fastest speed. Ref. [20] employed the pipeline adder architecture to implement the phase accumulator for a numerically controlled oscillator (NCO).

Fig. 5 illustrates a generic architecture for an $N \times M$ pipelined accumulator with a total of M pipelined rows. Each row has a total of M delay stages placed at the input and output of an N -bit adder. Obviously, an $N \times M$ pipelined accumulator has a latency period equal to the propagation delay of $M-1$ clock cycles. Note that an accumulator needs at least one delay stage even without any pipelined stages. The pipeline accumulator shown allows the $N \times M$ bit accumulator to operate at the speed of an N -bit accumulator, i.e., a speed-up of M times. When the number of adder bits is set to one ($N=1$), the $1 \times M$ bit accumulator can operate at the same speed as a 1-bit adder. To realize a 9-bit accumulator, we can set $N=1$ and $M=9$. Then, a 9-bit accumulator will run at the speed of a 1-bit accumulator consisting of a full adder and a flip-flop.

The pipelined accumulator is used for constant input words and can achieve the maximum operating frequency, whereas an

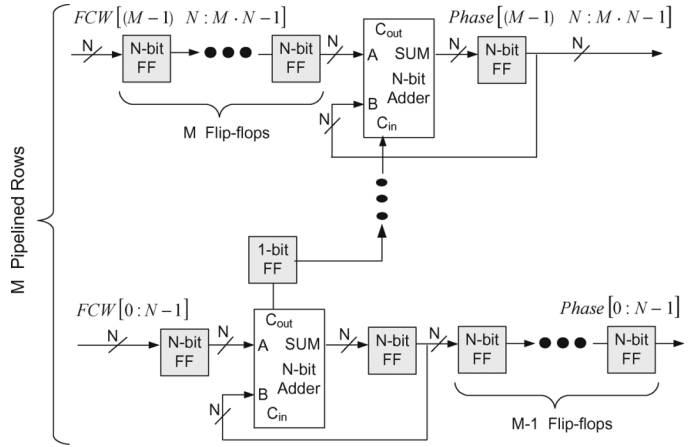


Fig. 5. $N \times M$ generic architecture of a pipelined accumulator.

accumulator with a carry-look-ahead (CLA) adder can be employed for variable inputs with medium operational frequencies. To achieve the maximum operating speed with a fixed FCW, a pipelined accumulator is used in this design. The total delay of the accumulator is one full adder propagation delay plus one D-flip-flop propagation delay. The MSB of the accumulator input is tied to zero, since the FCW will not exceed half of the clock frequency. The LSB of the pipeline accumulator output is discarded and only its 8 MSB bits are fed to the nonlinear DAC. The flip-flops in the accumulator were designed with a reset signal that can be used to reset the accumulator to zero.

In general, the ripple carry adder has complexity in the order of $O(N)$ and delay proportional to N , where N is the FCW length of the accumulator. The hardware cost of the pipeline accumulator is of the order $O(N^2)$. In order to properly trade the area for power, k -bit adders can be used for each pipeline stage as illustrated in Fig. 5. We implemented a 1×8 pipelined accumulator in order to achieve the maximum speed. If 2-bit adders are used in each pipeline stage, the critical path delay will not double based on (7). Thus, the accumulator speed will be greater than half of that of the accumulator using 1-bit pipelined adders.

B. SiGe CML Logic

Previous ultra-high-speed DDS designs used InP technology in order to take advantage of the high-speed InP transistors [1]–[4]. However, these InP DDS designs suffer from high power consumption and low yield. This DDS design utilizes a commercial 0.18 μm SiGe BiCMOS technology with the HBT peak f_t/f_{max} of 120/100 GHz. The digital logic is implemented using current mode logic (CML) cells with differential output swings of 400 mV. For a three-level CML circuit, a 3.3 V power supply is sufficient to keep all the bipolar transistors from saturation. If an NPN transistor operates in saturation mode, its speed is greatly degraded and its parasitic PNP transistor is turned on, causing increased noise coupling through the substrate.

In order to achieve a good balance between speed and power consumption, the bias current is set to 70% of the peak f_T current. Further increasing the biasing current does not speed up the CML circuit significantly. It is not proper to bias the CML

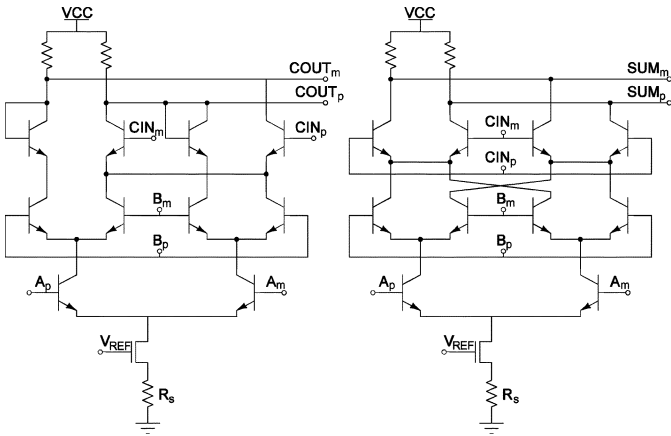


Fig. 6. CML full adder circuit.

circuits at peak f_T current, since any variation of the biasing current may drive the circuit beyond f_T current, slowing down the transistors significantly with unnecessarily large power consumption. Although the peak f_T current is not a parameter that guarantees the operational speed for different CML circuits with different loads, it is a good indicator for the average speed of the CML logic circuits. The current in a typical three-input CML gate is 0.55 mA, which is less than 1/5 of that used in InP DDS designs [2]. This bias current is sufficient to keep the delay of the three-level gates below 25 ps.

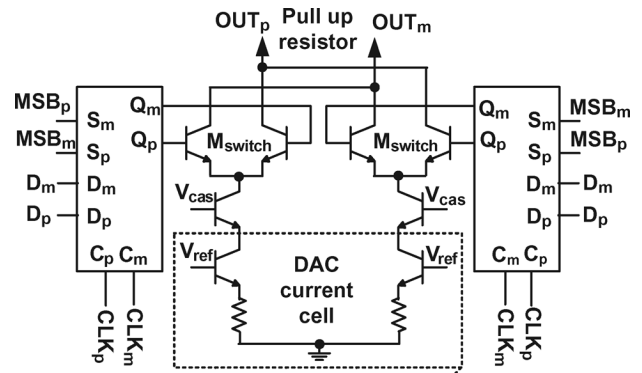
To provide more headroom for bipolar transistor operation, the current source of the CML logic uses an NMOS transistor with degeneration resistor. In this case, the overdrive voltage of the current source MOSFET is around 0.4–0.5 V, which is smaller than the headroom required by a bipolar transistor. In order to ensure that all the critical paths have the same delays, the signal paths are designed using symmetrical patterns.

Pipelined adder stages are used to achieve the speed that is equivalent to a 1-bit adder. To reduce the logic requirement of the adder, the structures described in [15] are adopted, as shown in Fig. 6. The sum and carry-out are implemented using one current tail for low power application. This adder circuit reduces the total number of bipolar transistors in the sum circuit from 14 to 10, and provides a speed improvement of around 15%. The delay of the sum block is estimated to be 30 ps, and the carry block is 25 ps, with optimized biasing.

The breakdown voltage BV_{CEO} of the NPN transistors in the 0.18 μm SiGe BiCMOS technology is approximately 1.8 V. With four-stacked NPNs under a 3.3 V supply, each transistor will experience less than 1 V across the C-E. In addition, all the circuits are self-biased with no base open, which guarantees safe operation of the transistors without breakdown.

C. Clock and MSB Trees

The most challenging parts of the design are the clock tree and MSB buffer tree designs. To eliminate glitches due to code errors induced by clock skews, clock trees are carefully balanced to ensure synchronization and drive capability. Because the differential clock signals drive every flip-flop cell, and the total number of flip-flops is above 200, synchronization of the clock signals is not a trivial task. With a clock input frequency



2	4	6	6	6	5	3	0
0	3	5	6	6	6	4	2
2	4	6	6	6	5	2	1
1	3	5	6	6	6	3	2
3	4	6	3	6	5	3	2
1	3	5	6	7	5	4	1
2	4	5	6	6	5	3	1
0	4	4	6	7	5	5	1

Fig. 7. Current switch circuit of the nonlinear DAC.

around 10 GHz, the current gain of the transistor degrades to about 10. Thus, the fan-out ratio of a clock buffer is only 3–4, and the depth of the clock buffer chain is at least six levels for this design. To fully turn on or turn off the differential pairs, the input differential peak-to-peak voltage swing should be more than $6V_T + I_E R_E$, in which V_T is the thermal voltage and I_E and R_E are the emitter current and emitter resistance of the bipolar transistor, respectively. The voltage swing also depends on junction temperature, which can reach above 100 °C for normal operating conditions. The clock signals at the flip-flop cells should swing no less than 150 mV, which is equal to $6V_T$ at room temperature. Since every switching cell in the DAC has an MSB signal, the total number of gates that the MSB must drive exceeds 120. This MSB signal must also be synchronized with other decoded digital bits. The depth of the buffer chain for the MSB signal is five levels. To accomplish all of this, the clock and MSB buffers require careful design, with layout symmetry and balance, in order to ensure synchronization along the clock and MSB distributions.

D. DAC Current Source and Switch

The essential building block of the nonlinear DAC is the sine weighted current source matrix. The unit current of each current source is 0.1 mA, which should provide the current switches with enough switching speed when toggling. The largest source current is 0.7 mA, which is composed of seven identical current sources. The table in Fig. 7 indicates the number of unit current sources in each sine-weighted current source. The sum of each row is the same, which assures the regularity of the current source array, as well as its compactness.

The current source matrix provides 64 pairs of sine-weighted currents that are summed at the differential current outputs, OUT_P and OUT_M . The current outputs are converted to differential voltages by a pair of off-chip 25 Ω pull-up resistors. Fig. 7 shows that the currents from the cascode current sources

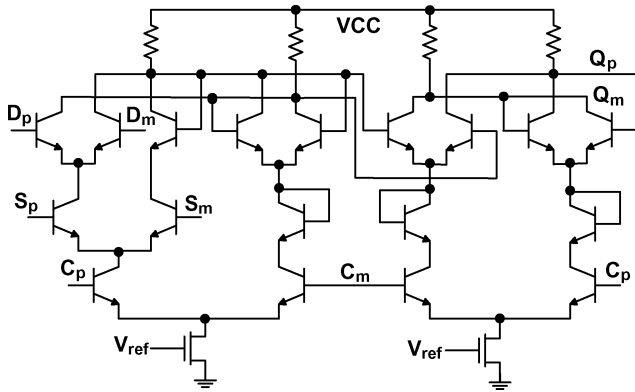


Fig. 8. Synchronous switch control circuit of the nonlinear DAC.

are fed to outputs, OUT_P and OUT_M , by pairs of switches (M_{switch}). The MSB controls the selection between different half periods. The current switch contains two differential pairs, with minimum size transistors, and a cascode transistor to isolate the current sources from the switches, and improve the bandwidth of the entire group of switching circuits. The size of the switching transistor pairs is chosen to be minimal in order to achieve the fastest switching speed with minimum power consumption, and to reduce the effect of clock feed-through.

For the current-steering DAC, the impedance Z_{imp} seen at the collectors of the switch transistors of each current cell must be large enough so its impact on the integral nonlinearity (INL) specification of the DAC can be tolerated [16]. However, Z_{imp} is frequency dependent. The impedance that is required to obtain a specified resolution is approximately

$$Z_{\text{imp}} = \frac{NR_L}{4Q} \quad (8)$$

where R_L is the load resistance, N represents the total number of unit current sources, and Q is the ratio of the signal to the second harmonic. To obtain 8-bit output resolution, Z_{imp} should be approximately 500 k Ω . When the frequency increases above 100 MHz, a cascode current source is needed to meet the requirement for Z_{imp} .

Uncertainty of the switching time of current switches is one of the major causes of glitches at the DAC outputs. To synchronize the switches of the DAC, a D-flip-flop with NAND function is inserted between the MSB control bit and the switch pairs in the DAC. The S_p and S_m are controlled by MSB signal and select either 0 or 180 degree phase, as shown in Fig. 8.

Device matching is one of the important factors that affect the static and dynamic performance of the DAC. The matching properties of SiGe bipolar transistors are normally one order of magnitude better than those of MOSFETs with similar feature sizes. To reduce IR drops and matching errors, one must carefully choose the current source transistor sizes and layout placements, and use wide interconnections. For long interconnections carrying global signals, such as the clock and the MSB phase word, transmission line effects are taken into consideration during the layout. In order to minimize parasitic capacitances and inductances, thick analog metal layers are used for global signal routing.

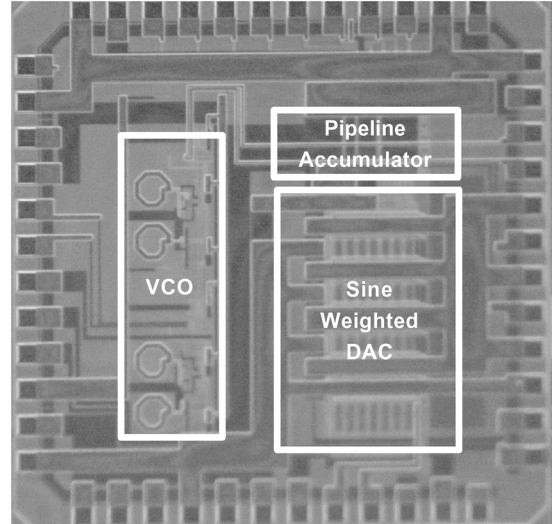


Fig. 9. Die photo of DDS chip.

V. LAYOUT

When running at a 10 GHz clock rate, layout plays an important role in assuring that the final design meets the expected speed requirement. The current source matrix and the switching matrix are separately laid out and isolated from each other using a deep oxide trench to reduce noise coupling from the digital circuitry to the current sources through the substrate. The output of the DAC is placed close to the output pins to reduce interference from the rest of the circuits. Differential pairs are placed in a symmetrical manner so that the differential signals travel the same distance. In order to make the layout compact and easy to cascade, the CML building blocks were designed to have the same height. Power supply distribution stacks several metal layers to reduce resistance.

Cadence Skill language was utilized to generate the connections that form the unit current sources into the sine-weighted current sources, in accordance with the given switching sequence. Hence, the INL of the nonlinear DAC, due to symmetrical and gradient errors, is minimized. Two dummy rows and columns have been added around the current source array to avoid edge effects. To minimize the systematic error, introduced by the voltage drop in the ground lines of the current-source transistors, sufficiently wide wires have been used. The clock inputs are differential CML compatible signals, and multiple clock inputs are provided to reduce the parametric inductance resulting from the pins. The maximum delay of the metal wire is about 40 ps, and the clock tree is carefully built to ensure an acceptable clock skew.

VI. EXPERIMENT RESULTS

The die photo of the DDS MMIC is shown in Fig. 9. This DDS design is quite compact with an active area of $2.3 \times 0.7 \text{ mm}^2$ and a total chip die area of $3 \times 3 \text{ mm}^2$ including the ESD pads, the layer density filling elements and an 8.2 GHz on-chip VCO that could be used to clock the DDS. The DDS prototypes were packaged using 48 pin ceramic leadless packages. For a frequency range over 10 GHz, the PCB test board was developed using a Rogers RO4003 laminate board, which has a loss tangent of

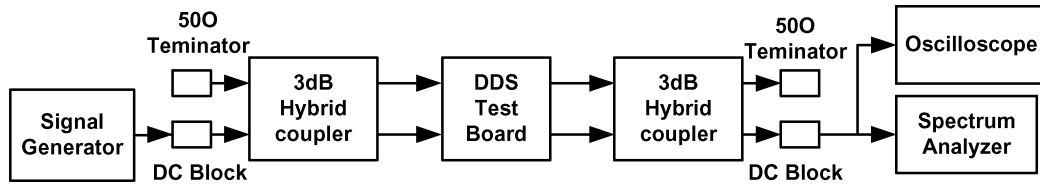


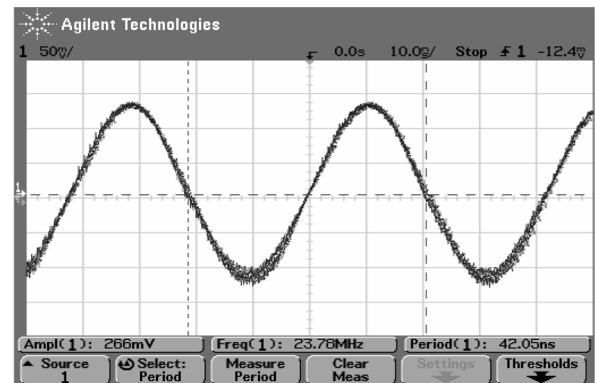
Fig. 10. DDS MMIC test setup.

less than 0.003 and good temperature stability. To convert the single-ended signal to differential clock inputs, a 180° 3 dB hybrid coupler is employed at the clock input. For the differential outputs, a second hybrid coupler is inserted into the output path. The test setup diagram is illustrated in Fig. 10.

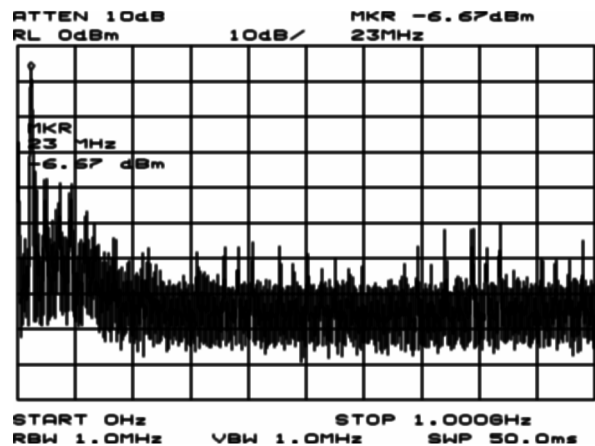
Power consumption of the DDS with the DAC is approximately 1.9 W, and the maximum clock frequency as measured is 12.3 GHz. With Nyquist output, the DDS achieves a maximum clock frequency of 11.9 GHz. The digital and analog parts of a sine-weighted DAC consume 300 mA from a 3.3 V supply and 35 mA from a 4 V supply, respectively. The accumulator consumes 250 mA of current with a 3.3 V supply.

Although the power consumption of the SiGe DDS is small compared to other InP DDS, its power density is high due to its small die size. For 1.9 W power concentrated on a small die area of 9 mm^2 , the power density of the DDS MMIC would exceed 21 W/cm^2 , which is a number that normally appears only for high performance processors. The relatively high power density of the DDS MMIC makes it difficult to dissipate the heat when it is packaged. The junction-to-ambient thermal resistance, θ_{JA} , of the 48-pin ceramic package is about 40°C/W with zero air flow. Therefore, the device junction temperature of the DDS MMIC could reach above 100°C at the room ambient temperature of 25°C with 1.9 W power consumption. For this reason, an external fan is used to cool the device during measurements. To further reduce the thermal resistance and maximize heat dissipation, packages with a heat sink can be used. To our knowledge, other InP MMICs [2]–[4] were tested on wafer, while this SiGe DDS MMIC was tested as a packaged part. To test the maximum speed, the packaged DDS chips were cooled down to -50°C – -80°C such that the junction temperature is around room temperature. This test condition provides a fair comparison between the packaged SiGe DDS MMIC and the wafer-probed InP DDSs. Lowering the junction temperature improves the transistor speed due to increased carrier mobility at lower temperature. Without cooling, the maximum clock speed of the packaged DDS MMIC is measured as 9.6 GHz with Nyquist output and 11 GHz with $\text{FCW} = 1$ at room ambient temperature. For the 20 tested prototypes, the chip performances are quite consistent. SiGe technology gains advantages of high yield and high performance over the InP technology.

Figs. 11–14 illustrate the measured DDS output spectra and waveforms for different outputs and clock frequencies. The measured spectra were obtained by cooling down the packaged chips so that the device junction temperature approaches room temperature. Fig. 11 presents the 23.5 MHz DDS output waveform and spectrum with a 12.021 GHz clock input. The time-domain waveform measurements were limited by the digital sampling scope's 500 MHz bandwidth. The measured



(a)



(b)

Fig. 11. (a) Measured DDS output waveform and (b) spectrum with a 23.5 MHz output ($\text{FCW} = 1$) and a clock at 12.021 GHz.

DDS output power is approximately -6.67 dBm . All measurements were done without calibrating the losses of the cables, the coupler and the PCB tracks.

Fig. 12 gives the measured DDS output spectra at Nyquist rate, namely, (a) output frequency at 5.930 GHz with clock at 11.913 GHz; and (b) output frequency at 5.04 GHz with clock at 10.110 GHz. Fig. 12(a) demonstrates the maximum DDS operation frequency of 11.9 GHz at Nyquist output with the spurious-free dynamic range (SFDR) of 22 dBc. The measured SFDR of the device, at 5.08 GHz output frequency with a 10.11 GHz clock, is approximately 30 dBc in narrowband as shown in Fig. 12(b). For Fig. 12(a), the FCW is chosen as $2^8 - 1$, which is the maximum allowed by an 8-bit FCW input. Thus, the output frequency is set at $((2^8 - 1)/2^9) \times f_{\text{clk}} = 5.93 \text{ GHz}$. The first order image

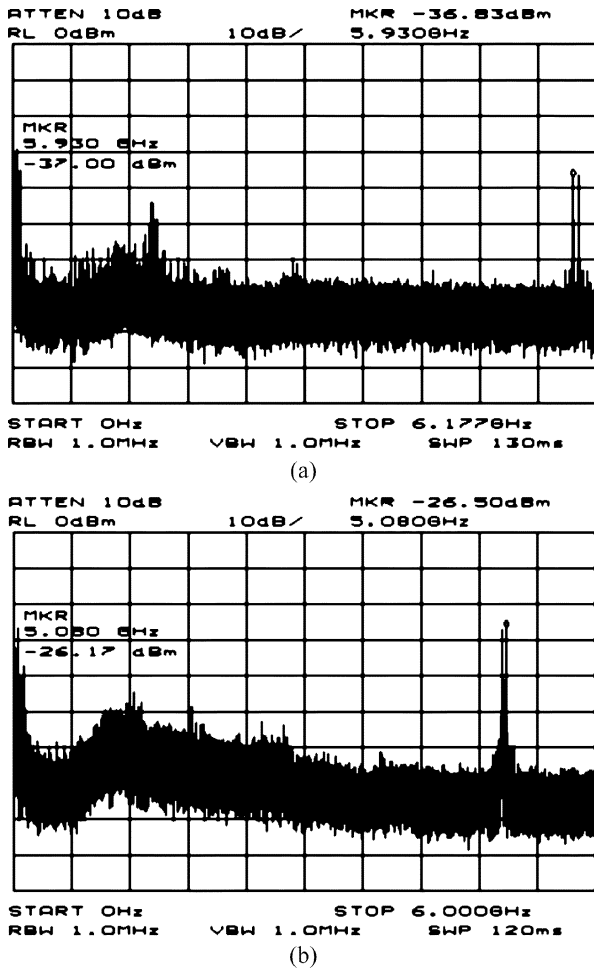


Fig. 12. Measured DDS output spectra at Nyquist rate ($FCW = 511$): (a) the output frequency at 5.930 GHz and the image tone at 5.98 GHz with a clock at 11.913 GHz; (b) the output frequency at 5.04 GHz and the image tone at 5.08 GHz with a clock at 10.110 GHz.

tone mixed by the clock frequency and the DDS output frequency occurs at $11.913\text{ GHz} - 5.93\text{ GHz} = 5.98\text{ GHz}$, which is 50 MHz apart from the output frequency, as shown in Fig. 12(a). Operating the DDS at close to Nyquist rate makes it very hard to filter out the image tones. Practically, the DDS output frequency is restricted to be less than $3/8$ of the clock frequency. An image tone at 5.08 GHz is also observed in Fig. 12(b) with a clock at 10.110 GHz.

Fig. 13 presents the measured DDS output spectrum with a 1.7898 GHz output and a 9.59 GHz clock. The measured output power of the DDS is -9 dBm , which corresponds to greater than -5 dBm power when cable and coupler loss are considered. The input FCW equals 96, so that the $GCD(96, 2^9) = 32$, which leads to spurs equally spaced with 600 MHz spacing around the fundamental tone when the clock is 9.59 GHz.

Fig. 14 gives the DDS output waveforms at 1.125 GHz with a 9 GHz clock. At high temperature, the transistors are slowed down and the DAC current switches are no longer perfectly synchronized due to increased internal delays. Fig. 14 demonstrates a clean sinusoidal output waveform with the package measurements at the 9.6 GHz clock frequency. Fig. 15 illustrates the measured DDS output spurious-free-dynamic-range

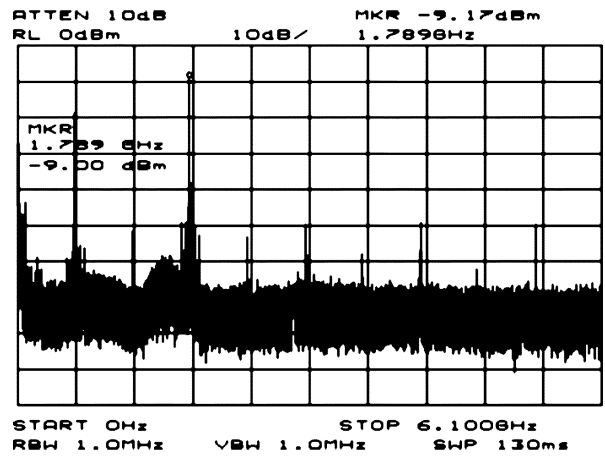


Fig. 13. Measured DDS output spectrum with a 1.7898 GHz output and a 9.59 GHz clock.

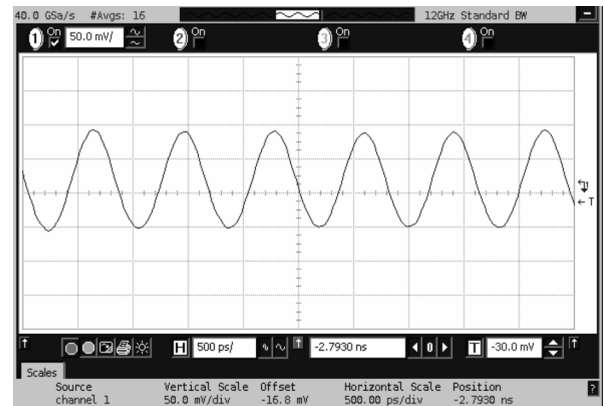


Fig. 14. Measured DDS output waveform with 1.125 GHz output and 9 GHz clock.

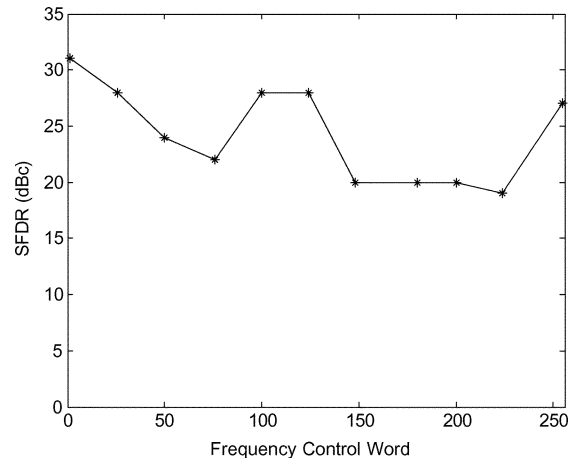


Fig. 15. Measured DDS output SFDR versus frequency control word at -20°C ambient temperature.

(SFDR) versus frequency control word with a 4.6 GHz clock at an ambient temperature of -20°C . The measured SFDR ranges from 20 to 30 dBc. Compared to the theoretical analysis, the degradation of the measured SFDR is due to a combination of effects including the wideband matching of the clock and output signals, nonlinearity associated with the nonlinear DAC, and

TABLE I
ULTRA-HIGH-SPEED DDS PERFORMANCE COMPARISON

Technology f_T/f_{\max} [GHz]	InP 137/267 [1]	InP 300/300 [2]	InP 300/300 [3]	InP 180/266 [4]	TFAST InP 406/423 [4]	SiGe 120/100 [This work]
Emitter area of minimal size transistor [μm^2]	1.5x4	0.4x2	0.4x2	0.5x2	0.25x1	0.2x0.64
Emitter current density at peak f_T [$\text{mA}/\mu\text{m}^2$]	1~1.2	5	5	-	-	6
Peak f_T current of min size transistor [mA]	7.2	4	4	-	-	0.77
Break down voltage BV_{ceo} [V]	8	4	4	-	5	1.8
Accumulator size [bit]	8	8	8	9	9	9
DAC resolution [bit]	7	7	5	-	-	8
Max clock frequency [GHz]	9.2	13	32	8	12	12.3 cooled 9.6 room
SFDR with Nyquist output [dBc]	30	26.67	21.56	38	30	22 @12GHz 27 @10GHz
Power consumption [W]	15	5.42	9.45	7	8	1.9
Transistors number	3000	1646	1891	8695	8800	9600
Die size [mm^2]	8x5	2.7x1.45	2.7x1.45	4x2	-	3x3 chip 2.3x0.7 active
FOM [GHz/W]	0.5	2.4	3.386	1.1	1.5	6.3 cooled 5.05 room Packaged
Test conditions	wafer probe	wafer probe	wafer probe	wafer probe	wafer probe	

noise coupling from the reference line, the substrate and the power supply.

When compared with the InP DDS in [1], which operates at a 9.2 GHz clock frequency, this design achieves similar SFDR performance, yet with much lower power consumption. Most of the InP DDS MMICs were measured using probe stations [2], [3], while this DDS RFIC was tested with packaged parts. Table I compares the recently published mm-wave DDS MMIC performances. The designs reported in [2] and [3] used InP technologies with an f_t/f_{\max} above 300/300 GHz, which is almost triple those reported here. The InP DDS [1] employs an 8-bit accumulator and an 8-bit DAC and operates at a maximum clock frequency of 9.2 GHz with a power consumption of 15 W. On the other hand, this SiGe 9-bit DDS consumes 1.9 W with 3.3 V power supplies for digital and analog circuits, respectively. The 4 V power supply was tied to a pair of pull-up resistors, providing more voltage headroom and output swing for the DAC output stage. The VCO and the DDS are separately powered, and the 1.9 W power consumption does not include the power of the VCO.

As shown in Table I, the minimum transistor size in the InP technology is much larger than SiGe technology. Although the current densities required to achieve peak f_T frequency in InP and SiGe technologies are similar, the current required to operate the minimum transistor close to a peak f_T frequency differs quite a bit, which contributes to the superior power efficiency performance of this SiGe DDS. When compared with the published DDS MMICs, this SiGe DDS achieves the best reported power efficiency FOM of 6.3 GHz/W with a much smaller die size of $2.5 \times 0.7 \text{ mm}^2$.

VII. CONCLUSION

This paper presented a 9-bit 12 GHz 1.9 W SiGe DDS RFIC design with a sine-weighted current-steering DAC. The packaged DDS MMIC achieves a maximum clock frequency of 12.3 GHz with a power consumption of only 1.9 W. At

Nyquist output, the DDS achieves a maximum clock frequency of 11.9 GHz, which corresponds to the best reported power efficiency FOM of 6.3 GHz/W. The SiGe DDS contains more than 9600 active devices with an active area of $2.3 \times 0.7 \text{ mm}^2$.

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Xuefeng Yu received the B.Sc. degree in electrical engineering from Tsinghua University, Beijing, China, in 2000, and the M.Sc. degree from the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China. He is currently pursuing the Ph.D. degree in electrical engineering at Auburn University, Auburn, AL.

His research interest is mm-wave integrated circuits with focus on high-speed D/A and A/D converters.



Fa Foster Dai (M'92–SM'00) received the Ph.D. degree in electrical and computer engineering from Auburn University, Auburn, AL, in 1997 and another Ph.D. degree in electrical engineering from the Pennsylvania State University, University Park, PA, in 1998.

From 1997 to 2000, he was with Hughes Network Systems of Hughes Electronics, Germantown, MD, where he was a Member of Technical Staff in very large scale integration (VLSI), designing analog and digital ICs for wireless and satellite communications.

From 2000 to 2001, he was with YAFO Networks, Hanover, MD, where he was a Technical Manager and a Principal Engineer in VLSI designs, leading high-speed SiGe IC designs for fiber communications. From 2001 to 2002, he was with Cognio Inc., Gaithersburg, MD, designing radio frequency (RF) ICs for integrated multiband wireless transceivers. From 2002 to 2004, he was an RFIC consultant for Cognio Inc. In August 2002, he joined Auburn University, Auburn, AL, as an Associate Professor and was made a Professor in electrical and computer engineering in 2007. His research interests include VLSI circuits for analog, mixed-signal and mm-wave applications, RFIC designs for wireless and broadband networks, ultra-high-frequency synthesis and mixed-signal

built-in self-test (BIST). He is the co-author of *Integrated Circuit Design for High-Speed Frequency Synthesis* (Artech House, 2006).

Dr. Dai served as a Guest Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS in 2001. He is the co-chair of the wireless workshop on Multi-Standard Wireless Transceiver RFIC Designs at 2007 IEEE Symposium on VLSI Circuits. He currently serves on the technical program committees of the IEEE Symposium on VLSI Circuits, the IEEE Custom Integrated Circuits Conference (CICC), the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) and the IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SIRF).



J. David Irwin (S'60–M'63–SM'71–F'82–LF'05) was born in Minneapolis, MN, in 1939. He received the B.E.E. degree from Auburn University, Auburn, AL, in 1961 and the M.S. and Ph.D. degrees from the University of Tennessee at Knoxville in 1962 and 1967, respectively.

He joined Bell Telephone Laboratories in 1967 as a Member of the Technical Staff and was made a Supervisor in 1968. He joined Auburn University in 1969 and became Head of the ECE Department in 1973. He is currently Earle C. Williams Eminent Scholar

and Head.

Dr. Irwin has held numerous positions within the IEEE, including President of both the Education and Industrial Electronics Societies and Editor-in-Chief of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS. He is the author or co-author of numerous publications, including 17 textbooks, and has received several education and technical awards.



Richard C. Jaeger (S'68–M'69–SM'78–F'86) received the B.S. and M.E. degrees in electrical engineering in 1966 and the Ph.D. degree in 1969, all from the University of Florida, Gainesville.

From 1969 to 1979, he was with the IBM Corporation working on precision analog design, integrated injection logic, microprocessor architecture and low-temperature MOS device and circuit behavior. He holds three patents and has received two Invention Achievement Awards from the IBM Corporation. In 1979, he joined Auburn University,

Auburn, AL, where he is now Professor Emeritus of Electrical and Computer Engineering. He was instrumental in founding the Alabama Microelectronics Science and Technology Center in 1984 and served as its Director until 1998. From October 2001 through 2004, he was Interim Director of Auburn University's Wireless Engineering Program and led implementation of Auburn's now accredited Bachelor of Wireless Engineering degrees, a joint effort between the ECE and CSSE departments. He has published over 300 technical papers and articles, served as principal investigator on more than \$8 M in research contracts, and authored or co-authored six textbook editions including the second edition of *Introduction to Microelectronic Fabrication* (Prentice Hall, 2002), the third edition of *Microelectronic Circuit Design* (McGraw-Hill, 2007) with T. N. Blalock, and *Computerized Circuit Analysis Using SPICE Programs* (McGraw-Hill, 1997) with B. M. Wilamowski.

Dr. Jaeger received the 1998 IEEE Education Society McGraw-Hill/Jacob Millman Award for "Development of a Modern and Innovative Design-Oriented Electronic Circuits Text," and the 2004 IEEE Undergraduate Teaching Award for "Excellence In Undergraduate Teaching and Development of Outstanding Textbooks for Courses In Microelectronics." He was a member of the IEEE Solid-State Circuits Council from 1984 to 1991, serving the last two years as Council President. From 1995 to 1998, he was Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He was elected to the IEEE Solid-State Circuits Society Adcom in 1999, and served as its Vice President in 2004–2005 and President in 2006–2007. He was Program Chairman for the 1993 IEEE International Solid-State Circuits Conference, and Chairman of the 1990 VLSI Circuits Symposium. From 1980 to 1982, he served as founding Editor-in-Chief of *IEEE MICRO*, and subsequently received an Outstanding Contribution Award from the IEEE Computer Society for development of that magazine. He was selected as one of the IEEE Computer Society's "Golden Core" and received the IEEE Third Millennium Medal. He was elected Fellow of the IEEE in 1986 and was appointed to the Distinguished University Professorship by Auburn University in 1990. He received the Birdsong Merit Teaching Award from the College of Engineering in 1991. In 1993, he was chosen as the Outstanding EE Faculty Member by the undergraduate students.