A 12-Bit Cryogenic and Radiation-Tolerant Digital-to-Analog Converter for Aerospace Extreme Environment Applications

Yuan Yao, Foster Dai, *Senior Member, IEEE*, Richard C. Jaeger, *Fellow, IEEE*, and John D. Cressler, *Fellow, IEEE*

***Abstract*—This paper presents an 80-MHz 12-bit cryogenic low-power digital-to-analog converter (DAC) implemented in a 0.5-μm SiGe BiCMOS technology. The cryogenic DAC is capable of operating over an ultrawide temperature (UWT) ranging from -180 °C to $+120$ °C and under the high-energy particle radiation environment on the lunar surface. A bandgap voltage reference for the UWT applications is designed using SiGe heterojunction bipolar transistors, and the current-steering DAC is implemented using a segmented current source array. The design considerations for both extreme temperature and radiation environments are discussed. The cryogenic and radiation-tolerant DAC chip occupies a die area of 3.5×1.8 mm^2 and consumes only 39.6 mW from a 3.3-V supply voltage. The maximum DAC sampling rate was measured at 80 MS/s at -180 °C using a 40-pin dual in-line package.**

***Index Terms*—Bandgap reference (BGR), digital-to-analog converter (DAC), radiation tolerance, silicon germanium (SiGe), ultrawide temperature (UWT).**

I. Introduction

With the development of aerospace exploration, the considerations for extreme environments have more comprehensively been included into most designs related to aerospace engineering. The extreme environments, such as temperature, radiation, pressure, and vibration, will easily preclude the use of conventional terrestrial engineering designs for operation, actuation, and movement under ambient conditions. Although the moon is relatively close to the earth and the radiation level there is not too high, the extreme temperature conditions on the lunar surface can still invalidate conventional electronic components and systems for control, sensing, and communication. This is problematic since the development of modular, expandable, and reconfigurable human and robotics systems for lunar missions clearly requires electronic components and integrated packaged electronics modules, which can robustly operate without external thermal control [1].

Manuscript received October 4, 2007; revised April 7, 2008. This work was supported by the NASA Code ESR&T program under Contract NNL05AA7C (ASTP-CCEI 2769).

Y. Yao, F. Dai, and R. C. Jaeger are with the Department of Electrical and Computer Engineering, Auburn University, Auburn, AL 36849-5201 USA (e-mail: yaoyuan@auburn.edu).

J. D. Cressler is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250 USA (e-mail: cressler@ece.gatech.edu).

Digital Object Identifier 10.1109/TIE.2008.924174

Unmanned lunar missions necessitate the combination of the mobility of a rover on the surface with sensing functions, electronics, and actuators for control of the rover. Therefore, the sensing and control modules on the rover, which are usually advanced electronics systems, need not only sense and monitor the performance of the rover to guarantee good operation of the mechanical systems but also successfully accomplish the tasks in scientific experiments and research [2]. Since remote electronics are, in principle, distributed over the entire rover, they cannot efficiently be located within conventional protective "warm boxes." Thus, in order to remove the bulky protective "warm boxes," newly designed electronics systems must robustly operate in extreme environments on the lunar surface, in the ultrawide temperature (UWT) range from -180 °C to $+120$ °C and radiation exposure environment.

To support NASA's goals of robotic missions and manned missions to the Moon before 2020, we have been developing and demonstrating extreme environment electronic components, such as basic digital logic circuits, data converters, voltage controlled oscillator, and other building blocks required for lunar robotic systems with distributed architectures, using commercial SiGe BiCMOS technology. SiGe BiCMOS is a monolithic technology that inherently provides both novel bipolar devices [SiGe heterojunction bipolar transistors (HBTs)] and Si CMOS. Unlike conventional Si transistors, SiGe HBTs are very well suited for operation in the lunar environment [3], [4]. The addition of Ge allows tailoring of the device bandgap, which can be used to optimize device behavior as a function of temperature. SiGe BiCMOS offers unparalleled low-temperature performance, wide temperature capability, and optimal mixed-signal design flexibility at the monolithic level by offering power-efficient high-speed SiGe HBTs and high-density Si CMOS [3]–[6]. The effort of IC development for extreme environment begins with evaluating SiGe BiCMOS devices across temperature and verifying the performance and reliability of circuit designs against system needs for UWT. Circuits are designed and fabricated in commercially available SiGe BiCMOS technology, tested, and then integrated into the packaging technology developed for system prototype delivery.

The digital-to-analog converter (DAC) is a crucial component in modern mixed-signal systems. High-speed high-accuracy DACs are increasingly demanded by many modern communication systems [7]. However, current DACs cannot properly operate when exposed to extreme temperature and radiation environments due to the limits of the characteristics

0278-0046/$25.00 © 2008 IEEE

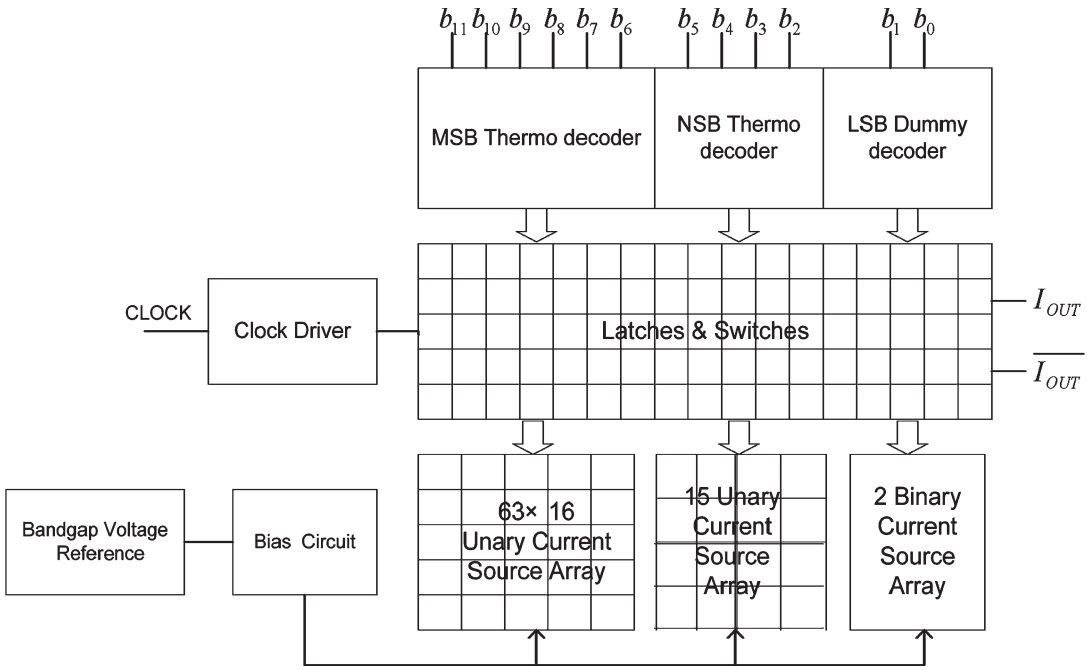


Fig. 1. Block diagram of the proposed cryogenic DAC.

of fabrication material, model accuracy in cryogenic conditions, and design difficulty in the UWT range. Due to the limitations on power, the electronics systems on the rover require low power consumption to provide longer operation time. Thus, there is a need for a specific DAC design that can solve the issues previously discussed, such as extreme temperature environments, radiation exposure conditions, and lower power.

This paper presents a lower power 12-bit current-steering cryogenic DAC design that is capable of operating over the UWT range and under radiation conditions on the lunar surface. This DAC design uses commercial SiGe BiCMOS technology to provide better performance under the cryogenic condition.

The organization of this paper is given as follows: In Section II, the 12-bit DAC architectural and circuit design for cryogenic applications is comprehensively discussed. The discussion includes the circuit structure of building blocks; circuit performance under cryogenic conditions; and design tradeoffs among speed, static and dynamic accuracy, and power consumption. In Section III, radiation effect is discussed to accurately simulate aerospace extreme environments. The measurement results of the DAC chip in the UWT range and radiation environments will be given in Section IV. Section V will present the final conclusions.

II. DAC Architecture and Circuit Design

A. Architectural Design

The current-steering DAC is the most common and almost exclusive type of DAC for high-speed high-resolution applications when compared with other typical DAC architectures [8]–[10]. This architecture provides a good balance between die size, power consumption, accuracy, and dynamic performance.

This on-chip current-steering 12-bit DAC is implemented by using a $6\text{MSB} + 4\text{NSB} + 2\text{LSB}$ segmented current-steering architecture shown in Fig. 1, which includes a thermometer decoder, current switch logic array, segmented current source array, clock driver, and bandgap voltage reference.

The thermometer-coded DAC has advantages over its binary counterpart, such as low differential nonlinearity (DNL), guaranteed monotonicity, and reduced glitch noise. For a 12-bit current-steering DAC, thermometer-coded segmentation for significant bits can be applied to shrink the chip area and reduce the currents through current switches [11], [12]. There are two types of segmentation: full segmentation and partial segmentation. Full segmentation can guarantee good dynamic performance and monotonicity, and reduce glitches, because every level in the DAC has a switch with a reference current connected to this switch. However, full segmentation in high-resolution converters is hard to implement due to worse jitter or time skews at high frequency, larger die size, and increased circuit complexity. For example, in a 12-bit fully segmented DAC, there will be $2^{12} - 1 = 4095$ switches that have to be addressed and switched at very accurate times. Partial segmentation is implemented by combining some segmentation in the most significant bits (MSBs) with a binary weighting for the less significant bits, which can obtain good accuracy and dynamic performance with an acceptable chip area and circuit complexity. Therefore, for the 12-bit DAC design, there is a tradeoff between the segmentation of the significant bits and the effect on layout complexity, glitches, monotonicity, precision, integral nonlinearity (INL), DNL, and speed [13], [14].

Tradeoffs also apply to segmentation, die area, and static INL and DNL performances [11], [15]. Although the digital area is very small without segmentation, extra die area is needed to obtain the required accuracy and linearity. Similarly, when a full segmentation is applied, the total area is still dramatically large due to the exponential increase in digital circuitry. With the determined performance specifications, there is an optimal

range in die area for thermometer-coded segmentation. If we define that the M MSBs are thermometer coded in one cluster, the K LSBs are kept in binary coding, and the $N - M - K$ intermediate bits are also thermometer coded in another separate cluster for the 12-bit DAC, we can choose 6MSB + 4NSB + 2LSB within the optimal range to keep the best balance between minimizing the circuit area of thermometer decoders and optimizing the DAC static and dynamic performances [15].

B. Unit Current Sources and Switches

The proposed 6MSB + 4NSB + 2LSB 12-bit current-steering DAC is implemented as follows: The six MSBs of the digital binary inputs are thermometer decoded to control 63 current sources, each having 16-NSB current weighting, and four thermometer-decoded NSBs to control 15 current sources with unit-NSB current weighting, whereas the remaining two LSBs control two binary-weighted current sources. The output currents of all current sources, which are switched on or off according to the digital input codes, are summed and driven into an external resistive load to generate the required analog output voltage [16].

Since switches need to be turned on or off at the same time, they should clearly be prevented from both being completely off. Otherwise, the voltage potential at the output of the current source will increase to the power supply voltage when both branches are completely shut off, and then the output voltage will return to normal low level when switches are turned on again. In some cases, the current source transistors may also get into the linear operation region and will then have much worse output impedance. Furthermore, this big change in output voltage will cause serious output glitches, which badly affect the DAC dynamic performance, including the signal-to-noise ratio (SNR), spurious free dynamic range (SFDR), and effective number of bits (ENOB). To avoid this problem, we need to ensure that the crossing point for the transfer curve of the differential switch pair cannot simultaneously turn off both transistors. For a p-type FET (PFET) switch pair, the crossing point should be a low voltage to give enough overdrive voltage to open the PFETs. Fig. 2 shows the schematic for the basic current switches used in the DAC, which can realize the required low-voltage crossing point. When CLK arrives, the switch will be turned on or off according to the state of the control signal, which comes from the preceding decoder and will enable or disable the switch based on the digital inputs. During operation, parallel inverters Inv2 and Inv3 simply add a time delay on the order of a nanosecond between the differential switch pair transfer curves. This delay can increase the switch transition time and shift the transfer curve in one branch a little bit off the original high-voltage crossing point to get the desired level. It is also necessary for switching signals to be properly matched to reduce the glitches. Meanwhile, we need to keep the rise and fall behaviors of the switch signals as equal as possible to improve the dynamic performance of the DAC.

To prevent the output signal of the converter from modulating the division accuracy due to channel length modulation, a cascade structure is applied for the current cell circuit. Fig. 3 shows the current source units for four different segmented bit

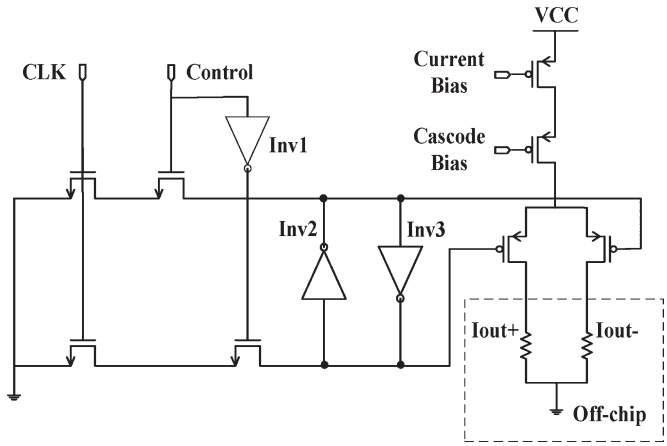


Fig. 2. Schematic of the basic current switch block.

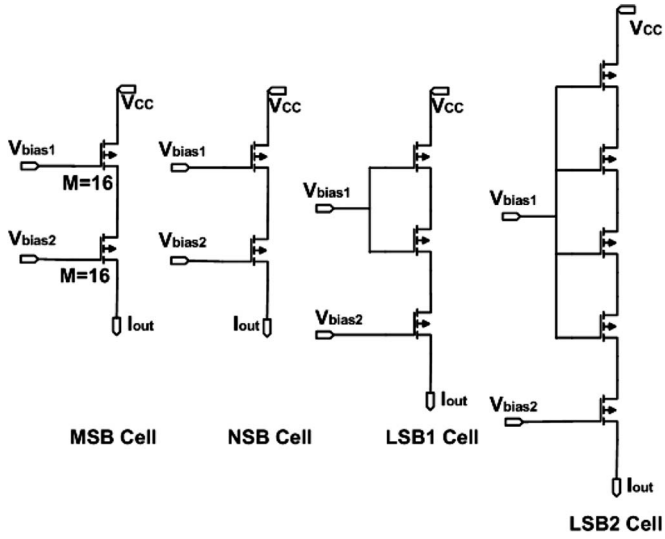


Fig. 3. Current source units for different significant bit cells.

cells: MSB, NSB, LSB1, and LSB2. The current relationship between them is

$$I_{\mathrm{MSB}} = 16I_{\mathrm{NSB}} = 32I_{\mathrm{LSB1}} = 64I_{\mathrm{LSB2}} \tag{1}$$

which corresponds to the segmentation of DAC. In addition, all bit cells are composed of p-channel MOSFETs (PMOSFETs) with the same size to minimize the process mismatch error during fabrication. Precise design and simulation is necessary to make all bit cells operate in the saturation region. Transistors for the NSB current source are set to the basic-size device used in the whole DAC current source array. For the MSB current source, the required 16-times NSB current can be obtained by paralleling 16 unit-size transistors. Due to the channel length modulation, the LSB1 and LSB2 current sources, which are constructed by putting the same basic-size transistors in series, might slightly be smaller than the expected value. Accurate PMOS device size must be obtained through precise postlayout simulation.

For this DAC design, we use PMOSFETs as current sources to achieve high accuracy at the cost of more area. Compared with n-channel MOS (NMOS) devices, PMOSFETs have smaller 1/f noise and do not need additional output pull-up

resistors, which provide convenience and compatibility when cascaded with the following circuits. At the same time, the n-well of the PMOSFETs can effectively eliminate the crosstalk transmitted by the substrate and other noises.

As shown in the DAC architecture for the LSB1 and LSB2 current switch cells, since the LSB D_0 and D_1 input signals are not converted into the thermometer code, there is an apparent delay difference compared with other significant bits. This delay difference will make the MSB and LSB switches asynchronously switched on at high frequency, which consequently causes worse DNL and INL, as well as larger output current error. Therefore, one LSB dummy decoder composing of an even number of inverters is used to remove this effect.

In the current-steering DAC, the impedance $Z_{\rm imp}$ seen in the drain of the switch transistors of each current cell has to be made large enough, so its impact on the INL specification of the DAC can be tolerated [17]. However, $Z_{\rm imp}$ is frequency dependent. The impedance that is required to obtain a certain resolution is approximately equal to

$$Z_{\rm imp} = \frac{NR_L}{4Q} \tag{2}$$

where R_L is the load resistance, N represents the total number of unit current sources, and Q is the ratio between the signal and the second harmonics. To obtain 12-bit output resolution, $Z_{\rm imp}$ has to be about 750 kΩ. When the frequency goes above 80 MHz, cascode current sources are needed to meet the requirement of $Z_{\rm imp}$.

To minimize the systematic error introduced by the voltage drop in the ground lines of the current-source transistors and take account of the increased device current at cryogenic temperature, metal lines widths were chosen based on precise simulation. The maximum delay of the metal wire on chip is approximately 75 ps, and the clock tree is carefully built to ensure an acceptable clock skew.

C. UWT BGR

For a current-steering converter, the static and dynamic characteristics of the DAC such as DNL, INL, SNR, SFDR, and ENOB are very sensitive to the accuracy and stability of the on-chip current reference. Therefore, it is rather critical to design a stable and temperature-independent bandgap reference (BGR) that is capable of operating over the UWT range from -180 °C to $+120$ °C.

The BGR circuit for UWT application is illustrated in Fig. 4. The design utilizes the SiGe HBT transistors to generate the temperature-independent voltage sources. For BJT Q_1 and Q_2,

$$V_{R3} = I_3 R_3 = V_{\rm BE1} - V_{\rm BE2}. \tag{3}$$

Meanwhile,

$$V_{\rm BE1} = V_T \ln\left(\frac{I_1}{I_{s1}}\right) \tag{4}$$

$$V_{\rm BE2} = V_T \ln\left(\frac{I_3}{I_{s2}}\right) \tag{5}$$

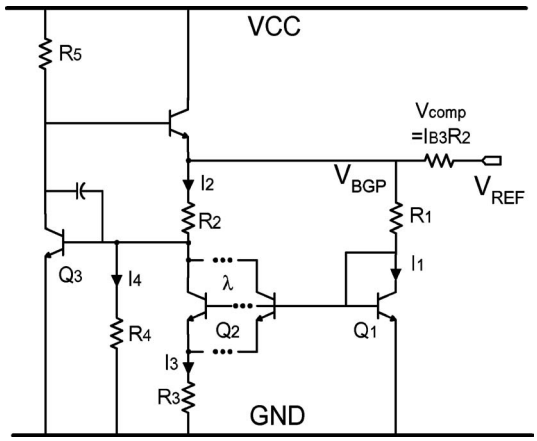


Fig. 4. Schematic of the UWT bandgap voltage reference.

where $V_T = kT/q$. Thus,

$$V_{R3} = I_3 R_3 = V_T \ln\left(\frac{I_1 I_{s2}}{I_3 I_{s1}}\right). \tag{6}$$

If λ is the number of transistors Q_2 in parallel, the current in R_3 is given by

$$I_3 = \frac{V_T}{R_3} \ln\left(\lambda \frac{I_1}{I_3}\right). \tag{7}$$

Thus, the collector current for Q_2 is given by

$$I_{C2} = \frac{\beta}{\beta+1} I_3 = \frac{\beta}{\beta+1} \frac{V_T}{R_3} \ln\left(\lambda \frac{I_1}{I_3}\right). \tag{8}$$

Finally, the BGR voltage at node $V_{\rm BGP}$ can be found as

$$\begin{aligned} V_{\rm BGP} &= V_{\rm BE3} + I_2 R_2 \\ &= V_{\rm BE3} + R_2(I_{B3} + I_{C2} + I_{R4}) \\ &= R_2 I_{B3} + V_{\rm BE3}\left(1 + \frac{R_2}{R_4}\right) \\ &\quad + V_T \frac{\beta}{\beta+1} \frac{R_2}{R_3} \ln\left(\lambda \frac{I_1}{I_3}\right). \end{aligned} \tag{9}$$

As shown in Fig. 4, when using the BGR output to generate a temperature-independent current, a compensating resistor needs to be placed between the bandgap output and the base of the load transistor to compensate the base current drawn by Q_3. This compensation scheme fine-tunes the temperature coefficient of the BGR. Thus,

$$\begin{aligned} V_{\rm REF} &= V_{\rm BGP} - V_{\rm comp} \\ &= V_{\rm BE3}\left(1 + \frac{R_2}{R_4}\right) + V_T \frac{\beta}{\beta+1} \frac{R_2}{R_3} \ln\left(\lambda \frac{I_1}{I_3}\right). \end{aligned} \tag{10}$$

Utilizing the positive temperature coefficient of V_T and the negative temperature dependence of $V_{\rm BE}$ [18], a constant and accurate voltage source over the UWT range can be generated. Furthermore, by changing the ratios of R_2/R_4 and R_2/R_3, we can adjust the coefficients of the negative and positive

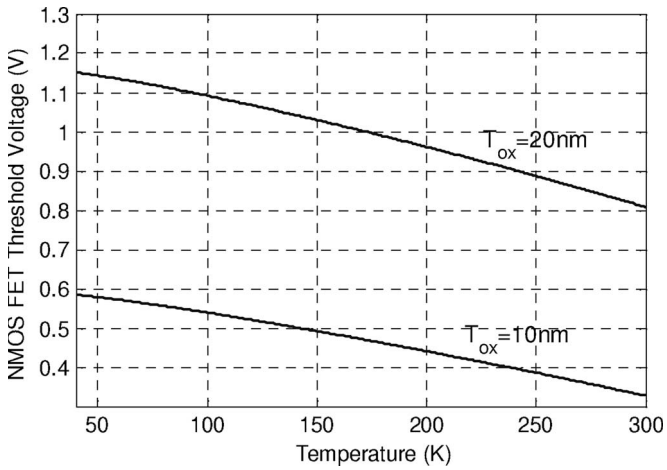


Fig. 5. Simulated NMOS threshold voltage versus temperature.

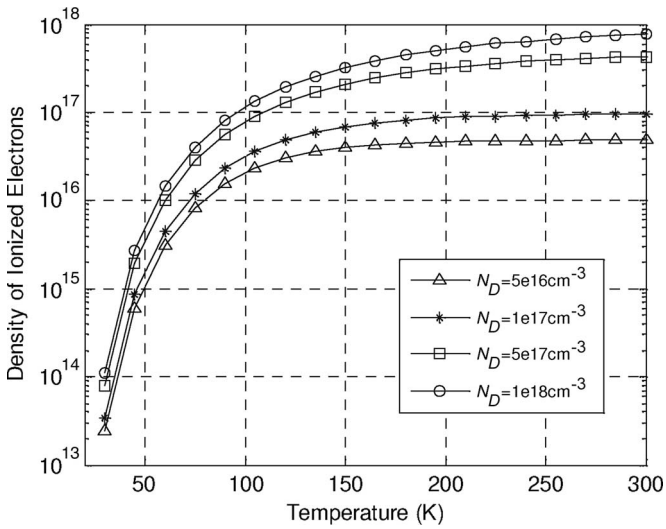


Fig. 6. Simulated density of ionized electrons versus temperature.

temperature terms, respectively, to accomplish the temperature independence for output current or output voltage.

D. Design Considerations for Extreme Environments

At low temperatures, the device characteristics for MOSFETs will differ from those in room temperature. As a result, circuit designs must consider device performance at low temperatures.

1) Current–Voltage Characteristics: When the temperature decreases, the channel conductance of MOSFETs increases [19]. In addition, this increase is quite symmetrical, and this means that the design parameters with which the proposed circuit can properly work in room temperature can also be maintained under low-temperature condition. Therefore, for some digital blocks in the DAC, the design for low-temperature applications can be quite straightforward, just keeping all aspect ratios the same as those in the room temperature design.

2) Threshold Voltage $V_{\rm TH}$: The threshold voltage for MOSFETs can be approximately modeled by [3], [5]

$$V_{\rm TH} = V_{\rm FB} + 2\phi_F + \sqrt{2q \cdot N_A \cdot \varepsilon_{\rm Si} \cdot (2\phi_F + V_{\rm BB})}/C_{\rm ox} \tag{11}$$

where N_A is the acceptor concentration of the well, $V_{\rm FB}$ is the flat-band voltage, $\varepsilon_{\rm Si}$ is the dielectric constant of silicon, $V_{\rm BB}$ is the bulk back bias voltage, $C_{\rm ox}$ is the capacitance of the gate oxide, and ϕ_F is the voltage difference between Fermi potential E_F and intrinsic Fermi potential $E_{\rm Fi}$. For ϕ_F in n-channel MOSFETs (NMOSFETs)

$$\phi_F = kT \ln(N_D/n_i) \tag{12}$$

where N_D is the n-type doping density. Thus, with the decrease of temperature, ϕ_F will be increased. This effect will give rise to an increased $V_{\rm TH}$ when temperature decreases, which also occurs for PMOSFETs. Fig. 5 gives the threshold voltage for NMOSFETs versus temperature for different gate oxide thicknesses.

However, the threshold variation for both transistors is also exactly symmetrical, which means that the thresholds that work well at room temperature will still maintain some of the CMOS digital logic circuit's performance, such as symmetry in rise and fall times and fan-in/fan-out ability [20]. However, higher voltage will be required to keep the device on and maintain the same overdrive capability when compared with room temperature. Extremely low voltage applications at low temperature may significantly be limited by this effect. Careful and complete simulations are needed to ensure the proper operation status at low temperatures.

3) Mobility and Operating Speed: At very low temperatures, freeze-out will result in a decrease in the number of free carriers, as shown in Fig. 6. However, this is compensated by an increase in the mobility of the major carriers. As a result of increased mobility, the working speed of circuits at low temperatures can reach higher frequency.

III. Radiation Tolerance

Due to the lack of atmosphere on the moon, the semiconductor devices working on the lunar surface need to sustain high-energy radiation, as well as extreme-temperature environments. High-energy radiation will dramatically impair the performance of devices and even cause destruction of the devices [21]. The damage suffered by microelectronics mainly comes from three different sources: 1) total dose effect; 2) displacement damage; and 3) single-event effects. For the proposed DAC, the cumulative effects, mainly the total dose effect, will be studied since they are more related to the factors that usually limit the operational lifetime and give rise to the malfunction of the DAC than the transient device performance caused by single-event effects.

The total dose effect will cause most significant damage and performance degradation to the DAC. When an energetic particle such as a proton is passing through an electronic device, it may be trapped and accumulated inside the device, which may dramatically affect device characteristics such as threshold and leakage current, and finally cause the malfunction of the DAC. At the same time, these energetic particles knock silicon atoms out of their proper crystal lattice locations, creating defects in the crystal structure, which appear as wells in the

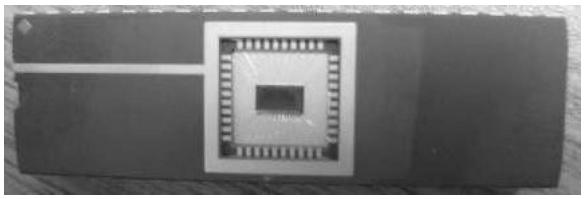


Fig. 7. Forty-pin DIP of the DAC chip.

electrical potential. Those wells trap conduction electrons, increasing the resistance and changing the threshold voltage of the device. This problem is especially important for current-steering DAC, where the output currents are summed up from the precise unit current sources. The radiation causes significant inaccuracy in the unit currents, which inevitably leads to the degradation of the DAC static performance, such as INL and DNL, and its dynamic performance, such as SFDR and ENOB. One possible radiation-tolerant design technique that is suitable for DAC design is to use large W/L transistors. By providing larger switch current, large W/L transistors can overcome the threshold shift and gate oxide capacitance increase caused by radiation trapped holes. Meanwhile, they reduce not only the possibility of device invalidation but also the cumulative change in device characteristics due to total dose effect. Usually, switching transistors with minimum size are chosen to achieve the fastest switching speed with minimum power consumption and to reduce the effect of clock feed-through (CFT). For the cryogenic DAC design, medium-size NMOS with $W/L = 10/1$ μm and three paralleled PMOSs with $W/L = 10/1$ μm are chosen. Moreover, switching transistors with larger size were used for MSB cells in order to lower the voltage across the transistors, which leads to some penalty of increased CFT due to increased gate capacitance.

In order to verify the radiation tolerance of the proposed DAC, different total high-energy proton doses, i.e., 30, 100, and 300 krad(Si), were used to mimic the radiation environments on the lunar surface. In order to mimic the worst-case radiation, the 63.3-MeV protons were directed perpendicular to the bare dies of the DAC with a 7.71-p/cm^2/s rate. No package was used as a protection in the experiment. The measurement results and discussions are presented next in Section IV.

IV. Measurement Result

The proposed cryogenic DAC has been implemented in a 0.5-μm SiGe BiCMOS technology. The package and micrograph photo of the DAC chip are given in Figs. 7 and 8, respectively. The size of the DAC chip is 3.5×1.8 mm^2, including pads. In the layout of the DAC, the current source array and the switches are placed in separate arrays to avoid coupling from the digital signals to the current sources. For aerospace applications, some special layout techniques should be taken into consideration during the whole layout process. To reduce the radiation effect, dummy transistors and duplicate cells are required to provide radiation protection for crucial circuit blocks. With the large W/L transistors and the protection cells, the area for crucial circuit blocks is enlarged, so that the capability of resisting the radiation effects is improved. Guard rings are also

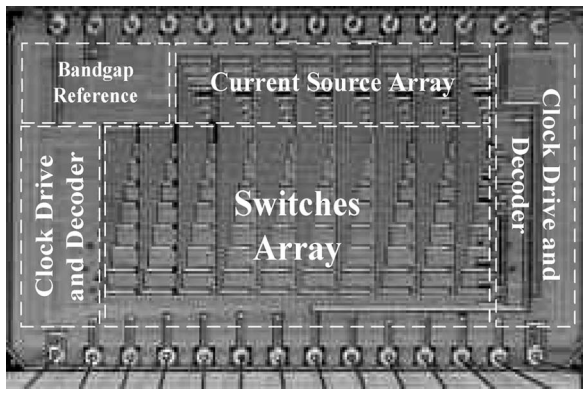


Fig. 8. Micrograph of the 12-bit cryogenic BiCMOS DAC.

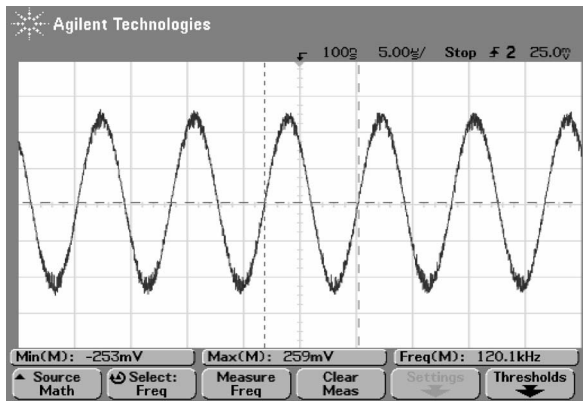


Fig. 9. Measured DAC differential output waveform without deglitch filter for $f_{\rm out} = 121$ kHz and $f_{\rm clock} = 25$ MHz at -180 °C.

used to provide good isolation for the DAC current source array to reduce total dose effect. For increased transconductance and freeze-out effect at very low temperatures, the interconnection metals with larger width should be used to provide margin for larger current conduction such that a sudden current increase will not damage the interconnection wires and invalidate DAC operation.

To test the cryogenic DAC, an air-proof chamber with electrical heating and liquid nitrogen cooling is used. The temperature inside the chamber can be controlled from -180 °C to $+120$ °C. The inputs and outputs of the DAC chip placed into the chamber are connected to a test board outside of the chamber using sub-miniature version A cables. The test board outside of the chamber contains a field-programmable gate array chip for DAC input generation. This test setup guarantees the integrity of input test signals and avoids the damage of the supporting electronic components against the wide temperature variations [22]–[24].

A. Measurements Before Radiation

Fig. 9 gives the measured DAC sinusoidal output waveforms at 121-kHz output frequency with the 25-MHz input sampling clock frequency at a temperature of -180 °C. Fig. 10 shows the measured sinusoid waveform at 625-kHz output frequency with an 80-MHz input sampling clock frequency at room temperature.

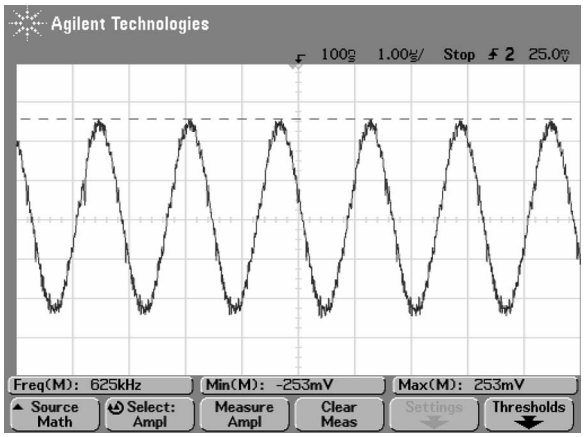


Fig. 10. Measured DAC differential output waveform without deglitch filter for $f_{\rm out} = 625$ kHz and $f_{\rm clock} = 80$ MHz at room temperature.

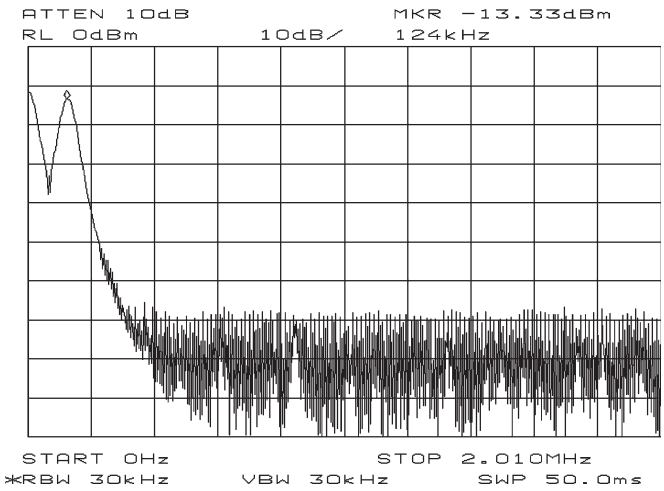


Fig. 11. Measured DAC output spectrum without deglitch filter for $f_{\rm out} =$ 121 kHz and clock $= 25$ MHz at -180 °C.

The SFDR at the 121-kHz output frequency with 25-MHz clock at the temperature of -180 °C is about 54 dBc, as shown in Fig. 11. The spectrum results are measured with only a single-ended output and without a deglitch low-pass filter. The total power consumption at 25 MHz with 3.3-V power supply voltage is 39.6 mW at -180 °C. Fig. 12 shows the measured DAC full-scale output current over the UWT range. The current output at -180 °C is 5.25 mA, and the standard output current is 5.12 mA at 25 °C. Thus, the effective temperature coefficient for the DAC is 97.7 ppm/°C.

Fig. 13 gives the measured 121-kHz output sinusoid waveform with 300-krad(Si) proton radiation dose at the temperature of -180 °C. Fig. 14 also shows the measured 625-kHz output sinusoid waveform with 300-krad(Si) proton radiation dose at room temperature in the same test condition as previously discussed.

B. Measurements After Radiation

With a 300-krad(Si) proton radiation dose, the SFDR at the 121-kHz output frequency with 25-MHz clock at the temperature of -180 °C is about 52 dBc, as shown in Fig. 15. Although there is a slight degradation in the DAC's SFDR

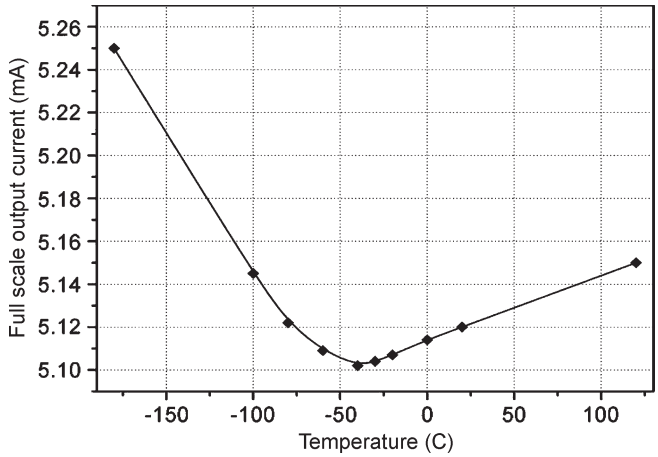


Fig. 12. Measured DAC full-scale output current over the UWT range.

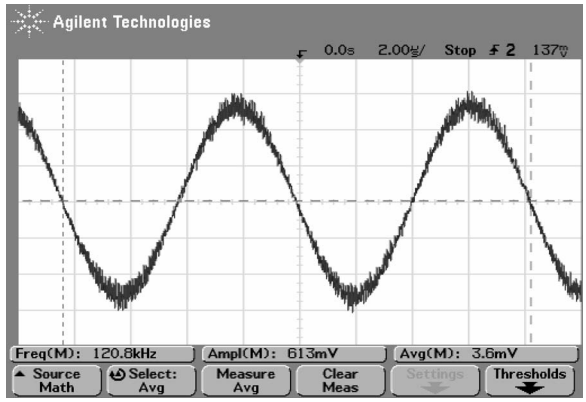


Fig. 13. Measured DAC differential output waveform with 300-krad(Si) proton radiation dose for $f_{\rm out} = 121$ kHz and $f_{\rm clock} = 25$ MHz at -180 °C.

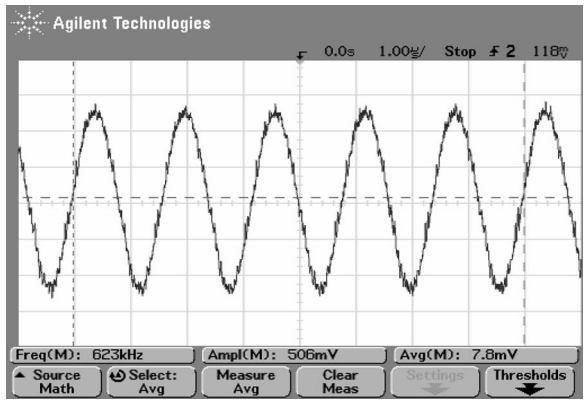


Fig. 14. Measured DAC differential output waveform with 300-krad(Si) proton radiation dose for $f_{\rm out} = 625$ kHz and $f_{\rm clock} = 80$ MHz at room temperature.

performance, which comes from the inaccuracy of unit current sources caused by total dose effect, the DAC still shows good radiation tolerance and robustness to properly operate in extreme environments. Compared to the commercial DAC given in [25], the DAC presented in this paper shows much better performance in extreme-temperature environments and is more appropriate for aerospace extreme environment applications. The total power consumption with a 3.3-V power supply voltage for different temperatures, operating frequencies, and

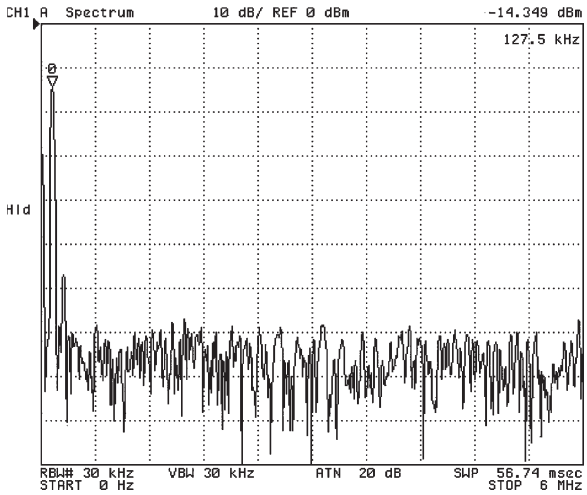


Fig. 15. Measured DAC output spectrum with 300-krad(Si) radiation dose for $f_{\rm out} = 121$ kHz and $f_{\rm clock} = 25$ MHz at -180 °C.

TABLE I
SUMMARY OF MEASURED DAC POWER CONSUMPTION

T (°C) / Dose (Krad(Si))	-180	25	120
0	39.6mW@25MHz 85.8mW@80MHz	39.6mW@25MHz 82.5mW@80MHz	39.6mW@25MHz 84.2mW@80MHz
30	39.6mW@25MHz 87.5mW@80MHz	39.6mW@25MHz 82.5mW@80MHz	39.6mW@25MHz 85.8mW@80MHz
100	46.2mW@25MHz 89.1mW@80MHz	46.2mW@25MHz 85.8mW@80MHz	46.2mW@25MHz 87.5mW@80MHz
300	49.5mW@25MHz 95.7mW@80MHz	46.2mW@25MHz 85.8mW@80MHz	46.2mW@25MHz 89.1mW@80MHz

total radiation doses is listed in Table I. The power consumption at -180 °C is larger than that at $+120$ °C, and both are larger than that at room temperature, which results from the increased unit current at extreme-temperature conditions corresponding to the results shown in Fig. 12. At the same time, the power consumption of the DAC becomes larger with the increase of total radiation dose and the operating frequency. When the DAC works at higher sampling frequencies, the digital circuits are more rapidly switched, which gives rise to larger dynamic power consumption. As for radiation effects, with the increase of total dose, more holes trapped in the oxide induce a threshold voltage shift for PMOS transistors. The additional interface state will degrade both the transconductance and the subthreshold slope, inducing a further threshold shift. The threshold shift and the variation of subthreshold slope will increase the OFF-state leakage current and, consequently, the power consumption of the device. Therefore, the total power consumption will gradually become larger for large total radiation doses when compared with smaller dose cases. Despite being affected by total dose effect, the proposed DAC with design considerations for extreme environments still demonstrates a good radiation-tolerant performance.

TABLE II
SUMMARY OF MEASURED DAC PERFORMANCE

Parameter	Performance
Technology	0.5μm SiGe BiCMOS
Temperature Range	-180°C ~ 120°C
Resolution	12
Conversion Type	Current Steering
Maximal Sampling Frequency	80 MS/s
Differential full-scale output	0.52 V
SFDR without radiation	52dBc@121k,25MS/s 120°C 54dBc@121k,25MS/s -180°C
SFDR with 300Krad(Si) proton dose	51dBc@121k,25MS/s 120°C 52dBc@121k,25MS/s -180°C
Power Supply	3.3 V
Power dissipation	39.6 mW@-180°C@25 MS/s
Die Size	3.5×1.8 mm^2
Package	40 pin DIP

Measurement results have indicated that the proposed cryogenic DAC is capable of operating over the complete range from -180 °C to $+120$ °C. At the same time, good radiation tolerance and robustness of the proposed DAC have also been verified by the postradiation measurements. Therefore, practical applications of this DAC for lunar aerospace exploration are possible. The cryogenic chip was packaged in a 40-pin dual in-line package. Higher operation frequency and better performance could be achieved if a plastic quad flat package with shorter leads had been used. Table II gives a summary of the cryogenic DAC performance.

With verified performance under aerospace extreme environments, the proposed cryogenic radiation-tolerant DAC can be used for resistance sensor system in aerospace industry to accomplish scientific exploration task on lunar surface. Through a Wheatstone bridge, an analog-to digital converter, and other auxiliary circuits, the target resistance value can automatically be obtained by the sensor in a 12-bit digital code. These codes will be sent into a logic block to make digital signal processing. By converting the digital output from the logic block, the DAC provides the bridge with a feedback control signal, which will adjust the bias current and consequently set up different measurement gears for the sensor. The resistance sensor can be applied to measure the temperature characteristics for electronic devices used in aerospace extreme environments. In addition, the DAC can also be widely used in other industrial fields, which need to work under aerospace extreme environments, such as space remote control, satellite communication, and further aerospace exploration.

V. CONCLUSION

In this paper, an 80-MHz 12-bit DAC was implemented in 0.5-μm SiGe BiCMOS technology for aerospace extreme environment applications. The measurement results showed that the proposed DAC is capable of operating over the ultrawide

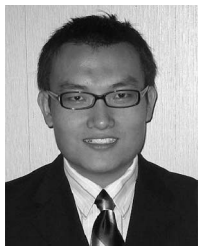
temperature range from the -180 °C to $+120$ °C. Meanwhile, for the aerospace radiation environment, the DAC also shows good radiation tolerance and robustness, which has been verified by the measurement results of three different dose cases. In order to achieve temperature independence, a BGR was designed to provide different segmented current source cells with stable and accurate current over the UWT range. Design considerations for both extreme temperature and aerospace radiation environments have also been discussed. The chip die area is 3.5×1.8 mm^2, and the total power consumption with a 3.3-V power supply is only 39.6 mW at -180 °C and 25-MHz sampling frequency.

ACKNOWLEDGMENT

The authors would like to thank G. Niu, W. Johnson, B. Blalock, M. Mojarradi, M. Palmer, D. Yang, B. Jun, M. Desai, M. Beatty, and the entire SiGe Code T team for their contributions to this paper.

REFERENCES

[1] P. R. Prazak, "A -55 to $+200$ °C 12-bit analog-to-digital converter," *IEEE Trans. Ind. Electron.*, vol. IE-29, no. 2, pp. 118–123, May 1982.
[2] G. Grunwald, G. Schreiber, A. Albu-Schäffer, and G. Hirzinger, "Programming by touch: The different way of human-robot interaction," *IEEE Trans. Ind. Electron.*, vol. 50, no. 4, pp. 659–666, Aug. 2003.
[3] J. D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors*. Norwood, MA: Artech House, 2003.
[4] B. Banerjee *et al.*, "Cryogenic performance of a 200 GHz SiGe HBT technology," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 2003, pp. 171–173.
[5] E. A. Gutierrez-D, M. J. Deen, and C. L. Claeys, *Low Temperature Electronics: Physics, Devices, Circuits and Applications*. San Diego, CA: Academic, 2001.
[6] F. Balestra and G. Ghibaudo, *Device and Circuit Cryogenic Operation for Low Temperature Electronics*. Boston, MA: Kluwer, 2001.
[7] T. Chen and G. Gielen, "The analysis and improvement of a current-steering DAC's dynamic SFDR—II: The output-dependent delay differences," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 2, pp. 268–279, Feb. 2007.
[8] K. O. Andersson and M. Vesterbacka, "Modeling of glitches due to rise/fall asymmetry in current-steering digital-to-analog converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 11, pp. 2265–2275, Nov. 2005.
[9] Y. Cong and R. Geiger, "A 1.5-V 14-bit 100-MS/s self-calibrated DAC," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2051–2060, Dec. 2003.
[10] T. Chen and G. Gielen, "The analysis and improvement of a current-steering DAC's dynamic SFDR—I: The cell-dependent delay differences," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 1, pp. 3–15, Jan. 2006.
[11] R. Van De Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, 2nd ed. Boston, MA: Kluwer, 2003.
[12] Y. Nakamura, T. Miki *et al.*, "A 10-b 70-MS/s CMOS D/A converter," *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp. 637–642, Apr. 1991.
[13] P. Vorenkamp, J. Verdaasdonk, R. Plassche, and D. Scheffer, "A 1 Gs/s, 10 bit digital-to-analog converter," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 1994, pp. 52–53.
[14] S. Haider, S. Banerjee, A. Ghosh, R. Prasad, A. Chatterjee, and S. Kumar Dey, "A 10-bit 80-MSPS 2.5-V 27.65-mW 0.185-mm^2 segmented current steering CMOS DAC," in *Proc. 18th Int. Conf. VLSI Des.*, Jan. 2005, pp. 319–322.
[15] C.-H. Lin and K. Bult, "A 10-b, 500-Msample/s CMOS DAC in 0.6 mm^2," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1948–1958, Dec. 1998.
[16] A. V. D. Bosch, M. A. F. Borremans, M. S. J. Steyaert, and W. Sanse, "A 10-bit 1-GSample/s nyquist current-steering CMOS D/A converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 315–324, Mar. 2001.
[17] A. Van den Bosch, M. Steyaert, and W. Sansen, "SFDR-bandwidth limitations for high speed high resolution current steering CMOS D/A converters," in *Proc. IEEE Int. Conf. Electron., Circuits Syst.*, Sep. 1999, pp. 1193–1196.
[18] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. New York: Wiley, 2001.
[19] A. Hammoud, R. L Patterson, S. Gerber, and M. Elbuluk, "Electronic components and circuits for extreme temperature environments," in *Proc. 10th IEEE Int. Conf. Electron., Circuits Syst.*, 2003, vol. 1, pp. 44–47.
[20] H. Hanamura, M. Aoki, T. Masuhara, O. Minato, Y. Sakai, and T. Hayashida, "Operation of bulk CMOS devices at very low temperature," *IEEE J. Solid-State Circuits*, vol. SSC-21, no. 3, pp. 484–490, Jun. 1986.
[21] J. P. Spratt, G. L. Schnable, and J. D. Standeven, "Impact of the radiation environment on integrated-circuit technology," *IEEE J. Solid-State Circuits*, vol. SSC-5, no. 1, pp. 14–23, Feb. 1970.
[22] J. Qin, C. E. Stroud, and F. F. Dai, "FPGA-based analog functional measurements for adaptive control in mixed-signal systems," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 1885–1897, Aug. 2007.
[23] J. Acero, D. Navarro, L. A. Barraga, I. Garde, J. I. Artigas, and J. M. Burdio, "FPGA-based power measuring for induction heating appliances using sigma–delta A/D conversion," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 1843–1852, Aug. 2007.
[24] E. Monmasson and M. N. Cirstea, "FPGA design methodology for industrial control systems—A review," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 1824–1842, Aug. 2007.
[25] R. Ramesham, N. Kumar, J. Mao, D. Keymeulen, R. S. Zebulum, and A. Stoica, "Data converters performance at extreme temperatures," in *Proc. IEEE Aerosp. Conf.*, Mar. 2006, p. 12.



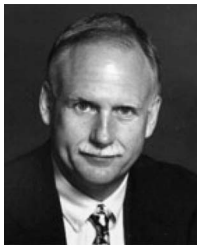
Yuan Yao received the B.S. degree from Fudan University, Shanghai, China, in 2002, and the M.S. degree from the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China, in 2005, both in microelectronics. He is currently working toward the Ph.D. degree in electrical and computer engineering in the Department of Electrical and Computer Engineering, Auburn University, Auburn, AL.

He is currently a Graduate Research Assistant with the Alabama Microelectronics Science and Technology Center, Auburn. His current research interests include analog, mixed-signal, and data conversion integrated circuit design for high-speed and low-power applications.

Foster Dai (M'92–SM'00) received the Ph.D. degree in electrical and computer engineering from Auburn University, Auburn, AL, in 1997, and the Ph.D. degree in electrical engineering from The Pennsylvania State University, University Park, in 1998.

From 1997 to 2000, he was with Hughes Network Systems, Hughes Electronics, Germantown, MD, where he was a member of Technical Staff in very large scale integration (VLSI) and designed analog and digital ICs for wireless and satellite communications. From 2000 to 2001, he was with YAFO Networks, Hanover, MD, where he was a Technical Manager and a Principal Engineer in VLSI designs and led high-speed SiGe IC designs for fiber communications. From 2001 to 2002, he was with Cognio Inc., Gaithersburg, MD, where he designed radio frequency (RF) ICs for integrated multiband wireless transceivers. From 2002 to 2004, he was an RFIC Consultant for Cognio Inc. In August 2002, he joined the Department of Electrical and Computer Engineering, Auburn University, as an Associate Professor and was promoted to Professor of electrical and computer engineering in 2007. He is a coauthor of *Integrated Circuit Design for High-Speed Frequency Synthesis* (Artech House, 2006). His research interests include VLSI circuits for analog, mixed-signal, and millimeter-wave applications, RFIC designs for wireless and broadband networks, ultrahigh frequency synthesis, and mixed-signal built-in self-test.

Dr. Dai has served as a Guest Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS in 2001 and 2008. He was a Cochair of the wireless workshop on *Multi-Standard Wireless Transceiver RFIC Designs* at the 2007 IEEE Symposium on VLSI Circuits. He currently serves on the Technical Program Committees of the IEEE Symposium on VLSI Circuits, the IEEE Custom Integrated Circuits Conference, the IEEE Bipolar/BiCMOS Circuits and Technology Meeting, and the IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF).



Richard C. Jaeger (S'68–M'69–SM'78–F'86) received the B.S. and M.E. degrees in electrical engineering and the Ph.D. degree from the University of Florida, Gainesville, in 1966 and 1969, respectively.

From 1969 to 1979, he was with IBM Corporation, where he worked on precision analog design, integrated injection logic, microprocessor architecture, and low-temperature MOS device and circuit behavior. In 1979, he joined Auburn University, Auburn, AL, where he is currently Professor Emeritus of electrical and computer engineering in the Department of Electrical and Computer Engineering. He was instrumental in founding the Alabama Microelectronics Science and Technology Center in 1984 and served as its Director until 1998. From October 2001 to 2004, he was Interim Director of Auburn University's Wireless Engineering Program and led the implementation of Auburn's now accredited Bachelor of Wireless Engineering degrees, a joint effort between the Department of Electrical and Computer Engineering and Department of Computer Science and Software Engineering. In his spare time, he is an avid amateur radio operator (K4IQJ) who enjoys chasing dx and contest operation. He has published more than 300 technical papers and articles, and has served as principal investigator on more than $8 million in research contracts. He authored or coauthored six textbook editions including the Second Edition of *Introduction to Microelectronic Fabrication* (Prentice-Hall, 2002), the Third Edition of *Microelectronic Circuit Design* (McGraw-Hill, 2007) with T. N. Blalock, and *Computerized Circuit Analysis Using SPICE Programs* (McGraw-Hill, 1997) with B. M. Wilamowski. He is the holder of three patents.

Dr. Jaeger was appointed to the Distinguished University Professorship by Auburn University in 1990. He was a member of the IEEE Solid-State Circuits Council from 1984 to 1991, serving the last two years as Council President. From 1995 to 1998, he was the Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He was elected to the IEEE Solid-State Circuits Society Adcom in 1999 and served as its Vice President from 2004 to 2005 and President from 2006 to 2007. He was the Program Chairman for the 1993 International Solid-State Circuits Conference and the Chairman of the 1990 VLSI Circuits Symposium. From 1980 to 1982, he served as Founding Editor-in-Chief of IEEE MICRO. He was selected as one of the IEEE Computer Society's "Golden Core." In 1993, he was chosen as Outstanding EE Faculty Member by the undergraduate students. He was the recipient of the IEEE Third Millenium Medal from the IEEE Computer Society, the Birdsong Merit Teaching Award from the College of Engineering in 1991, the 1998 IEEE Education Society McGraw-Hill/Jacob Millman Award for "Development of a Modern and Innovative Design-Oriented Electronic Circuits Text," the 2004 IEEE Undergraduate Teaching Award for "Excellence In Undergraduate Teaching and Development of Outstanding Textbooks for Courses In Microelectronics," two Invention Achievement Awards from the IBM Corporation, and the Outstanding Contribution Award from the IEEE Computer Society for the development of IEEE MICRO.

John D. Cressler (S'86–A'91–SM'91–F'01) received the B.S. degree in physics from Georgia Institute of Technology (Georgia Tech), Atlanta, in 1984, and the M.S. and Ph.D. degrees in applied physics from Columbia University, New York, NY, in 1987 and 1990, respectively.

He served on the research staff of the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, from 1984 to 1992, and on the faculty of Auburn University, Auburn, AL, from 1992 to 2002. In 2002, he joined the faculty of the School of Electrical and Computer Engineering, Georgia Tech, where he is currently a Ken Byers Professor of electrical and computer engineering. He has published more than 350 papers related to his research. He is a coauthor (with Guofu Niu) of *Silicon-Germanium Heterojunction Bipolar Transistors* (Artech House, 2003), the author of *Reinventing Teenagers: The Gentle Art of Instilling Character in Our Young People* (Xlibris, 2004), and the Editor of *Silicon Heterostructure Handbook: Materials, Fabrication, Devices, Circuits, and Applications of SiGe and Si Strained-Layer Epitaxy* (CRC Press, 2006). His research interests include Si-based (SiGe/strained-Si) heterostructure devices and technology, mixed-signal circuits and systems built from these devices, extreme environment electronics applications (radiation, low and high temperatures), device-to-circuit interactions, noise and reliability physics, device-level simulation, and compact circuit modeling.

Dr. Cressler was an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS (1998–2001), the IEEE TRANSACTIONS ON NUCLEAR SCIENCE (2002–2005), and the IEEE TRANSACTIONS ON ELECTRON DEVICES (2005–present). He has served on numerous Technical Program Committees, including those of *ISSCC, BCTM, IEDM, Si RF, WOLTE, ISTDM, ISDRS, NSREC, MTT, IRPS*, and *ECS*. He was the Technical Program Chair of the 1998 IEEE International Solid-State Circuits Conference, a Conference Cochair of the 2004 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, and the Technical Program Chair of the 2007 IEEE Nuclear and Space Radiation Effects Conference. He serves as an IEEE Electron Device Society (1994–present) and IEEE Nuclear and Plasma Sciences Society Distinguished Lecturer (2006–present). He was the recipient of the 1994 Office of Naval Research Young Investigator Award for his SiGe research program, the 1996 C. Holmes MacDonald National Outstanding Teacher Award by Eta Kappa Nu, the 1996 Auburn University Alumni Engineering Council Research Award, the 1998 Auburn University Birdsong Merit Teaching Award, the 1999 Auburn University Alumni Undergraduate Teaching Excellence Award, the 2007 Georgia Tech Outstanding Faculty Leadership in the Development of Graduate Students Award, and an IEEE Third Millennium Medal in 2000.