

# A 3-Bit 20GS/s Interleaved Flash Analog-to-Digital Converter in SiGe Technology

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**Abstract** — A 3-bit analog-to-digital converter (ADC) for software defined radio applications that can work at a sampling rate of 20 GS/s is presented in this paper. In order to operate at Ku-band, two flash current mode logic (CML) ADCs are time-interleaved to achieve a 20GHz sampling rate. A 3-bit current-steering digital-to-analog converter (DAC) is also designed for testing the high-speed ADC. The ADC-DAC RFIC is implemented in a 0.12  $\mu\text{m}$  SiGe technology and occupies an area of 1.5 x 1.7  $\text{mm}^2$ . The total power consumption for the entire ADC-DAC chip is 2.36 W with a 4.2 V power supply. The ADC-DAC RFIC is packaged in a 44-pin CLLC package and achieves a peak spurious free dynamic range (SFDR) of 30.5 dBc and a peak effective number of bits (ENOB) of 2.8 bits at a 20 GS/s sampling rate.

## I. INTRODUCTION

With the rapid development of modern communication and personal wireless products, there are increased demands for next generation communication transceivers that feature ultra-high data transmission rates with reconfigurable architectures. Digitizing the received signal at ultra-high frequency instead of baseband frequency will greatly simplify the radio architecture. Moving as many of the radio functions from the RF transceiver IC to the baseband digital chip as possible will improve the radio performance, cut the overall power and, most importantly, allow reconfigurability of the radio designs for multi-band and multi-standard coexistence. In a software defined radio transceiver, as shown in Fig. 1, the received signal will not be down-converted to an inter-mediate frequency (IF) or a baseband frequency. Instead, the received signal will be digitized by an ultra-high speed ADC directly at radio frequency (RF). Thus, mixers and frequency synthesizers that are power hungry and standard related can be eliminated from the RF transceiver. The only blocks needed in the receiver path is a low noise amplifier (LNA) and a variable gain amplifier (VGA), while the transmitter requires only a high-speed DAC, power amplifier (PA) and filter. With all the

benefits a software defined radio can provide, the burden lies upon the design of the ultra-high speed ADC and DAC. Therefore, data converters, especially the ADCs, become the most crucial building blocks for software defined radio designs. ADCs for software defined radio require high linearity, large dynamic range, small area and low power.

Although a 10~20 GS/s 3~4-bit ADC in InP technology [1] and a 40 GS/s 3-bit ADC in SiGe technology [2] have been reported to demonstrate the capability of over 10 GHz sampling speed, their large power consumption and die area prevent them from being integrated in a single chip for software defined radio applications. In this paper, a time-interleaved 3-bit flash ADC with low power consumption and small die area is presented for Ku-band software-defined-radio applications. A high-speed DAC is designed to form a complete data converter pair, which facilitates the ADC testing as well.

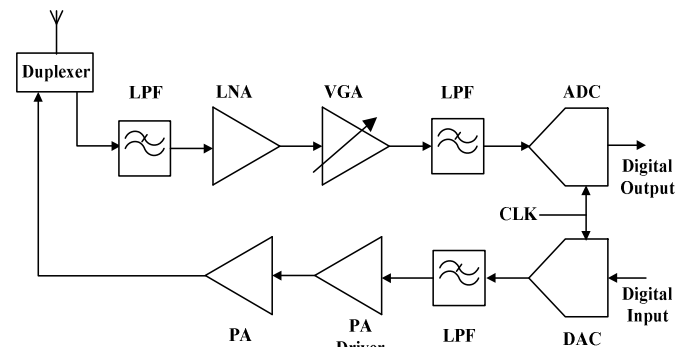


Fig.1 Architecture of the RF front-end for software defined radio transceiver.

The 0.12  $\mu\text{m}$  SiGe HBT technology is featured with a  $f_t/f_{\text{max}}$  of 210/310 GHz. The flash ADC architecture was chosen to achieve the maximum sampling frequency for the ADC design. The current mode logic (CML) circuits are adopted for digital logic implementations to provide fast

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switching speed. Finally, two identical flash ADCs are time-interleaved to double the conversion rate.

The organization of this paper is as follows: in Section II, the 3-bit ADC architecture and circuit design will be discussed. The discussion will mainly include circuit and layout design considerations and trade-offs for ultra-high speed, static and dynamic accuracy, and power consumption. A 3-bit current-steering high speed DAC is also designed for built-in-self-test (BIST) of the ADC function. In Section III, the measurement results of the ADC-DAC chip will be given. Conclusions will be given in Section IV.

## II. ADC-DAC ARCHITECTURE

As shown in Fig. 2, the proposed 3-bit ADC-DAC RFIC is composed of two 3-bit time-interleaved flash ADCs and one 3-bit DAC for ADC testing. Each ADC contains a sample/hold (S/H) amplifier, current comparators, thermometer-to-gray coder and D-flip-flops (DFFs) for retiming and buffer. The outputs of the two ADCs are time-interleaved and combined using a high-speed multiplexer (MUX). In order to obtain the maximum sampling rate, a current-steering DAC is implemented. When ADC-DAC is in operation, the input analog signal is sampled by two S/Hs for both odd and even channel ADCs driven by out-of-phase clocks. The signals after S/H are compared with 7 current-mode comparators which are set with 7 successive offset currents representing the 7 quantization threshold levels. After thermometer-to-gray coder and DFFs, the original analog input signal is converted into digital signals with gray code weight. Due to time-interleaving, the digital outputs in every stage are needed to be multiplexed by a clock signal with double frequency to generate the desired output at the doubled sampling rate. The 3-bit DAC converts the digital signals back to an analog signal that can be tested and measured easily using a digital scope or a spectrum analyzer.

Figure 3 shows the simplified schematic of the differential sample/hold amplifier used in the proposed ADC [3] [4]. As known, the sample/hold amplifier can effectively eliminate the sampling jitters resulting from the phase noise in the sampling clock source and the sampling uncertainty of the ADC. In order to reach the highest operation frequency and improve noise rejection, an open-loop architecture and fully differential structure are employed, respectively. The use of cascode structure in input and output amplifier stages can provide better isolation as well as avoids the breakdown problems of the SiGe HBTs in a 4.2 V power supply. The value of holding capacitor  $C_H$  is designed in the order of several hundred fF to ensure fast charging/discharging and a stable holding voltage at a 20 GS/s rate. In order to achieve better linearity, the product of total bias current and emitter degeneration resistor should be more than twenty times  $V_T$  [5].

Gray code is applied to simplify the coder/decoder logic circuits in order to obtain best speed performance [6]. Employing no more than three input CML cells, gray coder can cut the original four-stage logic (counting one gate and one emitter follower as one stage) to three-stage in the longest signal path of the least significant-bit (LSB), compared to the

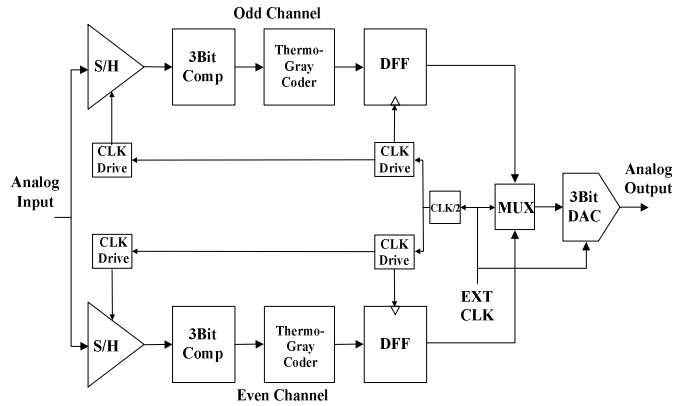


Fig. 2 Simplified block diagram for the proposed 3-bit time-interleaved high-speed flash ADC and DAC.

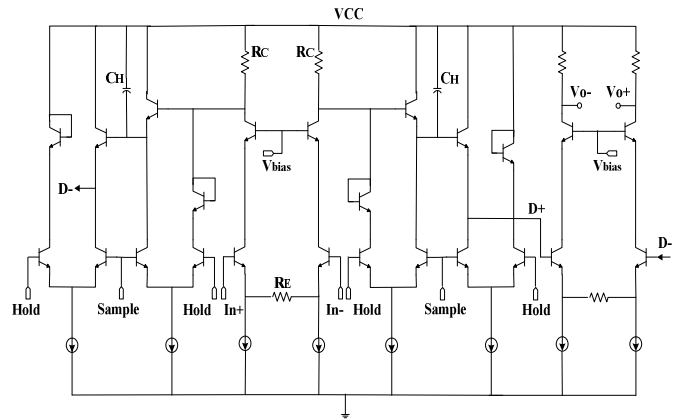


Fig. 3 Smpilified schematic of the differential sample/hold amplifier used in proposed ADC.

traditional binary code. By saving one stage, the compensation circuits for balancing the propagation delay in other signal paths can also be removed so that lower power consumption and higher speed can be simultaneously achieved.

As the key block of the flash type ADC design, current comparators convert the received analog input signal to digital outputs with different quantization threshold levels [2]. The accuracy and speed of the conversion directly affect the static and dynamic performance of the ADC, such as differential nonlinearity (DNL), integral nonlinearity (INL), signal-to-noise (SNR), spurious free dynamic range (SFDR) and effective number of bits (ENOB) etc. Unlike conventional voltage comparators using resistor network to set up the voltage threshold levels, current-mode comparators using active unit current sources can reduce parasitic RC effect in the crucial signal path during the conversion. As illustrated in Fig. 4, the signals coming from S/H are applied to a differential pair that has been optimally biased to realize the fastest switch speed. Meanwhile, pre-offset current which ranges from 0 to 7 unit currents will be added or subtracted from input analog signal at the collectors of the differential pair, based on the analog signal magnitude. The current offsets play the same role as the voltage thresholds in a voltage-mode comparator for quantizing the input signal. To reduce the

headroom lost through the degeneration resistors and to eliminate the mismatch caused by multiple resistors, only one degeneration resistor is used in the current comparators differential pair. Similarly, large bias current and emitter degeneration resistor should be used to increase its linearity range. In addition, the current comparator circuit needs to be redesigned after layout to take into consideration parasitic effects.

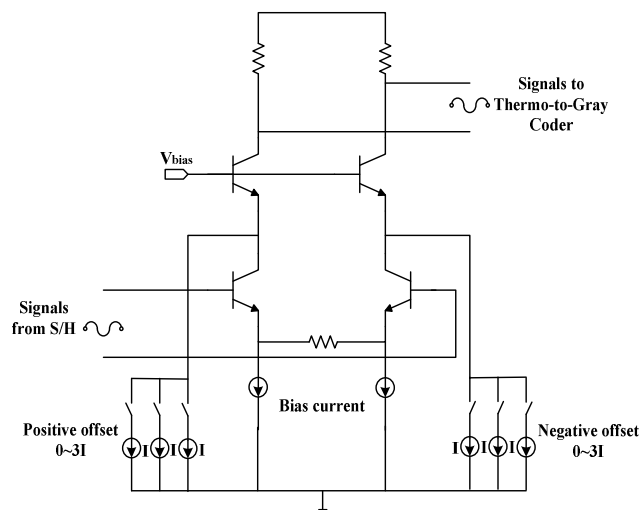


Fig. 4 Current comparator with quantization threshold levels set by the offset current.

### III. MEASUREMENT RESULTS

The 20GS/s 3-bit ADC and DAC were implemented in a  $0.12\ \mu\text{m}$  SiGe BiCMOS technology, as shown in the chip micrograph in Fig. 5. In order to demonstrate the software defined RF receiver, the ADC-DAC chip also includes a 10GHz RF front-end with an LNA and a VGA and a VCO generating the internal clock. The ADC circuit occupies  $1.5 \times 1.7\ \text{mm}^2$  die area and the 3-bit DAC takes an area of  $0.5 \times 1.0\ \text{mm}^2$ . Operating at a 20 GS/s sampling rate with a single 4.2 V power supply, the total power consumption of the ADC and the DAC is 2.36 W.

For Ku-band testing, the PCB test board was developed using a Rogers RO4003 laminate board, which has a loss tangent of less than 0.003 and good temperature stability. To convert the single-ended signal to differential inputs needed to drive the chip, a 180 degree 3dB hybrid coupler is employed at the clock input. For the differential output, another hybrid coupler is inserted into the output path. The ADC/DAC chip is packaged in a 44-pin ceramic leadless chip carrier (CLLC) package. The junction-to-ambient thermal resistance  $\theta_{JA}$  of the ceramic package is about  $40\ ^\circ\text{C}/\text{W}$  with zero air flow. Therefore, the device junction temperature of the ADC/DAC chip could reach above  $100^\circ\text{C}$  at the room ambient temperature with 2.3W power consumption. For this reason, an external fan is used to cool the device during measurements. The  $\theta_{JA}$  of the package is estimated as  $30\ ^\circ\text{C}/\text{W}$  with the fan air flow. All measurements were done using packaged prototypes, while other reported high-speed ADCs were tested

on wafer [2], which has less problems associated with the package heat dissipation and bonding wire effect.

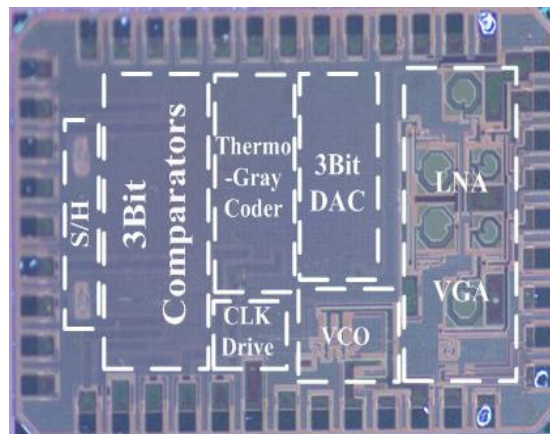


Fig. 5 Microphotograph of the 3-bit time-interleaved 20 GS/s flash ADC and 3-bit DAC chip.

Figure 6 shows the measured 40 MHz sinusoidal time domain waveform reconstructed by the on-chip DAC with a 20 GS/s sampling rate. The 8 step quantization is clearly shown in the waveform without the deglitch low pass filter after the DAC, which verifies the proper operation of both the ADC and the DAC functions. Figure 7 gives the measured DAC output spectrum for a 1.5 GHz ADC input signal at 20 GS/s sampling rate. The Measured SFDR, signal-to-noise-distortion-ratio (SNDR) and ENOB under this condition are 23.2 dBc, 18.6 dBc and 2.8 bits, respectively. It demonstrates a good dynamic performance for the 3-bit ADC-DAC pair.

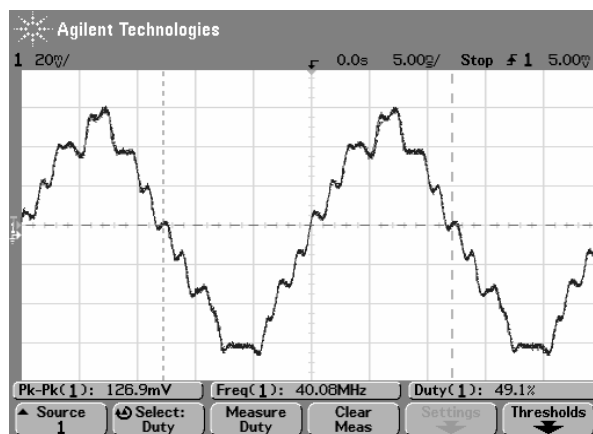


Fig. 6 Measured DAC output waveform showing 8 step quantization of a 40 MHz input signal sampled at 20 GS/s rate.

The measured SFDR for different ADC input frequencies at the maximum sampling rate of 20 GS/s is given in Fig. 9. The maximum dynamic range the implemented ADC-DAC can achieve is 30.5 dBc with a 4.2 GHz ADC input. For larger than 20 dBc SFDR, the ADC achieves an input bandwidth larger than 5.5 GHz. When the ADC input frequency is close

to the Nyquist frequency, the dynamic performance is degraded due to the channel mismatch in odd and even channels of the time-interleaved ADC and the bandwidth limitation of the S/H circuit.

The performance comparison of the 3-bit flash ADCs operating at above 10 GS/s sampling rate is shown in Table I. Note that other reported ADCs except this work were measured by wafer-probe, while this ADC and DAC were tested with packaged chips. Considering the performance degradation due to the package effects, this work demonstrates a good SFDR and ENOB with low power consumption and small die area. As a result, the proposed ADC and DAC provide an efficient means for data conversion in software defined radios.

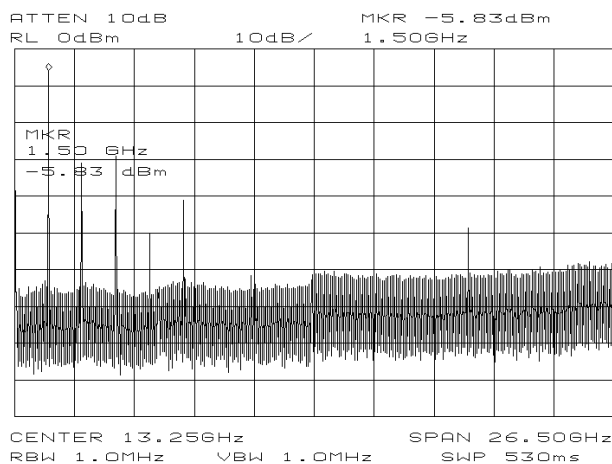


Fig. 7 Measured DAC spectral response for 1.5 GHz input signal at the sampling rate of 20 GS/s.

TABLE. I PERFORMANCE COMPARISON OF ULTRA-HIGH SPEED ADCS.

	[1]	[2]	[7]	This work
Sample Rate (GS/s)	10	40	24	20
SFDR / Input (dBc / GHz)	30.1/6	33/9	25/6	30.5/4.2
ENOB / Input (bits / GHz)	2.8/1	2.8/0.05	2.3/10	2.8/1.5
Power Supply (V)	4	--	-4	4.2
Power (W)	4.25	4.46	3.84	2.36
Technology (- / $f_T$ in GHz)	InP/80	SiGe/210	InP/150	SiGe/210
Die Area (mm <sup>2</sup> )	--	2.2 x 1.8	3 x 3	1.5 x 1.7
Figure of Merit (Power/2 <sup>ENOB</sup> *2*f <sub>s</sub> ) (pJ/step)	30.5	8.0	16.2	8.5
Test Prototypes	Wafer	Wafer	Wafer	Packaged

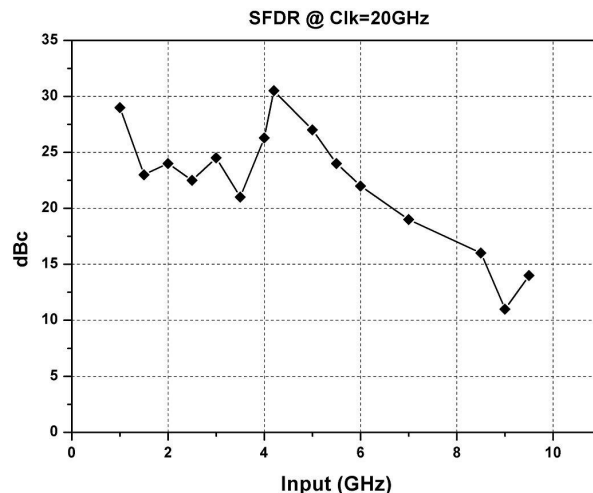


Fig. 9 Measured SFDR for 3-bit ADC-DAC pair as a function of input frequency at the sampling rate of 20 GS/s.

#### IV. CONCLUSION

A 3-bit 20 GS/s time-interleaved flash ADC for software defined radio applications has been implemented in a 0.12 μm SiGe technology. For testing purposes, a 3-bit current-steering DAC is also included on the chip. At the maximum sampling rate of 20 GS/s, the packaged ADC-DAC chip is measured with a peak SFDR of 30.5 dBc at 4.2 GHz ADC input and a peak ENOB of 2.8 bits at 1.5 GHz ADC input. The SiGe ADC consumes 2.36 W power with a 4.2 V supply and occupies a die area of 1.5 x 1.7 mm<sup>2</sup>.

#### ACKNOWLEDGMENT

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