A Novel DC-DC Charge Pump Circuit for Passive RFID Transponder

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Abstract
This paper presents a low-voltage, high-performance charge pump circuit suitable for implementation in standard CMOS technologies. The proposed charge pump has been used as a part of the power supply section of fully integrated passive radio frequency identification (RFID) transponder IC, which has been implemented in a 0.35-um CMOS technology with embedded EEPROM offered by Chartered Semiconductor. The proposed DC/DC charge pump can generate stable output for RFID applications with low power dissipation and high pumping efficiency. The analytical model of the voltage multiplier, the comparison with other charge pumps, the simulation results, and the chip testing results are presented.

Index Terms
DC/DC, charge pump, RFID, CMOS

I. INTRODUCTION

Charge pump circuits are used in applications where voltages higher than the nominal power supply are needed. High voltages are necessary for the programming of nonvolatile memories. For instance, in the mode of writing to the memory of RFID, the DC/DC charge pump circuit converts the DC supply voltage of 1.5V to a voltage of approximately 14V needed for programming the EEPROM[1][2].

II. ARCHITECTURE

In this section, we will describe the design consideration of the DC/DC charge pump. Most DC/DC charge pump designs are based on the circuit proposed by Dickson [3][4]. The Dickson’s charge pump circuit is widely used in the nonvolatile memories for many years, such as EEPROM and flash memories.

A. The Dickson charge pump

In fig.1, a four-stage Dickson charge pump circuit is shown. Two non-overlapping pumping clocks are used, which voltage amplitudes are usually identical to the supply voltage VDD. C1 to C4 are coupling capacitors with the same large enough value, denoted as C later. The gate and drain terminals of NMOSFET’s are connected and operated in saturation if it is on, while all the substrate terminals are grounded. The charges are pushed from left to right. The output voltage of the circuit is

\[ V \approx (\Delta V \times Vt) \times 4 + Vdd \]  

where \( \Delta V \) is the voltage fluctuation at each pumping node. \( \Delta V \) can be expressed as

\[ \Delta V = Vdd \times \frac{C}{C + Cg} \times \frac{T \times I_{load}}{C + Cg} \]  

where \( C, T, \) and \( I_{load} \) stand for the parasitic capacitance associated with each pumping node, the clock period, and the output current loading.

However, for high output generated voltages, the increase in the threshold voltage due to the body effect can significantly reduce the pumping efficiency. It is also known that the circuit performance is limited due to the threshold voltage drop of the NMOS devices and the reverse charge-sharing phenomenon.

In recent years, several modifications of the Dickson’s charge pump circuit have been proposed to solve the output voltage saturation problem. The four-phase pulse charge pump circuit is the favorable style in the market[5]. Nevertheless, this circuit has to use four-phase clock signals to drive it, which is at the cost of complicated control circuits and large power consumption.

B. The NCP2 charge pump

The circuit of NCP2 proposed by [6] is shown in Fig.2. It utilizes CTS (charge transfer switches) to solve the problem...
of body effect by using the next pumping voltages to switch each CTS.

![Fig.2 A four-stage NCP2 charge pump circuit](image)

However, \( V_m \) still unavoidably grows along with the increasing body effect resulted from increasing pumping voltage presented at each terminal of CTS. The circuit of NCP2 proposed by [6] which uses high-voltage clock generator can eliminate the body effect, but it's not used widely because of the complicated high voltage amplitude clock generator circuit. Another problem of NCP2 mainly lies in increased parasitic capacitance at pumping nodes, which reduces the pumping efficiency.

![Fig.3 A four-stage SP charge pump circuit](image)

C. The SP charge pump

The small pump (SP) circuit [7], as shown in Fig.3, utilizes an extra gate bias control circuit. The design concept in SP is two-fold. It uses small pump circuit to control the gates of major pump circuit, which has a better pumping efficiency than NCP2. But the circuit suffers from another two problems. Firstly, the technique to solve the body effect, utilizing the manufacture of floating body of NMOS transistors or triple-well technology, can not be implanted in the normal ASIC process. Secondly, the circuit uses a small pump circuit for gate biasing in main circuit, and this mechanism results in another problem of reverse charge sharing problem.

D. The voltage doubler charge pump

As shown in Fig.4, the proposed charge pump circuit [8] utilizes the cross-connected NMOS, voltage doubler as a pumping stage. The charge transfer from one stage to the next is accomplished by using a pair of PMOS as serial switches (MP). The MOS transistors MS can ensure the wells of the PMOS transistor switches always in the higher voltage between source and drain. However, the charge pump circuit is complicated, and so many transistors used will increase the parasitic capacitances, which can reduce the output voltage gain. In addition, for higher voltage operation, the voltage doubler needs quite large transient charging current at the edge of the clock, which is hard to supply by the former stage AC/DC voltage multiplier in RFID application.

![Fig.4 One stage of the voltage doubler charge pump](image)

![Fig.5 The proposed charge pump circuit](image)

E. The proposed charge pump

The proposed charge pump circuit is implemented in the normal n-well/p-type substrate CMOS 0.35μm process. As shown in Fig.7, the two pumping clocks CLK and CLK1, which is generated by the on-chip oscillator(details omitted), are out-of-phase and have the same voltage amplitude \( V_ab \). PMOS transistors MTi are the main charge transfer parts. NMOS transistors MNi and PMOS transistors MPi are used in this circuit to turn on and turn off completely as charge transfer switches. The operation of the charge pump circuit is explained as follows. When CLK becomes low and CLK1 becomes high, the nodes 2&4 are charged to \( V_2+\Delta V \), \( V_4+\Delta V \) respectively by the couple capacitors \( C_2&C_4 \). The voltages of nodes 1&3 are discharged from \( V_1+\Delta V \), \( V_3+\Delta V \) to \( V_1 \), \( V_3 \) respectively, in which \( V_1+\Delta V \) is equal to \( V_2 \), \( V_3+\Delta V \) is equal to \( V_4 \), and \( V_3+\Delta V \) is equal to \( V_3 \). The PMOS transistor MP turns on, which leads to that the gate voltage of MS is nearly equal to the voltage of node 2.
Then the charge transfer transistor MT2 turns off completely. Meanwhile, the NMOS transistor MN2 turns on, which leads to that the gate voltage of MT2 is nearly equal to the voltage of node 1. Then the charge transfer transistor MT3 turns on completely, and charge is pushed from node 2 to node 3. The analysis of MT4 and MT5 is similar to MT2 and MT3 respectively. On the other hand, when CLK becomes high and CLK1 becomes low, there will be some similar analysis on these charge pumping transistors. So the new charge pump circuit will push the charge only in one direction effectively.

It is possible to use floating-well configuration to eliminate the body effect [9]. However, this design may generate substrate current by floating devices. Another configuration proposed by [10] utilizes some MOS transistors to control the substrate voltage to eliminate the body effect, but meanwhile degrades the pumping gain and needs more setup time. So we adopt the configuration of connecting the substrates to the drains of the PMOS transistors which have the higher voltages than the sources. Proved by the simulation results, the proposed substrate connecting technique has better pumping gain than techniques used in [9] or [10].

III Simulation Results

The simulations were performed with the SPECTRE simulator, using a 0.35-um CMOS technology with embedded EEPROM from Chartered Semiconductor. All the charge pump capacitances (Ci) are 2 pF, and all the output load capacitances (CL) are 20pF. All the simulations were carried out at 20MHz.

The proposed charge pump circuit is compared with the MOS Dickson, NCP2, and SP charge pumps together. Figures 6-9 present the output voltage for different numbers of pumping stages and power supply voltages. The output current loading is 2uA in all cases. From these figures it is obvious that the proposed charge pump circuit presents higher voltage gain when compared with other circuits, for all the power voltage supplies and for any number of pumping stages. In addition, the proposed circuit is much less complicated than SP charge pump, based on better performance.

Figures 8 and 9 indicate that the proposed circuit presents an almost linear behavior with the increase of the number of the pumping capacitors at 1.2V and 0.9V voltage supplies. So it is also suitable for some low voltage applications.
Fig. 11: Simulated output voltages against load current for VDD=1.5V

Fig. 12: Simulated output voltages against load current for VDD=1.2V

Fig. 13: Simulated output voltages against load current for VDD=0.9V

Figures 10-13 show the output voltage for different values of output current. All the charge pumps are using 4 pumping capacitors. For the same output current, the proposed charge pump generates much higher output voltages compared with the other circuits. Moreover, it exhibits smaller output voltage drop for high values of output current. Simulations have also shown that the output voltage of the proposed charge pump is settled in a shorter time period.

IV Fabrication and Measurements

We have implemented the proposed circuit (12 pumping stages) in a 0.35μm CMOS offered by Chartered Semiconductor. The chip picture is shown in Fig. 14.

The testing results have indicated that the presented novel circuit is capable to provide efficient, stable high voltage for EEPROM programming.

V Conclusion

A low-voltage, high performance charge pump circuit is proposed. Theoretical analyses and circuit simulations used for the design optimization have been presented. Simulations have shown that the proposed new charge pump circuit can reduce the threshold voltage drop, eliminate the body effect completely, and then improve the pumping gain. Therefore, the new charge pump circuit can transfer voltage levels more effectively than the other circuits. Proven by the chip testing, the circuit demonstrates the capability of generating stable DC high voltages as the programming voltage for RFID tags.

References