A 5GHz Low Power WLAN Transceiver SiGe RFIC for Personal Communication Terminal Applications

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Abstract — A low-cost low-power single chip WLAN 802.11a transceiver is designed for personal communication terminal and local multimedia data transmission. It has less than 130mA current dissipation, maximal 67dB gain and can be programmed to be 20dB minimal gain. The receiver system noise figure is 6.4dB in high-gain mode.

Index Terms — Personal communication terminal, SiGe RFIC, WLAN 802.11a transceiver.

I. INTRODUCTION

For some personal communication terminal applications, the simple low-cost single chip 802.11a WLAN transceiver is now considered to be employed to perform the local network multimedia data transmission. This transceiver system diagram is shown in Fig.1. The walking IF architecture is chosen because a single Integer-N frequency synthesizer would be enough to supply the whole RF and IF LO frequency. In addition, only one wide-tuning range VCO is needed to cover the 802.11a low and middle band. For few co-users and large data-amount application, less channel are needed. To reduce terminal costs, this system can be designed to use the two of the three bands in 802.11a protocol.

Fig.1 802.11a transceiver system diagram

II. RECEIVER FRONT-END

Receiver front-end includes a differential LNA, an image-rejection filter and a down mixer. The differential LNA has good noise performance and less dependence on the package parameters. Image-rejection filter is constructed with an inductor and two capacitors to remove the 3.2GHz image interfere. RF mixer is also differential structure to interface with differential LNA. Down mixer output goes out of the chip to a SAW filter, which has 1.05GHz center frequency and 30MHz bandwidth and 30dB out-of-band attenuations.

The circuit schematic of the mixer is shown in Fig. 2, which is a typical Gilbert cell with a single-ended input but a differential output. Inductor L_e is used as emitter degeneration to increase the linearity of the mixer while consuming little voltage headroom. When LO is ideal square wave, the mixer’s voltage gain is

$$A_v = \frac{2}{\pi} \frac{R_L}{r_e + j\omega L_e}$$

(1)

Where $R_L$ is the load resistance and $r_e$ is the emitter resistance of Q1 or Q4. Since mixer’s IIP3 is proportional to $GmLE$, $L_e$ should be carefully chosen to compromise between the gain and the IIP3. Noise matching is achieved by selecting the sizes of $L_n$ and the transistors and operating the RF transistors at the current density required for minimum noise figure. Combining with the matching network, $L_n$ also achieves simultaneous noise and power matching [1]. Since the current in the quad switching transistors is decided by the RF transistors below, the current density for peak $f_t$ is achieved by sizing the transistors. In this design, they are 1/6 of the RF transistors. The LO signals are applied to the base of the quad transistors through buffers, so that their amplitude...
can be kept large enough for completely switching. $L_f$ and $C_f$ are tuned on the LO+RF frequency to get rid of the unwanted sideband. The LC tank tuned on the second RF harmonic, acts as an AC current source in the emitter of the input transistor pair [2].

III. TRANSMITTER

A. Transmitter Base-band VGA

Transmitter variable gain attenuates the input signal by 0–30dB with a step size of 3 dB. The fig.3 is the gain cell and the digitally controlled current sources. The receiver variable gain range is 36dB with a step size of 3dB. IQ modulator includes two mixers similar with the receiver IF mixers, which share the resistors and loads[3].

B. Power Amplifier Pre-driver

The power amplifier driver consists of a differential cascade, an emitter follower, and a common-emitter amplifier just like fig.4 shows. It is to drive the 50Ω input of the off-chip power amplifier. The degeneration inductors of the cascade help to match the input of the PA driver, and they also trades gain for linearity as the sizes are increased. The tanks here are resonated at 5.2GHz, and the inductors can provide 35dB image rejection.

IV. INTEGER-N FREQUENCY SYNTHESIZER

Integer-N Frequency Synthesizer is shown in fig.5. It consists of a LC VCO which has a wide linear tuning range from 3.9GHz to 4.258GHz and so can cover the whole 5.15–5.35GHz band. Schematic of VCO is shown in fig.5. PMOS FETs are used so the tank, especially the varactors can be biased at a wider linear range. This VCO...
Fig. 6 Schematic of wide tuning range VCO with AAC also employs an automatic-amplitude-control circuitry which can keep the VCO in current-limit region and alleviate the AM and AM to PM noise. AAC also provides perfect ambient-proof characteristics over process, temperature and frequency variation. The schematic of AAC VCO is shown in fig.6.

An 8-bit programmable multi-modulus divider (MMD) is designed based on the topology of cascaded 2/3 dual-modulus prescaler cell[4]. The divide ratio can be programmed from 256 to 511. But only the 259 to 266 is used, then we can get a RF LO frequency from 4.144 to 4.256GHz, corresponding to a RF frequency range from 5.18GHz to 5.32GHz. The IF LO frequency is a quarter of the RF LO frequency, which is achieved by twice dividing by 2 operations. In this process, the IQ LO signal for IF mixer can also come into being. The PFD is a totally differential structure for symmetric and noise rejection. The CP is differential input and single-ended outputs, its current can be programmed from 200μA to 2.1mA. These currents can be used to adjust the loop gain. The control signal for MMD and programmable CP is given by a SPI data-load digital block.

Fig 7 is the die layout picture of the transceiver system. The die occupies 16mm² areas and with total 48 pads.

Table 1 System specifications:

<table>
<thead>
<tr>
<th>System Spec.</th>
<th>RX High Gain</th>
<th>RX Low Gain</th>
<th>TX High Gain</th>
<th>TX Low Gain</th>
</tr>
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<tbody>
<tr>
<td>Gain</td>
<td>67.1dB</td>
<td>20dB</td>
<td>14.8dB</td>
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<tr>
<td>NF</td>
<td>6.4dB</td>
<td>16.7dB</td>
<td>38.4dB</td>
<td>38.5dB</td>
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<tr>
<td>IIP3</td>
<td>-25.4dBm</td>
<td>5.3dBm</td>
<td>-5dB</td>
<td>3.2dB</td>
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<tr>
<td>Current Consumption</td>
<td>110mA</td>
<td>130mA</td>
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<td></td>
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</table>

VI. CONCLUSION

This paper represents a low-power and low-cost SiGe RFIC WLAN 802.11a transceiver system for personal communication terminal applications. From table 1 we can see that it has low power dissipation, its performances can meets the applications for local high speed data transmission and so can be used in personal communication terminals.

REFERENCES