FPGA-Based Analog Functional Measurements for Adaptive Control in Mixed-Signal Systems

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***Abstract*—A field-programmable-gate-array (FPGA)-based built-in self-test (BIST) approach that is used for adaptive control in mixed-signal systems is presented. It provides the capability to perform accurate analog functional measurements of critical parameters such as the third-order intercept point, frequency amplitude and phase responses, and noise figure. The results of these measurements can then be used to adaptively control the analog circuitry for calibration and compensation. The BIST circuitry consists of a direct digital synthesizer-based test pattern generator and a multiplier/accumulator-based output response analyzer. The BIST approach has been implemented in an FPGA-based mixed-signal system and used for actual analog functional measurements. The BIST measurements agree quite well with the results obtained with the traditional analog test equipment. The proposed BIST circuitry provides a unique means for high-performance adaptive control in mixed-signal systems.**

***Index Terms*—Adaptive control, built-in self-test (BIST), field-programmable gate arrays (FPGAs), mixed-signal testing, noise figure (NF).**

I. Introduction

THE CONCEPT of the adaptive control has been known and studied for decades [1]. The technology is mainly used in industrial systems whose critical parameters vary over time or with environmental variations, such as temperature, external pressure, humidity, etc. Its basic theory is to include an adaptive controller in a time-varying or environmentally sensitive system that can monitor the performance of the system and adjust it accordingly such that the performance variation can be diminished to an acceptable or even negligible level. However, its applications were restricted by the intensive computation that is required for adaptive control algorithms. With the advance of the integrated circuit (IC) technology in recent years, more and more field-programmable gate arrays (FPGAs) are adopted in industrial systems for their ability to be reconfigured in the field to implement a desired function according to real-time demands. The flexibility and calculation capability of an FPGA attracts more people to design and implement adaptive control algorithms in FPGAs [2]–[7].

Although traditionally adaptive control is studied and applied in industrial systems, it can also be well utilized in a mixed-signal electronic system, such as a wireless transceiver that is typically composed of several analog circuit components whose parameters vary greatly due to temperature, supply voltage, and process variations. For example, the wireless transceiver that is mounted in a car may experience an intensive temperature variation from -40 °C to $+120$ °C. Under such an extreme condition, one of the major problems associated with integrated analog filters is the cutoff frequency variation. If the cutoff frequency can be measured in the system, the variation can be compensated using built-in tunable filter designs [8]. Sometimes, a mixed-signal system is required to offer multimode interoperability for multiband and multistandard applications. Adaptive control can also be used in such a system to monitor the analog circuitry and switch it between several modes [8].

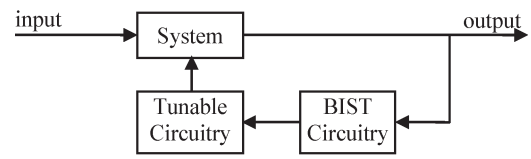

Fig. 1. General model of an adaptive mixed-signal system with BIST technology.

The built-in self-test (BIST) technology provides a system not only the capability to test [9], [10] but also an efficient means for calibrating, compensating, and adjusting the analog circuitry adaptively [8]. It is more than appropriate to be applied in a mixed-signal system with supports for adaptive control. The general model of an adaptive mixed-signal system built with the proposed BIST technology is illustrated in Fig. 1. First, the BIST circuitry captures the system output, through which the critical parameters of the system performance are determined in real time. Then, the built-in tunable circuitry, such as capacitor banks, resistor banks, etc., will be adjusted according to the measurement results, such that the system variations could be compensated correspondingly. For example, if the cutoff frequency of the system deviates from the expected value, another capacitor in the capacitor bank can be activated to stabilize the cutoff frequency. If the linearity of a system is degraded because of the increased interfere or signal strength, the bias current of an amplifier in the system can be adjusted accordingly in the tunable circuitry. However, all in all, the key factor that determines the performance of an adaptive system that is illustrated in Fig. 1 is to accurately measure the functional parameters of the system using the BIST circuitry.

Although it is inevitable that the BIST and tuning circuitry will bring some resource overhead to a system, the cost of added test hardware can be more than compensated for by the benefits of the reliability and the reduced testing and maintenance cost [11]. Furthermore, with FPGAs in the digital portion of a mixed-signal system, the FPGA can be reconfigured with the

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BIST circuitry only when needed for analog test and measurement; otherwise, the normal system function would reside in the FPGA such that there is no area or performance penalty associated with the BIST circuitry.

To perform a suite of analog functionality tests in a BIST environment, such as linearity, frequency response, and noise figure (NF) measurements, the frequency spectrum of the signal coming from the device under test (DUT) needs to be measured and analyzed by an output response analyzer (ORA) included in the BIST circuitry [12]. A few techniques have been proposed to perform on-chip frequency-domain testing of mixed-signal circuits in [13]–[25]. However, all these techniques have their associated problems and disadvantages. For example, [13]–[17] give some simple approaches aimed at decreasing the complexity of the embedded testing circuits, but the precision is limited. The on-chip linear ramp generators in [18]–[22] either depend heavily on additional components or have not experimentally proven their fidelity. The approach in [23], which is based on fast Fourier transform (FFT), introduces considerable area overhead and power consumption to implemented on-chip test and measurement circuitry. While this approach has been successfully implemented in FPGAs, it requires the vast majority of the logic resources in one of the largest and most expensive FPGAs on the market. References [24] and [25] proposed a method to make frequency-domain tests using on-chip generated sine waves and analyzing the results with an on-chip digital signal processor (DSP). However, not only does the approach require 1-bit sigma–delta digital-to-analog converters (DACs) with moderate area overhead, but also, the precision of the generated frequency is not fine enough to support some analog tests such as various analog modulation and linearity tests using precise two tones [8]. Most of these approaches focus only on one or two simple parameter tests such as cutoff frequency of a filter and cannot perform complete analog tests such as frequency response, linearity, noise, and modulation tests [8].

A novel mixed-signal BIST approach has been proposed based on direct digital synthesizer (DDS)-based test pattern generator (TPG) and multiplier/accumulator (MAC)-based ORA [8]. A major merit of DDS is that its output frequency, amplitude, and phase can be precisely and rapidly manipulated under digital control. Other inherent DDS attributes include the ability to tune with extremely fine frequency and phase resolution and to rapidly "hop" between frequencies [26]. Because the signal is in digital form, it is easy to include different modulation capabilities in the DDS. Therefore, many analog functional tests, such as amplitude and phase response in the frequency domain and third-order intercept point (IP3), can be performed using the BIST architecture [8]. Some experimental results for IP3 and frequency response (both phase and amplitude) using this BIST architecture have been presented in [8], [27], and [28] to demonstrate the feasibility and accuracy of the BIST approach.

In this paper, we show how, with some modifications, the proposed BIST approach can be extended from the current suite of IP3 and frequency response functional measurements to include NF measurement of the analog circuitry in any mixed-signal IC or system. For the first time, the BIST for NF measurement is demonstrated for a mixed-signal system. We also address a number of practical implementation issues and considerations. The BIST approach has been implemented in parameterized Verilog, and the resultant synthesized BIST approach is efficient in terms of area overhead and fits in the smallest and least expensive FPGAs in the market. As a result, it can easily be incorporated in any mixed-signal system that incorporates FPGAs, either for permanent residence with the digital system function or only when desired for on-demand test and measurement by in-system reprogramming the FPGA. The paper is organized as follows. An overview of the BIST approach is given in Section II. Section III begins with a brief introduction to frequency response and linearity measurement. Then, the theoretical background of signal-to-noise ratio (SNR) and NF measurements and how they are conducted in the BIST architecture are presented in this section. Experimental results of synthesis and implementation of the BIST circuitry in FPGAs along with actual frequency response and NF measurements made with the resultant hardware are presented in Section IV, including an analysis of the noise introduced by the FPGA and the BIST circuitry.

II. Overview of BIST Approach

A. Basic BIST Architecture

The mixed-signal BIST architecture that is illustrated in Fig. 2 is capable of accurate on-chip analog functional measurements for characterization and compensation of analog circuitry as well as for fault detection [8]. To minimize the area and performance penalty on the analog circuitry, the majority of the BIST circuitry resides in an FPGA in the digital portion of the mixed-signal system. The digital portion of the BIST circuitry includes a DDS-based TPG, a MAC-based ORA, and a test controller. Locating the majority of the BIST circuitry in the digital portion of the mixed-signal system also provides an efficient interface to the BIST circuitry for initiation of test and measurement sequences and retrieval of subsequent results by a processor. The test scheme utilizes the existing DACs and analog-to-digital converters (ADCs) typically associated with most mixed-signal architectures to provide accurate analog testing and measurements while minimizing the hardware added for BIST.

The only test circuitry added to the analog domain is loopback capabilities needed to facilitate one or more return paths for the test signals to the ORA. The number and location of these loopback capabilities determine the accuracy and resolution of tests and measurements associated with a given analog function. For example, in Fig. 2, the multiplexer that is labeled MUX4 facilitates testing and verification of the BIST circuitry prior to its use for test and measurement of the analog circuitry. The incorporation of MUX3 in the analog circuitry allows test and measurement of the DAC/ADC pair prior to test and measurement of the analog DUT. As a result, the effects of the DAC and ADC can be factored out for more accurate measurements of the DUT.

Although the theoretical model of the proposed BIST approach is straightforward, there are a number of practical issues to be considered during implementation. For example,

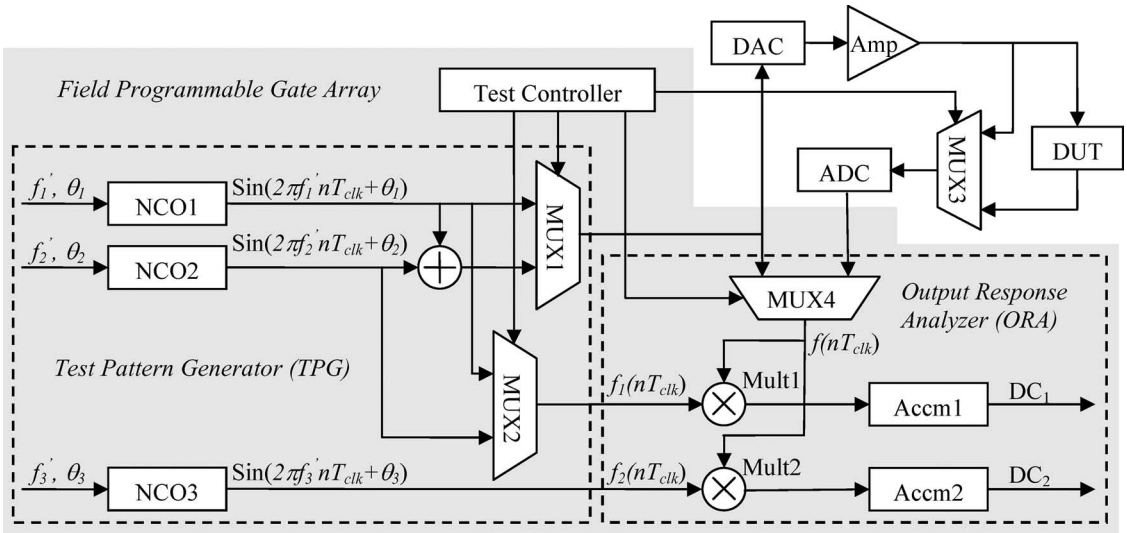

Fig. 2. General model of BIST architecture and implementation in FPGA.

MUX3 must have sufficient bandwidth to pass signal and good R_{on} flatness in the signal variation range. Although MUX3 will affect the DUT's output response in some way, its effect can be cancelled out through calibration. While measuring the DAC/ADC pair for calibration through MUX3, the effect caused by the MUX is already included in that measurement. Therefore, the effort of deembedding DAC/ADC pair will remove the effects of MUX3 as well. Since the ADC/DAC pair provides the communication interface between digital and analog circuitry, their resolution and speed determine the performance of the overall system as well as the BIST system. An ADC or DAC will always generate some quantization noise. When sampling (or synthesizing) a full-scale sine wave with an N-bit ADC (or DAC), the theoretical signal-to-quantization noise ratio can be shown to be $6.02N + 3\log_2(OSR) + 1.76$, where OSR is the oversampling ratio [29]. Therefore, the higher the resolution of the ADC/DAC pair, the cleaner the signal, and hence, better performance can be achieved by both the system and the measurements obtained with the BIST circuitry. However, a high-resolution ADC/DAC usually costs more, consumes more power, runs at lower speed, and, in the case of the BIST approach, requires larger MAC. As a result, there are tradeoffs to be considered while choosing the word length of the ADC/DAC pair. For example, the ADC/DAC pair may be measured beforehand to see if the pair satisfies the requirement, as will be discussed in Section IV-A.

The area and power consumptions of the proposed BIST scheme depend on the resolution of the converters. For high-resolution BIST scheme, sigma–delta modulation can be applied to reduce the DDS area and power consumption [37].

B. TPG Operation Principal

The DDS-based TPG consists of three numerically controlled oscillators (NCOs) and utilizes the existing DAC from the mixed-signal system to complete the DDS. Fig. 3 shows a more detailed view of the NCO used in the TPG. The phase accumulator is used to generate the phase word based on the

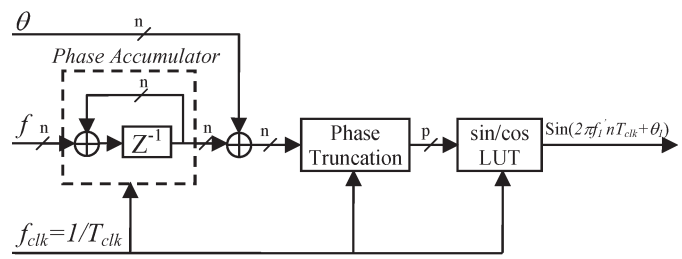

Fig. 3. NCO used in TPG.

frequency word f and the initial phase word θ. Then, the NCO utilizes a lookup table (LUT) to convert the truncated phase word sequence to a digital sine-wave sequence, as shown in Fig. 3. The output sine-wave frequency is determined as

$$f' = \frac{f \cdot f_{\text{clk}}}{2^n} \tag{1}$$

where n is the word width of the phase accumulator. The BIST system that is shown in Fig. 2 requires three NCOs to generate three test tones. To save the die area, the sine LUT of three NCOs can be shared by time multiplexing the LUT input and output. Thus, three NCOs contain only three phase accumulators and one sine LUT. Note that the sine LUT consumes the majority of the NCO area. The phase truncation noise introduced in the NCO can be further reduced using a sigma–delta modulator (SDM) [27]. In addition, the SDM can also be used to reduce the LUT size, leading to a compact DDS design for low-cost BIST applications [37].

The ORA consists of two sets of $N \times N$-bit multiplier and $2N + M$-bit accumulator pairs, with each MAC performing in-phase and out-of-phase analysis, respectively. In the design of the ORA, N is the number of bits from the DDS and ADC, and M is chosen such that $2^n \leq K \leq 2^M$, where K is the length of the BIST sequence in clock cycles and n is the number of bits of the frequency word to the NCO. A more detailed description of how the ORA works is given in the following section.

C. ORA Operation Principal

While performing frequency response, linearity, and NF measurements, $f_1(nT_{\rm clk})$ and $f_2(nT_{\rm clk})$ (refer to Fig. 2) are set to $\cos(\omega nT_{\rm clk})$ and $\sin(\omega nT_{\rm clk})$, respectively. As a result, the DC_1 and DC_2 accumulator values can be described as

$$\mathrm{DC}_1 = \sum_n f(nT_{\rm clk}) \cdot \cos(\omega nT_{\rm clk}) \tag{2}$$

$$\mathrm{DC}_2 = \sum_n f(nT_{\rm clk}) \cdot \sin(\omega nT_{\rm clk}). \tag{3}$$

From (2) and (3), it can be seen that DC_1 and DC_2 are actually the in-phase and out-of-phase components, respectively, of the DUT's output response $f(nT_{\rm clk})$ at frequency ω. Also, the signal $f(nT_{\rm clk})$'s Fourier transform $F(\omega)$ can be expressed through DC_1 and DC_2 according to the following formula:

$$F(\omega) = \sum_n f(nT_{\rm clk}) \cdot e^{-j\omega nT_{\rm clk}} = \mathrm{DC}_1(\omega) - j \cdot \mathrm{DC}_2(\omega). \tag{4}$$

From (4), the signal $f(nT_{\rm clk})$'s frequency spectrum $F(\omega)$ within the bandwidth can be measured through DC_1 and DC_2 by sweeping the frequency ω over the bandwidth of interest. However, in comparison with the FFT algorithm, which computes $F(\omega)$ over the whole frequency domain simultaneously, the MAC-based ORA configuration in Fig. 2 only measures $F(\omega)$ at one frequency point at a time, with the entire frequency spectrum obtained through successive measurements.

From the aforementioned complex function $F(\omega)$, the amplitude $A(\omega)$ and the phase $\Delta\phi(\omega)$ of the spectrum $F(\omega)$ can be derived as follows:

$$F(\omega) = \mathrm{DC}_1(\omega) - j \cdot \mathrm{DC}_2(\omega) = A(\omega)e^{j\Delta\phi(\omega)} \tag{5}$$

where

$$\Delta\phi(\omega) = -tg^{-1}\frac{\mathrm{DC}_2(\omega)}{\mathrm{DC}_1(\omega)} \tag{6}$$

$$\begin{aligned} A(\omega) &= F(\omega)e^{-j\Delta\phi(\omega)} \\ &= \sum_n f(nT_{\rm clk}) \cdot e^{j[\omega nT_{\rm clk} - \Delta\phi(\omega)]} \\ &= \sum_n f(nT_{\rm clk}) \cdot \cos\left(\omega nT_{\rm clk} - \Delta\phi(\omega)\right) \end{aligned} \tag{7}$$

or

$$\begin{aligned} A(\omega) &= -j \cdot F(\omega)e^{j\left(\frac{\pi}{2} - \Delta\phi(\omega)\right)} \\ &= -j \cdot \sum_n f(nT_{\rm clk}) \cdot e^{j\left[\frac{\pi}{2} + \omega nT_{\rm clk} - \Delta\phi(\omega)\right]} \\ &= \sum_n f(nT_{\rm clk}) \cdot \sin\left(\frac{\pi}{2} + \omega nT_{\rm clk} - \Delta\phi(\omega)\right). \end{aligned} \tag{8}$$

The amplitude and phase parameters are used widely in functional measurements of analog circuits. The amplitude response $A(\omega)$ is of interest to functional measurements because many important parameters, such as cutoff frequency, in-band ripple, bandwidth, NF, etc., are determined by it. The phase variation versus frequency $\Delta\phi(\omega)$ is also called *group delay*, which can be used to describe the phase delay introduced by electrical devices. It is the phase delay that causes a phase difference between the external path through the DUT and the internal path from the TPG to the ORA (refer to Fig. 2).

TABLE I
RELATIONSHIP BETWEEN $\Delta\phi(\omega)$ AND $\Delta\phi_o(\omega)$

	$\lvert\mathrm{DC}_1\rvert \geq \lvert\mathrm{DC}_2\rvert$	$\lvert\mathrm{DC}_1\rvert \leq \lvert\mathrm{DC}_2\rvert$
$\mathrm{DC}_1>0$; $\mathrm{DC}_2>0$	$\Delta\phi(\omega)=\Delta\phi_o(\omega)$	$\Delta\phi(\omega)=90°-\Delta\phi_o(\omega)$
$\mathrm{DC}_1>0$; $\mathrm{DC}_2<0$	$\Delta\phi(\omega)=360°-\Delta\phi_o(\omega)$	$\Delta\phi(\omega)=270°+\Delta\phi_o(\omega)$
$\mathrm{DC}_1<0$; $\mathrm{DC}_2>0$	$\Delta\phi(\omega)=180°-\Delta\phi_o(\omega)$	$\Delta\phi(\omega)=90°+\Delta\phi_o(\omega)$
$\mathrm{DC}_1<0$; $\mathrm{DC}_2<0$	$\Delta\phi(\omega)=180°+\Delta\phi_o(\omega)$	$\Delta\phi(\omega)=270°-\Delta\phi_o(\omega)$

The phase delay is an important issue to the MAC-based ORA because it will affect the accuracy and implementation of the BIST approach. Once the phase retardation $\Delta\phi(\omega)$ is identified based on (6), $A(\omega)$ can be measured through DC_2 or DC_1 according to (7) or (8) if the test tone generated by NCO can be phase adjusted using $\Delta\phi(\omega)$ or $\pi/2 - \Delta\phi(\omega)$. However, once we have obtained $\Delta\phi(\omega)$ from (6), we can also correct the measured amplitude $A(\omega)$ as follows:

$$A(\omega) = \frac{\mathrm{DC}_1}{\cos\,\Delta\phi(\omega)} = \frac{\mathrm{DC}_2}{\sin\,\Delta\phi(\omega)}. \tag{9}$$

Therefore, the technique not only measures the phase difference but also facilitates correction of the amplitude measurement based on the phase difference. This ensures the accuracy of the proposed BIST scheme for linearity, frequency response, and SNR measurements. Accurate measurement of the phase delay is therefore critical to the functionality measurements made by the MAC-based ORA.

For an on-chip test, we do not have to set up a full-length *arctangent* LUT to get the exact phase delay from DC_1 and DC_2. First, the quadrant of $\Delta\phi(\omega)$ can be determined easily from the sign bits of DC_1 and DC_2. Before further discussions, we define the absolute phase offset of $\Delta\phi_o(\omega)$ in the corresponding quadrant to simplify the analysis. The absolute phase offset $\Delta\phi_o(\omega)$ can be calculated through the formula as

$$\Delta\phi_o(\omega) = \begin{cases} -tg^{-1}\dfrac{\lvert\mathrm{DC}_2(\omega)\rvert}{\lvert\mathrm{DC}_1(\omega)\rvert}, & \lvert\mathrm{DC}_1(\omega)\rvert \geq \lvert\mathrm{DC}_2(\omega)\rvert \\ -tg^{-1}\dfrac{\lvert\mathrm{DC}_1(\omega)\rvert}{\lvert\mathrm{DC}_2(\omega)\rvert}, & \lvert\mathrm{DC}_1(\omega)\rvert \geq \lvert\mathrm{DC}_2(\omega)\rvert \end{cases}. \tag{10}$$

From (10), we can determine that the value range of $\Delta\phi(\omega)$ varies from 0° to 45°. Also, the relationship between the phase delay $\Delta\phi(\omega)$ and the absolute phase offset $\Delta\phi_o(\omega)$ can be summarized in Table I.

Therefore, $\Delta\phi(\omega)$ can be identified with $\Delta\phi_o(\omega)$ whose value range is [0°, 45°]. Upon the analysis until now, the *arctangent* LUT can be decreased by half. However, when $\mathrm{DC}_2/\mathrm{DC}_1$ is very small, $\arctan(\mathrm{DC}_2/\mathrm{DC}_1)$ can be represented by the ratio of $(\mathrm{DC}_2/\mathrm{DC}_1)$. Thus, the length of the *arctangent* LUT can be compressed further such that the hardware resources used by the phase calculation can be minimized while keeping the calculation result precise enough.

As implied previously in this paper, there are different techniques for compensating for the phase delay to prevent seriously degrading the accuracy of the amplitude measurement.

1) *Approach 1:* Adjust the phase of the outgoing test tone in the NCO such that the DUT output response is in-phase with the NCO tone to be multiplied in the ORA, and then, perform the amplitude measurement according to (7) or (8).
2) *Approach 2:* Calculate the corrected amplitude directly according to (4).
3) *Approach 3:* Obtain the amplitude directly from DC_1 and DC_2 without a phase delay measurement as follows:

$$A(\omega) = \sqrt{\mathrm{DC}_1^2 + \mathrm{DC}_2^2}. \tag{11}$$

Each of these three approaches has advantages and disadvantages. The most attractive merit of first approach is that it does not require any extra circuitry to calculate the amplitude once the phase delay is identified. Such a simple hardware implementation is desired in a good BIST strategy. However, there are also some disadvantages associated with this approach. First, an extra accumulation cycle is required to obtain the amplitude response, which increases the processing time. Second, this approach cannot be used for NF measurement. In the linearity and frequency response measurements, all the signals under analysis by the ORA are deterministic signals, namely the phase delay is a constant. Once the phase delay is identified in one accumulation cycle, the phase delay can be used in the subsequent accumulation cycle. However, the situation differs in the NF measurement. Usually, the noise in electric devices can be modeled as a white Gaussian noise process whose phase also varies from time to time and must be viewed as a random variable. In other words, the phase delay keeps changing in different accumulation cycles. Therefore, the NF measurement cannot be performed with (7) and (8).

The second approach can perform the phase and amplitude measurement almost simultaneously. Also, it does not have the constraints that the first approach does for the NF measurement. However, extra hardware to realize the division and sinusoidal operation in (9) is required in this approach.

There is one common point between the first two approaches in that the amplitude is calculated based on the phase delay obtained beforehand. If there is any calculation error in the phase delay, the error will be introduced into the calculation of amplitude and degrade the precision. The third approach does not have this drawback because the amplitude and phase are calculated independently according to (6) and (11), but the cost is the extra hardware to implement the square and square root operations.

The advantages and disadvantages of these three approaches are summarized in Table II. The bold entries in the table represent the desired properties for an ideal ORA implementation. As can be seen, the third approach is the preferred strategy and used in the ORA implementation. The only drawback of this approach is the extra hardware introduced by the square root operation. Because the amplitude is usually measured and evaluated in the unit of decibels in real-life applications,

TABLE II
SUMMARY OF THE THREE APPROACHES

Approach	#1	#2	#3
hardware overhead	**Low**	high	high
speed	Low	**high**	**high**
constraints	Cannot be used for NF measurement.	**no**	**no**
propagation error	Yes	yes	**no**

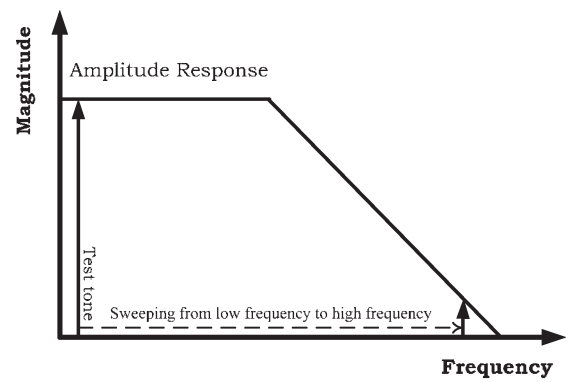

Fig. 4. Frequency response measurement by BIST.

the calculation of (11) can be transformed to the logarithm domain as

$$A'(\omega) = 20\,\log_{10}\left(A(w)\right) = \frac{10}{\log_2 10}\log_2\left(\mathrm{DC}_1^2 + \mathrm{DC}_2^2\right) \tag{12}$$

where $A'(\omega)$ is the measured amplitude in decibel units. The hardware implementation of (12) can be done with a LUT or a simple linear approximation algorithm [30] depending on the precision requirement.

III. Analog Functional Measurements

As presented in [8], [27], and [28], the actual BIST implementation proved the feasibility of the proposed architecture to perform linearity and frequency response measurements and showed experimental results that are very close to the results measured with external test equipment. An overview of how these measurements are conducted in the BIST circuitry is given here.

A. Frequency Response Measurement

When performing the frequency response measurement, NCO1 generates an in-phase digital sinusoidal wave at the frequency ω (refer to Fig. 2), which is then converted to a test tone by the DAC to drive the DUT. At the same time, NCO3 generates an out-of-phase sinusoidal wave with same frequency. The two waves are fed into the ORA as $f_1(nT_{\mathrm{clk}})$ and $f_2(nT_{\mathrm{clk}})$, respectively, and used to calculate the amplitude and phase response of the DUT at this frequency point. By sweeping the frequency ω over the frequency band of interest, as illustrated in Fig. 4, the frequency response of the DUT over the band of interest can be obtained.

B. Linearity Measurement

Linearity is normally measured by the IP3 using a two-tone test [8], [27]. During an IP3 measurement, the DUT is driven by a two-tone test signal $A\cos(\omega_1 t) + A\cos(\omega_2 t)$. The output coming from the DUT is analyzed at frequencies ω_2 and $2\omega_2 - \omega_1$ by the ORA, and fundamental and IM3 terms are obtained as

$$\text{fundamental term} \approx \frac{1}{2}A^2\alpha_1 \tag{13}$$

$$\text{IM3 term} = \frac{3}{8}A^4\alpha_3. \tag{14}$$

Expressing these two terms in decibels, the difference ΔP can be determined, and the input-referred IP3 (IIP3) can be calculated by

$$\text{IIP}_3\ [\text{dBm}] = \frac{\Delta P\ [\text{dB}]}{2} + P_{\text{in}}\ [\text{dBm}]. \tag{15}$$

C. NF Measurement

NF measurement is an important analog functionality test along with the IP3 and frequency response measurements. Noise introduced by an analog circuitry includes thermal noise, shot noise, flicker noise, etc. [10]. Those noises will be mixed together with the interested signal. The more the noise that is introduced by circuit components, the more difficult it is to extract the interested signal. Therefore, the noise is a critical issue to any electrical system's performance. For example, consider the low-noise amplifier (LNA) widely used in RF communication systems. Since an LNA locates in the first stage of the receive path, its noise will be magnified by the gain of the following stages and dominates the noise performance of the overall system. Therefore, the noise introduced by the LNA must be well controlled to guarantee the overall system performance. Because the noise is such a key issue to a system, it is important to include NF measurement in the BIST approach. If the noise introduced by critical components like LNAs can be measured in the system, it will be much easier for IC and system manufacturers to test and diagnose potential problems related to noise in mixed-signal systems. The proposed BIST approach also provides a unique means to adaptively tune the LNA circuitry (e.g., its bias current) for compensation of the performance variations.

There are two important parameters widely used to characterize the system noise. One is the SNR, which is defined as

$$\text{SNR} = \frac{\text{signal power}}{\text{noise power in interested bandwidth}}. \tag{16}$$

Alternatively, the noise added in a circuit can be characterized using the NF, which is defined as

$$\text{NF} = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} \tag{17}$$

where SNR_{in} and SNR_{out} are the SNRs measured at the input and output of the DUT, respectively [27].

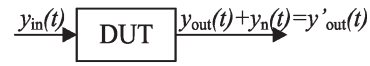

Fig. 5. Noise introduced by DUT.

The noise introduced by a DUT can be mathematically modeled, as illustrated in Fig. 5. $y_{\text{out}}(t)$ is the response of the DUT's idealistic model to the input signal $y_{\text{in}}(t)$, whereas $y_n(t)$ represents the noise generated by the DUT. Without loss of generality, $y_n(t)$ is usually assumed to be a white Gaussian additive noise. The measurement of noise is computed in the frequency domain instead of the time domain, mainly due to the following two factors: First, it is very hard to estimate $y_n(t)$'s power from the time domain, and second, even if we can find a way to determine $y_n(t)$'s power, it is still meaningless because we only care about the noise over the bandwidth of interest, which is usually much smaller than $y_n(t)$'s real power [10], [31].

The popular way to analyze and measure noise is to specify its power spectral density (PSD). Mathematically, PSD describes a stochastic sequence's power distribution at the frequency domain. Therefore, given the noise's PSD, the total noise power over the band of interest can be obtained through the integral of the PSD within the bandwidth. A number of classical nonparametric spectral estimation methods are given in [32]. The periodogram method, among these methods, is the simplest one and fits our BIST architecture perfectly. The periodogram for a digital sequence $x_0, x_1, \ldots, x_{N-1}$ is given by

$$S(f) = \frac{1}{Nf_s}\left|X_N(f)\right|^2 = \frac{1}{Nf_s}\left|\sum_{n=0}^{N-1} x(n)e^{j2\pi fn}\right|^2 \tag{18}$$

where f_s is the sampling frequency of the digital sequence $x(n)$, and N is the length of sequence $x(n)$.

According to (18), the PSD of the noise introduced by the DUT can be described as

$$\begin{aligned} S(f) &= \frac{1}{Nf_{\text{clk}}}\left|\sum_{n=0}^{N-1} y_n(nT_{\text{clk}})e^{j2\pi fn}\right|^2 \\ &= \frac{1}{Nf_{\text{clk}}}\left|\sum_{n=0}^{N-1}\left[y'_{\text{out}}(nT_{\text{clk}}) - y_{\text{out}}(nT_{\text{clk}})\right]e^{j2\pi fn}\right|^2. \end{aligned} \tag{19}$$

Furthermore, the aforementioned continuous spectrum representation can be expressed in a sampled discrete format. Thus, (19) can be transformed as

$$S(k) = \frac{1}{Nf_{\text{clk}}}\left|\sum_{n=0}^{N-1}\left[y'_{\text{out}}(nT_{\text{clk}}) - y_{\text{out}}(nT_{\text{clk}})\right]e^{j\frac{2\pi}{L}nk}\right|^2. \tag{20}$$

Usually, (20) can be computed through the FFT algorithm. However, there is always a large area penalty and power consumption associated with an FFT processor. The philosophy of our BIST approach is to sacrifice the processing time to obtain a much more flexible, simpler, and cheaper BIST approach for on-chip and in-system test and measurements.

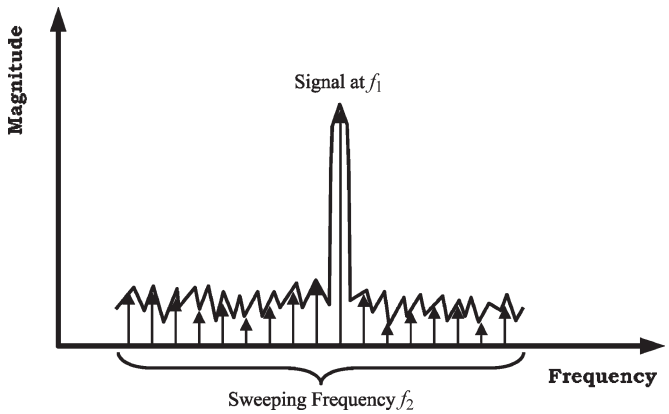

Fig. 6. SNR measurement using BIST.

To perform the NF measurement in the BIST approach (refer to Fig. 2), the TPG in the BIST circuitry generates a sine-wave $\sin(\omega_1 t)$ to stimulate the DUT. An in-phase tone and an out-of-phase tone at frequency ω_2 are produced at the same time and fed into the ORA. By sweeping ω_2 over the interested frequency band, the ORA can then obtain $y'_{\text{out}}(t)$'s spectrum information, as illustrated in Fig. 6. Since the signal of interest only appears at frequency f_1, the spectrum of the noise $Y_n(f)$ can be easily estimated by sampling at all other frequencies with respect to the signal at frequency f_1. Then, the noise's PSD and SNR can be measured based on (20) and (16), respectively. As illustrated in Fig. 2, the test controller is capable of bypassing the DUT through MUX3 such that the input and output SNR of the DUT can be measured, respectively. From these two SNRs, the NF of the DUT can be determined directly using (17) in the BIST circuitry.

IV. Experimental Results

To prove the effectiveness and feasibility of the proposed BIST architecture for NF measurements of analog circuitry in addition to linearity and frequency response measurements, we have implemented the BIST architecture shown in Fig. 2 in hardware. The digital portion of the BIST circuitry was implemented in a Xilinx Spartan XC2S50 FPGA on a Xinlix XSA50 printed circuit board (PCB). A DAC (AD9752AR by Analog Devices) with low-pass filter and an 8-bit ADC (AD9225AR by Analog Devices) were implemented on a separate PCB. An operational amplifier built on a separate board serves as the DUT for the NF and frequency response measurement. The actual BIST circuitry is shown in Fig. 7. Some important parameters of the experimental hardware system are summarized in Table III. Although some of experimental results presented in this section show some constraints of our current BIST circuitry to perform the NF measurement, it should be noted that these limitations are mainly due to the prototype hardware instead of the proposed BIST architecture.

A. Validity of DDS-Generated Test Tones

A comparison between the test tones generated by our actual TPG implementation and an Agilent 33250A waveform generator was conducted to ensure the validity of the

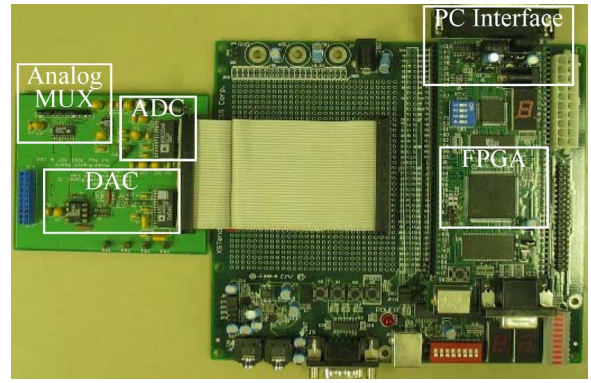

Fig. 7. Experimental hardware prototypye system.

TABLE III
Experimental System Parameters

Parameter	Value
DAC Resolution	8-bit
ADC Resolution	8-bit
f_s (DAC/ADC Sampling Clock)	12.5MHz

DDS-based TPG as a signal source for NF measurement, without introducing excessive noise in the frequency band of interest. Fig. 8 gives the spectrums of two tones measured by an Agilent 8563EC spectrum analyzer with *resolution bandwidth* (RBW) of 100 Hz. According to [33], it is known that the actual signal-to-noise floor ratio (SNFR) can be expressed as

$$\text{SNFR}_{\text{actual}}\ [\text{dBc/Hz}] = \text{SNFR}_{\text{displayed}} - 10\ \log_{10}(\text{RBW}) \tag{21}$$

where $\text{SNFR}_{\text{displayed}}$ is the SNFR displayed directly on the spectrum analyzer. From (21), the $\text{SNFR}_{\text{actual}}$ for the tone coming from the 33250A is around 110 dBc/Hz, whereas the one for the TPG is about 7 dBc/Hz worse than the signal generator, with some apparent spurious contents at several frequency points.

As compared with the signal generator, the TPG provides a dynamic range of measurable noise level only with 7 dBc less. Also, this problem could be solved if a DAC/ADC pair with higher resolution could be adopted in the mixed-signal system. As for the distortion shown in Fig. 8(a), it has ignorable impact on the NF measurements as well as the linearity and frequency response measurements. In NF measurements, what we care most about is the noise floor. Although the spurs have higher noise power than the noise floor, they appear only at several frequency points. Therefore, their contribution to the total noise power over the frequency band of interest would be negligible. On the other hand, the frequency spectrum information used for the linearity and frequency response measurements is only the one located at the carrier frequency, which is over 60 dBc higher than the spurs. Hence, again, the spurs' effects to the accuracy of these measurements are of no concern. The conclusion then is that the DDS-based TPG is a valid signal source for the BIST circuitry, although its performance is slightly worse than an external signal generator.

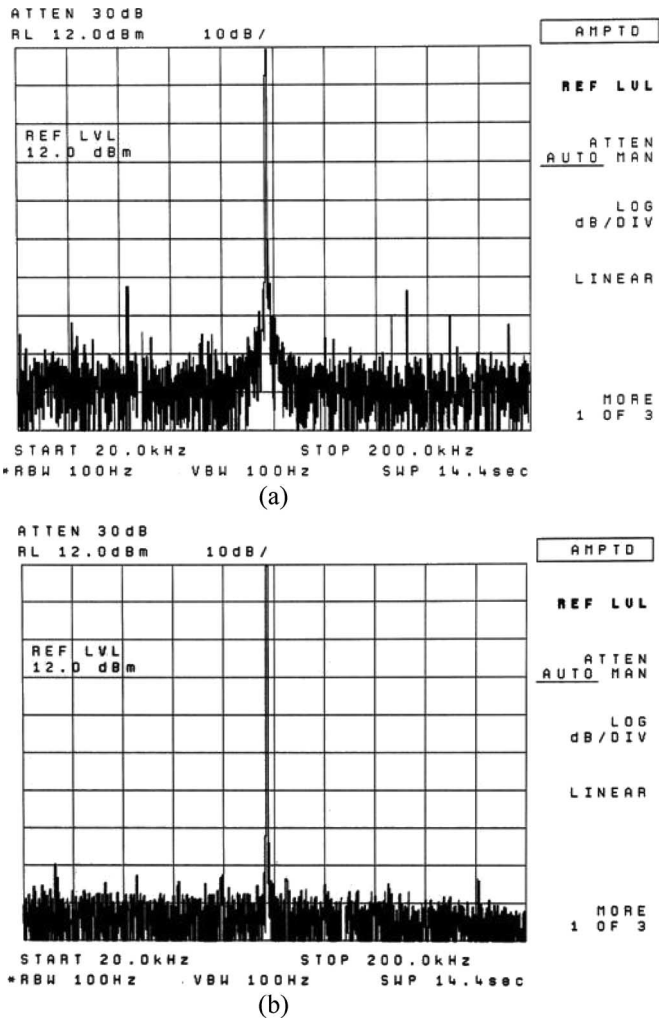

Fig. 8. Comparison of DDS-based TPG and signal generator. (a) DDS-generated tone observed by spectrum analyzer. (b) Tone from signal generator observed by spectrum analyzer.

B. Noise Calibration in BIST Circuitry

The BIST circuitry, as an electrical system itself, will also introduce noise. The noise in BIST circuitry limits the dynamic range of measurable noise level and degrades the accuracy of the measurement results. Thus, the noise introduced by every key component (refer to Fig. 2) along the test path should be deembedded prior to the actual measurements.

1) Noise of the DAC: In the test path, the DAC is driven by a digital tone with 8-bit resolution. Because of the limited word length effect, the introduction of quantization noise is inevitable. Using the time-domain method of SNR measurements presented in [25], the signal-to-quantization noise ratio of the digital tone over the band $[0, f_s/2]$ is about 36.2 dB. After the digital tone is converted to an analog tone, its frequency spectrum is displayed in Fig. 8(a). The SNR over the same band can be calculated according to (22), which is cited from [34], i.e.,

$$\mathrm{SNR} = \mathrm{SNFR}_{\mathrm{displayed}} - 10\,\log_{10}\left(f_s/(2\cdot \mathrm{RBW})\right). \quad (22)$$

Thus, the SNR after the DAC is obtained is about 35 dB, which does not take the distortion into consideration. Thus, the actual SNR after the DAC is slightly lower than 35 dB. Comparing the two SNRs before and after the DAC, we find that the DAC introduces very little noise, and its effects can be easily cancelled out through careful calibration.

2) Noise of the Amp and MUX3: The spectrum of the signal after the Amp and MUX3 was also measured by the spectrum analyzer. There was very little difference between the spectrum and the one shown in Fig. 8(a). Thus, the noise introduced by these two components can be neglected.

3) Noise of the ADC: Because the signal after the DAC is transformed back into digital form, it cannot be measured directly using the spectrum analyzer. However, according to the specifications for the DAC and ADC, the noises introduced by the DAC and ADC are very close to each other. Therefore, it is believed that the noise introduced by the ADC is also small and can be compensated easily as the noise done by the DAC.

4) Noise of the ORA Due to the Finite Number of Bits: After the signal enters the ORA, the spectrum purity, as described in Section II, is affected by the limited word length effect, namely the quantization noise that intrinsically exists in any digital systems. The calculation noise can be quantified through a simulation on computer. In the simulation, a digital sine wave with 8-bit resolution was generated in software, which then was analyzed by two simulated ORAs. One ORA performs the analysis using double-precision numbers and can be treated as an ideal ORA, whereas the other one simulates the actual ORA used in our BIST circuitry with 8-bit resolution. The results are shown in Fig. 9, from which we find that the 8-bit ORA will introduce a calculation noise of about 11 dBc/Hz. Although the noise can be quantified precisely and compensated, it sacrifices the BIST circuitry about 12 dB of dynamic range.

5) Noise of the FPGA: The FPGA used to realize the TPG and ORA is another noise source in the whole test path. It is well known that the switching noise caused by a heavy-loaded FPGA chip is very significant. It should be noted that Fig. 8(a) is measured when all modules in the FPGA are in idle state, only with NCO1 as an exception. However, while the FPGA is fully loaded with the NF measurement, the signal measured at the same test point as Fig. 8(a) abruptly changes to what is shown in Fig. 10. From the comparison between the two measured spectrums in Figs. 8(a) and 10, it can be found that the noise floor increases above 30 dB/Hz at low-frequency end and above 25 dB/Hz at the high end (note that the RBW is equal to 10 Hz instead of 100 Hz as was the case in Fig. 8). The spectrum of the injected FPGA switching noise varies slowly with time. While this causes some difficulty to quantify the noise with external test equipment, the noise can easily be characterized using the BIST circuitry instead, which will soon be verified.

According to the measurement and analysis done in this section, the SNFR of our BIST circuitry itself is about $(103 - 12 - 30)$ dBc/Hz $= 61$ dBc/Hz. The calculation and switching noise contributes most of the noise in the circuitry and decreases the BIST's dynamic range by about 40 dB.

C. NF Measurement Using External Test Equipment

To verify the accuracy of the BIST circuitry NF measurement, another NF measurement was conducted totally, with

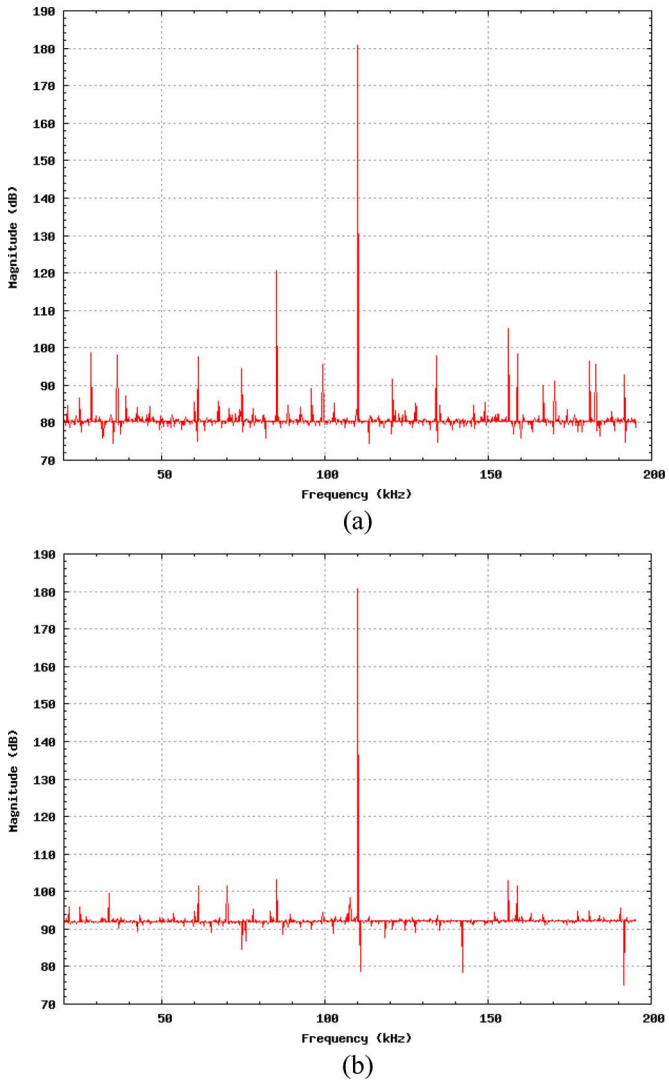

Fig. 9. Calculation noise caused by limited word length effect. (a) Spectrum analysis done by an ideal ORA. (b) Spectrum analysis done by an ORA with 8-bit resolution.

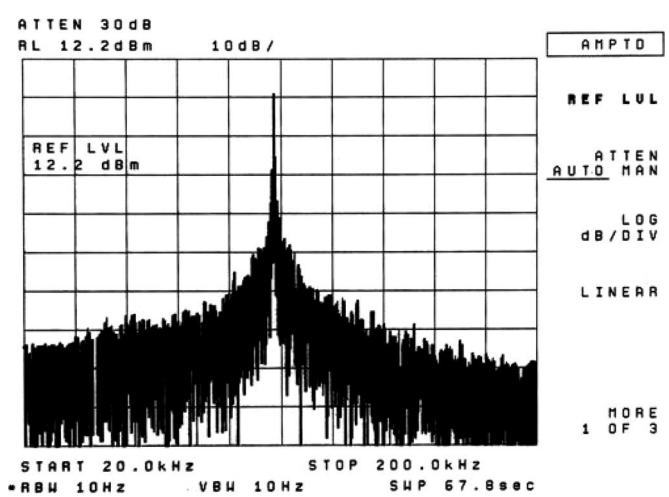

Fig. 10. TPG-generated tone during NF measurement.

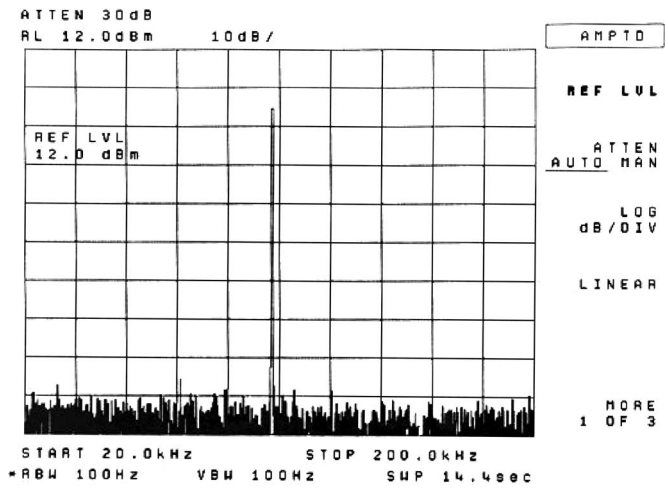

Fig. 11. Output response of the DUT driven by 33250A waveform generator.

external test equipment as a reference. The test tone entering into the DUT is generated by the signal generator, and its spectrum is shown in Fig. 8(b). The output coming from the DUT was measured by the spectrum analyzer and is shown in Fig. 11. The $\mathrm{SNFR_{in}}$ and $\mathrm{SNFR_{out}}$ of the DUT are read from these two figures as 110 and 96 dBc/Hz, respectively. From (17) and (22), the DUT's NF can be calculated as

$$\mathrm{NF_1} = \mathrm{SNFR_{in}} - \mathrm{SNFR_{out}} = 110 - 96 = 14\ \mathrm{dB}. \tag{23}$$

D. NF Measurement Using BIST Circuitry

The NF measurement by the BIST circuitry was conducted as described in Section III, and the measured spectrums are shown in Fig. 12. The $\mathrm{SNFR_{in}}$ and $\mathrm{SNFR_{out}}$ of the DUT are read from Fig. 12 as 60 and 45 dBc/Hz, respectively. The DUT's NF can be calculated in the same way as (23), and the result is

$$\mathrm{NF_2} = \mathrm{SNFR_{in}} - \mathrm{SNFR_{out}} = 60 - 45 = 15\ \mathrm{dB}. \tag{24}$$

Comparing the $\mathrm{NF_1}$ and $\mathrm{NF_2}$ in (23) and (24), we find that there is only 1-dB difference between the two measurements using external test equipment and the BIST circuitry. This shows the accuracy of the BIST measurement circuitry. Also, when comparing the $\mathrm{SNFR_{in}}$ shown in Fig. 12(a) and the estimated SNFR presented at the end of Section IV-B, we see that there exists only about 2-dB difference. This also proves the accuracy of the BIST circuitry from another aspect. Of course, the current BIST circuitry cannot provide good dynamic range, as discussed in Section IV-B. However, the major problems were identified according to the analysis in Section IV-B. As a result, the performance of the BIST system can be easily improved.

Through the noise analysis presented in Section IV-B, it was shown that the resolution of the DAC/ADC pair and FPGA switching noise play major roles to constrain the performance of the BIST circuitry. To realize a high-performance BIST

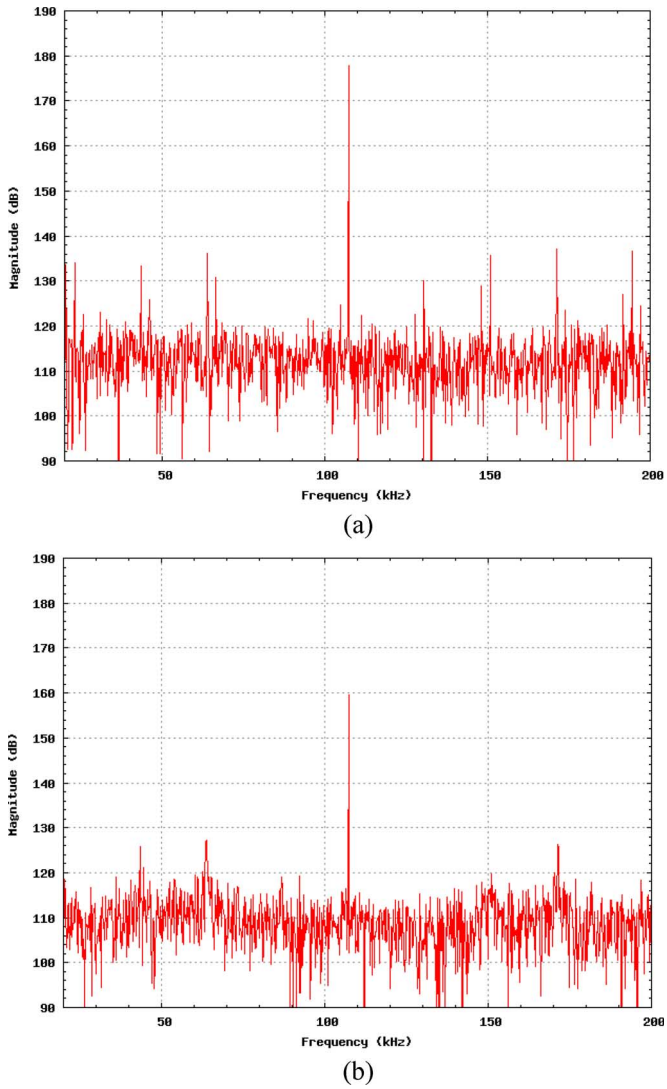

Fig. 12. NF measurement of DUT performed by BIST circuitry. (a) SNFR measurement at DUT input. (b) SNFR measurement at DUT output.

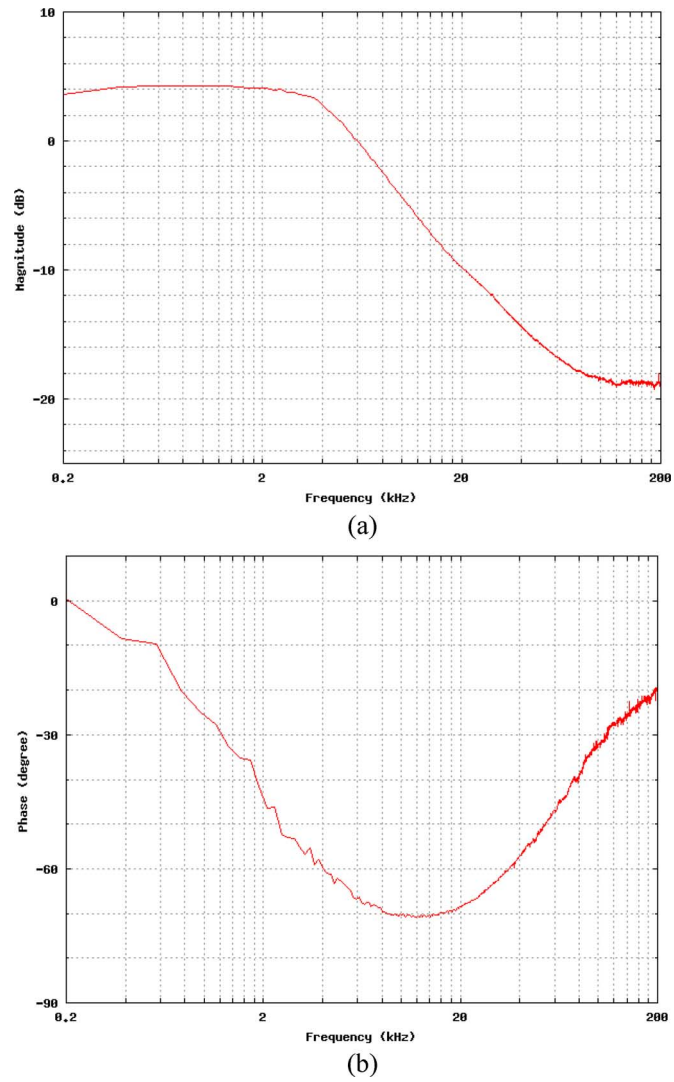

Fig. 13. Frequency response measurement of DUT performed by BIST circuitry. (a) Amplitude response measurement. (b) Phase response measurement.

circuitry based on this architecture, a DAC/ADC pair with higher resolution would be used. Preventing the FPGA switching noise from injecting into the analog portion of the system is another critical factor to be taken into consideration in the design of a mixed-signal system that uses FPGAs.

E. Frequency Response Measurement Using BIST Circuitry

The frequency response of the DUT is also measured by the BIST circuitry. The measured amplitude and phase response of the DUT are shown in Fig. 13(a) and (b), respectively. Although more variations are observed at high-frequency end than at low end in both of the figures, the phenomenon is not a mistake but is what we expected. The reasons are twofold. First, the DDS-generated tones at high frequency have fewer samples in each period than the ones at low frequency. Thus, there are more errors injected the digital tones for the ORA at high frequency, which then causes more variations. Second, the logarithm operation compresses the x-axis more at high frequency than at low frequency, which magnifies the intensity of the variations greatly. These two factors are combined together and cause the intensive variations.

TABLE IV
SYNTHESIS RESULTS FOR BIST CIRCUITRY

FPGA Attribute	Used by BIST	Total in FPGA	% Usage
# of slices	371	768	48%
# of flip-flops	263	1,536	17%
# of 4-input LUTs	656	1,536	42%
Maximum BIST Clock Frequency = 48.5 MHz			

F. Comparison of DDS-Based BIST and FFT-Based BIST

The TPG, test controller, and ORA were implemented with a Xilinx Spartan XC2S50 FPGA along with an interface to allow a processor to control the BIST circuitry and retrieve the BIST results. Table IV summarizes the synthesis results to give an idea of the area of the complete BIST circuitry occupied in an FPGA. It should be noted that the XC2S50

TABLE V
FPGA RESOURCES USED FOR EACH BIST COMPONENT

FPGA Attribute	TPG NCO	ORA MAC	PC interface
# of slices	42	101	41
# of flip-flops	36	60	35
# of 4-input LUTs	52	182	52

TABLE VI
RESOURCES USAGE OF 256-POINT FFT IMPLEMENTATIONS ON VIRTEX II FPGA

Type	# of slices	# of block RAMs	# of 18×18 multipliers	Transform frequency
Pipelined	1769	4	12	195 kHz
Burst I/O	1411	7	9	92 kHz
Minimum Resources	1365	0	3	37 kHz

is a small-sized FPGA in the Spartan II series and has the same size as the smallest Virtex FPGA. In fact, the 8-bit BIST circuitry can easily fit in the smallest Spartan II series FPGA, i.e., the XC2S15. Therefore, the size of the BIST circuitry is reasonably small, with the DDS-based TPG accounting for approximately one-third of the total circuitry. Moreover, there is some additional circuitry for data capture and monitoring purposes, which can be eliminated for actual BIST implementations. These additional resources are referred to as PC interface in Table V, where a breakdown of the resources required for each type of BIST component is summarized. The resources usage of a MAC with respect to the different bit numbers of multiplier and accumulator was studied and presented in [12].

The maximum clock frequency of the BIST circuitry is dominated by delays in the multiplier and accumulator in the ORA and can be increased significantly by simply pipelining the ORA with additional flip-flops at the outputs of the multiplier before entering the accumulator. Since there are more four-input LUTs used in the BIST circuitry than flip-flops, pipelining the ORA will cause little, if any, increase in the FPGA utilization because most flip-flops at LUT outputs are unused in the synthesized implementation.

These synthesis results can be compared to the FFT-based BIST approach proposed in [23] and the FFT implementations in [35] and [36]. For a 256-point FFT with a 32-point approximate kernel, [23] used a Virtex II XC2V8000, which itself is almost 250 times larger than the XC2S15, for implementation of that FFT-based BIST approach. The maximum clock frequency of this approach was reported to be between 1 and 2 MHz [23], whereas our approach will operate at 48.5 MHz with no modifications to the architecture, such as pipelining, to improve performance. Reference [35] gives a number of FFT implementations for different point size on Virtex-II, Virtex-II Pro, and Virtex-4 series FPGAs. We chose three types of 256-point FFT implementations on Virtex II for comparison. The resources usage and performance of these implementations in a Virtex-II FPGA are summarized in Table VI. For another example, a 1024-point radix-2 FFT alone requires 3332 slices in addition to three 18 × 18-bit multipliers in a Virtex II or Spartan 3 FPGA [36].

Consider the fastest pipelined implementation in Table V as an example. With almost five times more slices, plus four 18 432-bit block RAMs and twelve 18 × 18-bit multipliers that are not used in our circuitry, the pipelined-type FFT processor can only run at 195 kHz. However, using much fewer resources, our circuitry not only provides the same function as an FFT processor can do but also includes TPG, ORA, test controller, and a communications interface. Furthermore, the two multipliers in the ORA account for almost one-third of the total resources used by the BIST circuitry. As a result, by using only two of the multiplier cores in the Virtex-II FPGA, we can reduce the slice count in Table IV by about one-third. Virtex-4 contains DSPs that include not only 18 × 18-bit multipliers but also 48-bit accumulators. As a result, two DSP cores can be used in a Virtex-4 FPGA to implement the entire ORA, reducing the BIST circuitry slice and flip-flop counts in Table IV by two-thirds and greatly improving the maximum clock frequency of the synthesized BIST circuitry. Finally, the accumulators in the DSP can also be used for implementing the accumulators of the NCOs in the TPG, whereas RAM cores can be used for the sine-wave LUTs. As a result, almost the entire BIST circuitry can be implemented in the high-performance DSP and RAM cores in the Virtex-4 FPGA. However, the synthesis results in Tables IV and V illustrate the fact that the BIST circuitry can be efficiently implemented in any FPGA without the need for specialized cores.

From this comparison, we can conclude that the BIST circuitry presented in this paper is much simpler and cheaper, and can also achieve flexibility that the FFT-based approach cannot provide. For example, the maximum number of the points that an FFT processor can compute is fixed, such that it is difficult, if not impossible, to adjust the frequency resolution when using an FFT-based approach. Instead, the frequency resolution can be easily tuned with the step size of the sweeping frequency in our BIST approach. In addition, we are typically only interested in several frequency points or in a narrow bandwidth, which can be done easily using our scheme, whereas FFT-based scheme has to compute a great amount of information that may be useless because FFT processes the whole frequency domain at one time.

In an application-specific IC, the digital portion of the BIST circuitry could be efficiently implemented as standard cell via synthesis tools. However, FPGAs provide the ability to implement the BIST circuitry only during offline testing such that there are no area, performance, or power penalties to the system during normal operation.

V. CONCLUSION

An FPGA-based BIST approach used for adaptive control in mixed-signal systems was presented. It provides the ability to perform analog functional measurements, including NF measurements as well as IP3 and frequency response. The accuracy of the BIST circuitry is proved through experimental results listed in Section IV and [8]. The proposed BIST circuitry provides an effective means for adaptive control in a mixed-signal system. The BIST architecture has been implemented in Verilog and parameterized for specification of the desired

size of the DDS-based TPG and MAC-based ORA based on the sizes of the DAC and ADC targeted for the mixed-signal system. As a result, it can be easily incorporated in any mixed-signal system design and synthesized into an FPGA. The BIST implementation is efficient in terms of area and can easily fit into the smallest FPGAs in the market. This facilitates permanent residence of the BIST circuitry in the system application. Alternatively, in-system reprogramming of the FPGA can be used to reconfigure the BIST circuitry into the FPGA with access to the DAC and ADC for on-demand analog functional test and measurement for adaptive control of the system without imposing area, performance, or power penalties during normal system operation.

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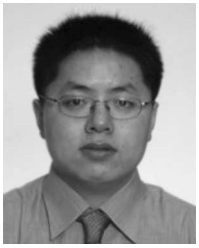

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