

A Fully Integrated Multi-Band MIMO WLAN Transceiver RFIC

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Abstract

A multiple input multiple output transceiver compliant with IEEE 802.11a/b/g and Japan wireless LAN standards is presented. The transceiver has two complete radio paths integrated on the same chip. When two chips are used in tandem to form a four path composite beam forming system, 15dB of link margin improvement is obtained. The transceiver was implemented in a 47GHz SiGe technology and consumes 195mA in RX mode and 240mA in TX mode from a 2.75V supply.

Introduction

The ever-increasing demand for wireless and multimedia applications [1]-[3] such as video streaming keeps pushing future wireless LAN (WLAN) systems to support much higher data rates (100 MBit/s up to 1 GBit/s) at high link reliability and over greater distances. Next-generation wireless communication systems are focused on increasing the link throughput (bit rate), the network capacity and the transmit range. A multiple input multiple output (MIMO) system in combination with space-time signal processing allows increased data rate and/or improved transmission range and link reliability without additional costs in bandwidth or transmitted power. MIMO systems using multiple antennas allow enhancements to the existing IEEE 802.11 WLAN technology [4][5]. The next generation of WLAN standards could be based on MIMO technology to achieve high data rate and improved range. Indoor environments, where most of the WLAN systems are deployed, are typically characterized by richly scattered multipath signals. Under these conditions having MIMO will lead to dramatic performance improvements. Fig. 1 compares the SNR ratios required for a given data rate using different radio configurations. In the graph a conventional single-input-single-output (SISO) 1x1 link, namely, one transmitter one receiver architecture is compared to various MIMO systems such as a 1x2 select diversity link (spatially separated receiver or transmitter antennas to select the strongest signal), a 4x4 link that uses composite beam forming (CBF) technology and maximal ratio combining, and a vector CBF (VCBF) link. This paper presents a MIMO radio RFIC implementation that supports CBF technology. VCBF represents a potential future MIMO application, which uses separate orthogonal data streams on each antenna to reduce the required SNR.

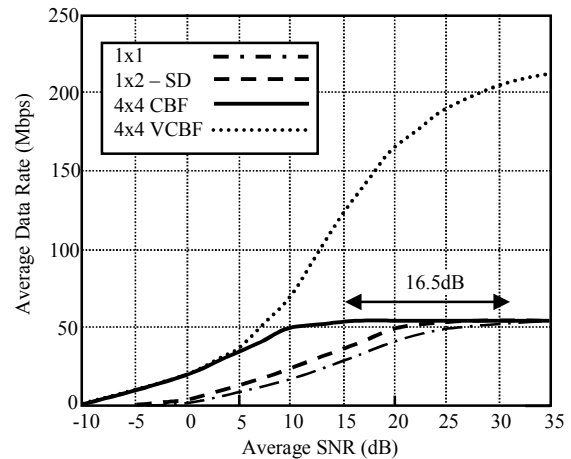


Fig. 1. Data rate vs. required SNR for various link configurations.

This paper presents an RFIC transceiver designed for MIMO WLAN applications. Two complete a/b/g dual-band radios are integrated on a single chip and can be used to form a two-radio by two-radio link. Additionally two chips can be used together to form a 4 X 4 link. This chip itself includes a $\Sigma\Delta$ based fractional-N frequency synthesizer, and two transceivers for both the 2.5GHz and 5GHz bands. With the exception of the synthesizer loop filter, and the matching networks for LNA and PA, the entire 2x2 MIMO radio system is integrated in one chip. Two chips may be used together in a master and slave configuration to form a 4 X 4 MIMO radio transceiver system.

MIMO Transceiver Design

As a trade-off between level of integration and complexity/yield, this work integrated two multi-band dual radio paths on the same die. A 2x2 MIMO link can therefore be formed using only two MIMO transceiver ICs, compared to four SISO chips. The presented MIMO WLAN transceiver IC supports the 802.11b/g, 802.11a lower/middle and Japan 2.4/5GHz bands. In this system only two radios were integrated because more would have led to more expensive packaging, lower yield, and for many applications a 2x2 MIMO system with two radios is sufficient. However, if more than two radios are desired in a particular application, then even two, three, or more dual-radio transceiver chips can be used in a single link, provided that their local oscillations (LO) are all phase synchronized. Each transceiver pair consists of a master and a slave dual-radio transceiver chip. The slave chip synchronizes

its LO to the master chip by means of the LO porting circuitry, in which the master chip's $\Sigma\Delta$ fractional-N synthesizer can be used to drive the slave chip's LOs for synchronization. To the best of the authors' knowledge this work is the first WLAN MIMO integrated transceiver reported so far.

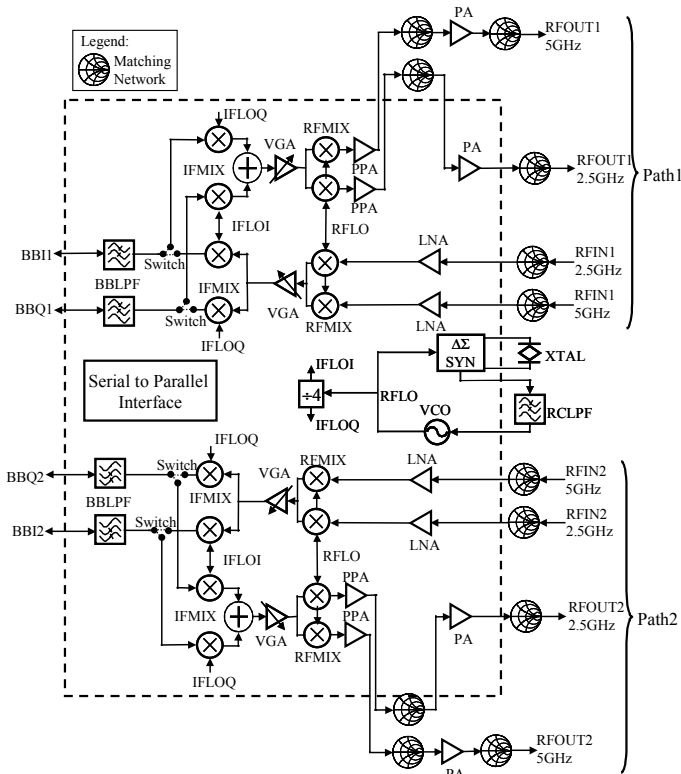


Fig. 2. MIMO Transceiver Architecture.

The dual-radio MIMO transceiver block diagram is illustrated in Fig. 2. Each individual multi-band radio consists of a receiver (RX), a transmitter (TX), a base-band filter, a shared frequency synthesizer, bandgaps, control logic and a serial to parallel interface (SPI) for transceiver programming. The transceiver is a superheterodyne architecture with sliding intermediate frequency (IF). In this architecture only one frequency synthesizer is required to generate the first LO [6]. The second LO is obtained by dividing the first LO by four. This reduces not only the number of frequency synthesizers, but also the number of LOs and IFs that require synchronization for a MIMO transceiver system. The drawback of the sliding IF architecture is that the system must tolerate a wider IF bandwidth. In this case, the IF signal varies from 800MHz to 1070MHz. An LO porting scheme has been employed on the chip such that the mixers can be driven either by the synthesizer on the same die or by an external LO generated by another chip.

The receiver consists of single ended cascoded LNAs, down conversion mixers, a variable-gain amplifier (VGA), an I/Q demodulator and baseband filters. The LNAs are single ended in order to reduce silicon area and power consumption. There are two LNAs, one for 2.4GHz and another for 5GHz bands. The 2.4GHz LNA has high gain and low gain modes

that step the gain by 22dB. The RF mixer outputs drive the Variable Gain Amplifier (VGA), which provides up to 23dB gain in 3dB steps with a total of 15 steps. The VGA output drives the IF quadrature demodulators, which generate the I/Q baseband signals. Careful layout in the I/Q demodulator ensures good quadrature matching. Finally the I/Q demodulator outputs drive the tunable baseband filters.

Each TX chain consists of IF quadrature modulators, VGAs, and two RF upconversion mixers, pre-drivers and power amplifiers (PAs) for 2.4 and 5 GHz bands, respectively. The VGA has a gain range of 39dB, and a gain step of 3dB. Each RF mixer is followed by an on-chip image rejection filter, which has a low-pass characteristic for the 2.4GHz band and a band-pass characteristic for the 5GHz band respectively. The output power detectors are integrated with the PA, and no off-chip components are required.

The base-band filters were implemented using active-RC circuits due to the demanding requirement for high linearity. The filter can be programmed to have a narrow-band mode with a 9.8MHz corner (5th order elliptic) and wide-band mode with a 41.75MHz corner (7th order Chebyshev). The filter corner frequency is digitally tunable in 16 steps in order to compensate for the variations over process and temperature. In order to save silicon area, a multiplexing scheme is implemented such that the same filter cores are used for both transmit and receive modes. The mixer DC offset is compensated using digital-to-analog converters (DAC) with feedback controls provided by the base-band IC.

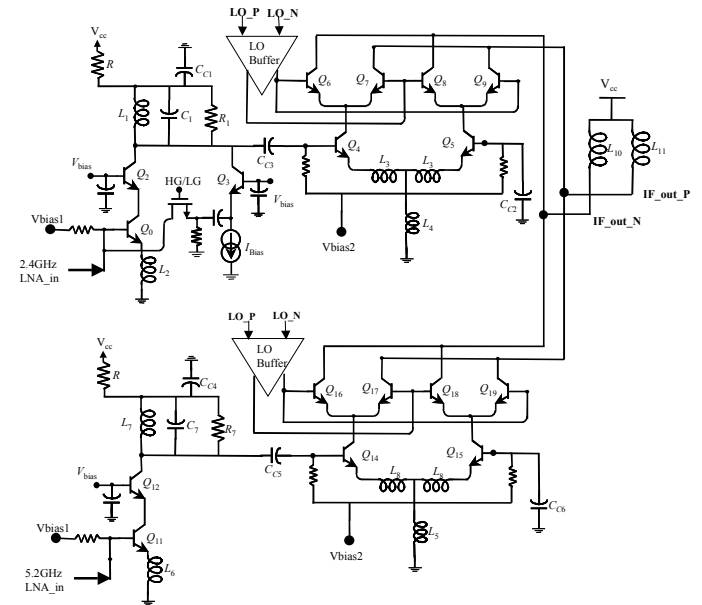


Fig. 3. Schematic diagram of dual-band receiver front end.

The multi-band receiver front-end schematic is shown in Fig. 3 where bias circuitry is not included for simplicity. The LNAs are single ended in order to reduce silicon area and power consumption (only 5mA of DC current per LNA). They are tuned cascode-common-emitter LNAs with inductive emitter degeneration for increased linearity. The 5GHz LNA (Q_{11} , Q_{12}) has high gain only. The 2.4GHz LNA has high gain and low

gain modes. For high gain the cascode amplifier (Q_0 , Q_2) is powered while the common-base amplifier (Q_3) is off. For low gain, the NMOS switch is turned on and Q_3 is turned on while Q_0 is powered down. The RF mixers are Gilbert cell mixers with inductive degeneration for increased linearity with low noise. The 2.4GHz and the 5.2GHz mixers are connected together at their IF outputs in order to share external inductive pull-ups (L_{10} , L_{11}) which tune the IF port to 1GHz as well as increase voltage headroom. This creates a bandpass response at the IF output which removes higher order harmonics. The 2.4/5.2GHz front-ends provide 25/20dB of voltage gain respectively.

Measured Results

The transceiver was fabricated in a 47GHz SiGe BiCMOS process with 0.5 μ m lithography. The back end of the process featured thick aluminum metallization designed to provide high quality inductors. A die photo of the chip is shown in Fig. 4. The entire MIMO transceiver chip is measured to be 5.4mm by 5.4mm and the chip occupies a total silicon area of 29.1mm². The 802.11a/b WLAN MIMO transceiver has been packaged in a 72pin Leadless Plastic Chip Carrier (LPCC) package and mounted in a PCB for testing.

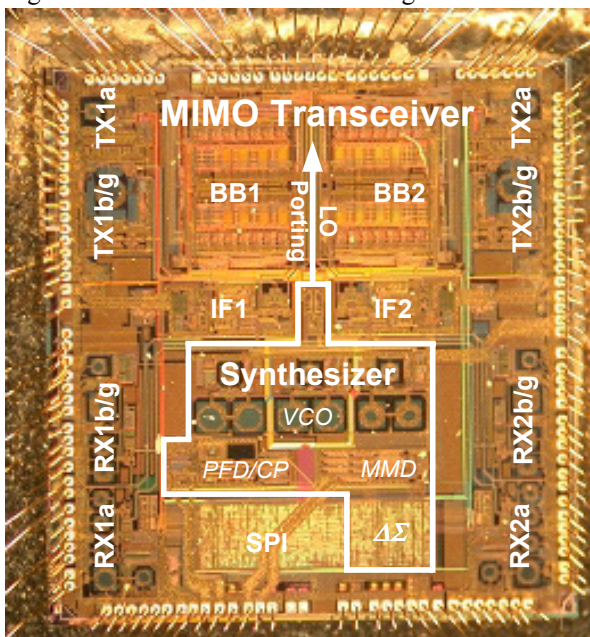


Fig. 4. Die photograph of the dual radio MIMO WLAN transceiver.

The total current consumption in receive mode for one path was 195mA for either 2.4GHz or 5.2GHz band including the synthesizer power consumption. When two receiver paths in the dual radio system were powered the current went up to 320mA. The current didn't double because the two paths shared the synthesizer, which is one of the advantages of integrating multi-radio MIMO system in one chip. The receiver gain for the full path was 77dB for the 2.4GHz band and 72dB for the 5.2GHz band. The noise figure for the full receiver chain was 4.5dB in the 2.5GHz path and 7.4dB in the 5.2GHz path.

The tunable baseband filter was configured as a 5th order

elliptic ladder filter for a narrow-band mode with 9.8MHz corner frequency. The measured filter passband ripple below 6MHz was 0.6dB p-p and the group delay ripple below 6MHz was 50nsec p-p. The attenuation at 12MHz was 15dB, and attenuation beyond 21MHz was more than 60dB. The noise of the filter was approximately 400 nV/ \sqrt{Hz} measured differentially at the receive filter output. At full signal output amplitude, third order mixing products were approximately 55dBc down. A plot of the measured filter response is given in Fig. 5 for 32 different chips.

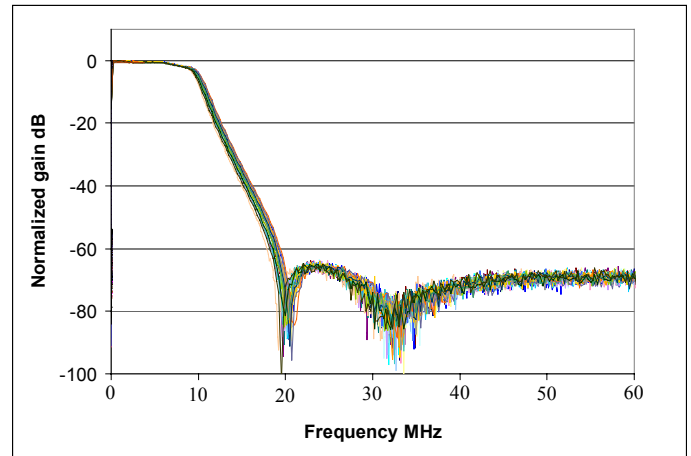


Fig. 5. Plot of the measured base band filter response in narrow band mode for 32 devices.

The I-Q modulators achieved better than 40dB of image rejection and 26dB of carrier rejection. The TVGA has a gain range of 39dB, a gain step of 3dB, a gain variation smaller than 0.3dB, and phase variation smaller than 25°. Each RF mixer has either an on-chip low-pass (2.4GHz) or band-pass (5GHz) filter associated, and the image rejection is better than 20dB. The transmitter can deliver +10dBm of linear power at 2.4GHz with the on-chip PA, and +13.5dBm of linear power at 5GHz with an off-chip PA. The cross coupling between the two transmit paths is better than 40dB.

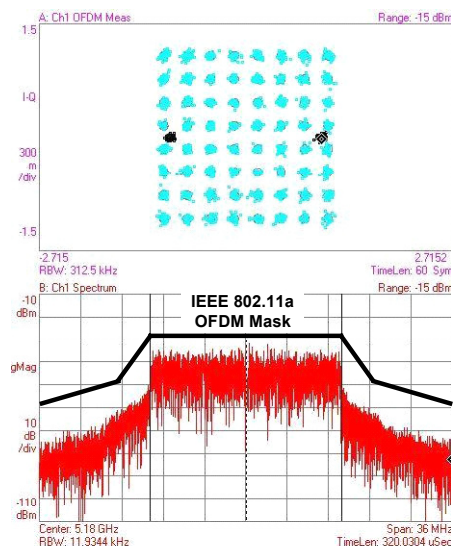


Fig. 6. EVM Measurement for 802.11a Channel 36, EVM=4.3% meets IEEE 802.11a OFDM requirement.

The total current consumption in transmit mode for one radio path is 240mA for the 802.11b/g band and 255mA for the 802.11a band. When two paths are powered the current goes up to 400mA in the 802.11b/g band and 430mA in the 802.11a band. Fig. 6 shows a typical EVM measurement, which complies with the IEEE 802.11a WLAN standard requirements. The integrated jitter for the synthesizer was better than 0.43°rms for the 802.11b/g band and better than 0.86°rms for the 802.11a band. Table I summarizes key performance parameters for the transceiver.

TABLE I

SUMMARY OF TRANSCEIVER PERFORMANCE

Parameter Band	Performance	
	802.11b/g	802.11a
Technology	0.5 μ m SiGe BiCMOS	
Voltage Supply	2.75V	2.75V
TX Chain Current Supply (1path/2paths)	240/400mA	255/430mA
RX Chain Current Supply (1path/2paths)	195/320mA	195/320mA
Synthesizer Current supply	36mA	36mA
TX output power	11dBm	13.5dBm
RX NF @ Max Gain	4.1dB	7.5dB
RX chain Max Gain	77 dB	72 dB
RX chain Min Gain	5.5dB	25dB
Rx IIP3 @ Min Gain	+8.8 dBm	-12.8 dBm
RX I/Q Amplitude Imbalance	0.3 dB	0.3 dB
RX I/Q Quadrature Error	2.0°	2.0°
Max DC offset without correct	90mV	90mV
Synthesizer Integrated Noise 100Hz to 10MHz	0.35-0.43° rms	0.63-0.86° rms

In order to demonstrate the MIMO radio link using the developed dual-radio RF transceiver ICs, a prototype link was tested to determine the improved range of a MIMO WLAN in the company's office building. Fig. 7 shows the range improvements that were achieved by using different link configurations as measured from a central access point (AP). Note that a 4x4 link is not shown in the figure, as the office was not big enough to test the range limits using this type of link. As shown, the WLAN transmission range has been greatly improved using 4x2 CBF configuration, where 4 radio paths (2 dual-radio RFICs) are used in the access point (AP) and 2 radio paths (1 dual-radio RFIC) are used at the user end. The total transmit power for any MIMO configurations under the test were within the IEEE 802 WLAN standard. The "2sel" refers to 2-antenna selection diversity. This configuration uses 2 antennas and the receiver selectively picks the one with the strongest signal. Thus, a 4CBFx2sel is actually a 4x1 CBF configuration with the receiver antenna corresponding to the strongest signal out of a two-antenna selection diversity. Similarly, a 1x2sel is a 1x1 configuration with the receiver antenna corresponding to the strongest signal out of a 2-antennas selection diversity. For a 1x1 conventional SISO configuration, the WLAN range is limited within a few offices. We have compared the SISO range achieved using our WLAN transceiver IC to that obtained using commercial SISO WLAN devices made by Cisco and Proxim. Similar SISO transmit ranges were achieved under the same transmit power.

Conclusions

This paper has presented the implementation of an IEEE 802.11a/b/g compliant transceiver RFIC in a 47GHz SiGe BiCMOS process for 2.4GHz and 5.2GHz multi-band MIMO WLAN applications. To the best of the author's knowledge, the transceiver RFIC presented in this paper is the first published design for multi-band MIMO WLAN applications. The transceiver RFIC includes two complete radio paths fully integrated on the same chip. Using a walking IF architecture, the dual radio transceiver employs a single $\Sigma\Delta$ fractional-N synthesizer for RF and IF LO generations that cover the entire IEEE 802.11a/b/g and Japan WLAN bands. Using a total of four dual-radio RFICs a 4X4 MIMO radio link has been implemented and tested under a typical indoor WLAN environment. The 4X4 MIMO radio achieves 15dB of link margin improvement over a conventional SISO radio.

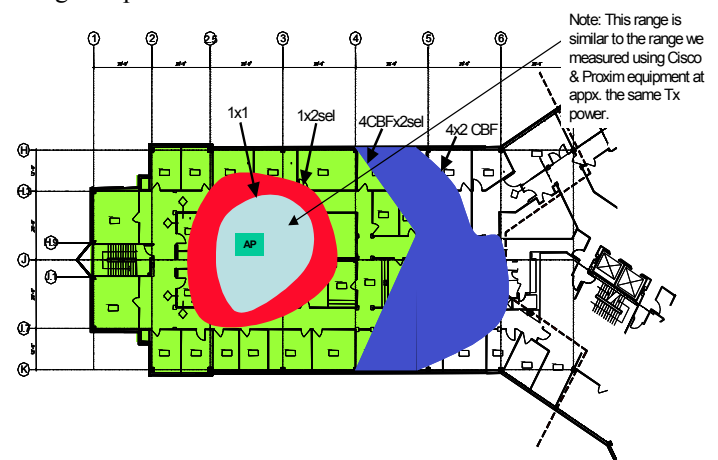


Fig. 7. Demonstration of improved WLAN range using the developed MIMO transceiver RFICs.

Acknowledgment

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