A NOVEL DDS ARCHITECTURE USING NONLINEAR ROM ADDRESSING WITH IMPROVED COMPRESSION RATIO AND QUANTISATION NOISE

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ABSTRACT

This paper presents a novel direct digital synthesis (DDS) architecture that exploits the slope of the sine function for compression of storage requirements. The proposed architecture is compared with the existing DDS architectures and the simulation results demonstrate improved compression ratio and quantization noise.

1. INTRODUCTION

Direct Digital Frequency Synthesizer (DDFS) provides fast switching and precise frequency resolution**.** The simplest architecture for DDFS uses an N-bit accumulator, a read only memory (ROM) and a digital to analog converter, implemented using the same reference clock f_{clk}. The output frequency of the DDFS depends on the N bit input word called Frequency Control Word (FCW). At any instant the value in the accumulator represents the phase of the sinusoid, so it is referred as phase accumulator register. The value in the phase accumulator register is used to address the ROM storing the values of the sinusoid. The output frequency of the DDFS depends on f_{clk} as

$$f_{out} = f_{clk}\frac{FCW}{2^N} \quad (1)$$

The finest resolution possible is

$$f_{res} = \frac{f_{clk}}{2^N} \quad (2)$$

This most common DDFS architecture is presented by Tierney, *et al* in [1]. This architecture however incorporates a large ROM, which restricts high-speed applications and requires huge power consumption. The basic advantages of ROM compression are increased speed, reduced die size, cost and digital switching noise. Hence reduction of the size of the ROM using compression techniques is important for high-speed and low power applications.

This paper presents a compression technique which exploits the variation of slope of the sinusoid to vary the number of values that have to the interpolated between successive ROM values. The sine wave has been assumed to be piece-wise linear between the values stored in the ROM. The technique requires a small multiplier that does not present a bottleneck to low power and high-speed applications. The results show that it can achieve a considerable reduction in ROM size with reduced circuit complexity without degradation in the spurious response. The proposed architecture with non linear addressing meets the performance goal of -90 dBc of spurious rejection with a ROM of 2^6 x 13 + 2^5 x 12 =1216 bits resulting in a compression ratio of 94.3:1.

2. PROPOSED DDS ARCHITECTURE

2.1. Generic architecture

We start with a generic description of the proposed DDS architecture as shown in Fig. 1. In this architecture certain values of the sinusoid are stored in the ROM and the entire sinusoid has to be constructed using these values. The data that are not stored in the ROM have to be interpolated. At any clock cycle the value in the phase register indicates the phase of the sine function. As all the values of the sine function are not stored in the ROM, out of the N bits of the phase address register only the first m bits are used for addressing. The remaining d bits (d = N-m) indicate the relative position of the sine value that has to be interpolated from the value that has been stored in the ROM. The value in the phase register at any instant is given by

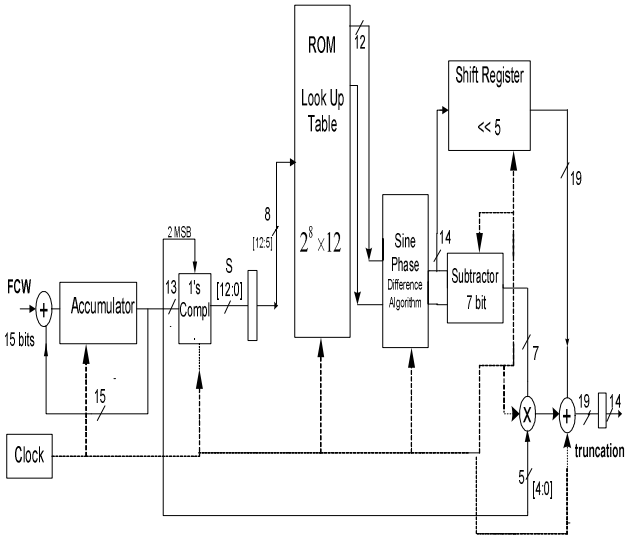

Figure 1. Phase to amplitude conversion using a multiplier.

$$R = FCW \times (i-1) \quad (3)$$

where FCW is the input frequency control word to the phase accumulator and i is the number of clock cycles. The word length of R is N bits. The phase of the sine value that has to be calculated is obtained as

$$B = \frac{2 \times \pi \times R}{2^N} \quad (4)$$

The equation used for calculating the value that has to be interpolated is obtained as

$$\sin(B) = \frac{(\sin C - \sin A)}{(d)} \times \left(di[d-1:0]\right) + \sin(A) \quad (5)$$

where $\sin(B)$ is the sine function value which has to be calculated and $\sin(A)$ and $\sin(C)$ are sine values stored in the ROM where $\sin(C) > \sin(A)$. d = N-m gives the number of values that have to be interpolated if FCW=1. The LSB bits, di (S [d-1:0]) of the phase register, indicate the relative position of the sine value that has to be interpolated from the sine value that has been stored in the ROM. In other words it represents the number of clock cycles required for the value in the phase register to change from A to B. The output of the ROM has a word length of k bits.

The division, requiring more hardware, in Eq. (5) has been modified by multiplying d on both sides, which is equivalent to shifting $\sin(A)$ by a corresponding number of bits.

The output word length of n = k+d bits increases the precision of representation. The n bits are later truncated to k bits to meet the specifications of the DAC. The memory requirements here are 2^m x k bits. The expression $(\sin(C) - \sin(A)) \times (di[d-1:0])$ of the Eq. 5 is calculated either by using a Multiplier (Fig. 1) or an accumulator-counter module in place of the multiplier where the value in the accumulator is added to itself for the number of times indicated by the counter. But the accumulator-counter module runs d times faster than the phase register. This is a bottleneck as the speed of the technology might not be utilized to its fullest advantage. But this structure facilitates to incorporation of a Sigma-Delta modulator at its output before the DAC to attain much better spurious response. In this paper we emphasize the architecture using multiplier.

The normalized slope of the sine wave changes from 1 to 0 as the angle changes from 0^0-90^0. So the difference between successive ROM values is more in the beginning and reduces to almost 0 as the slope approaches zero at 90^0. Therefore, the number of values that have to be interpolated are less in the high-sloped region than the number of values that have to be interpolated in the low-sloped region of the sinusoid. For the architecture mentioned as shown in Fig. 2, the sinusoid is partitioned in to two parts; 0^0-45^0 and 45^0-90^0. As the change in the slope of the sinusoid is less between 45^0-90^0, the number of ROM values stored to calculate the sine value after 45^0, can be reduced to almost half without considerable drop in the spurious response.

The numbers of addressing lines to ROM2 change accordingly to m-1, where m is the number of addressing lines to ROM1. The number of values that have to be interpolated between 45^0-90^0 will increase (twice the number that have to be interpolated in architecture with single ROM) and the relative position of the value that has to be interpolated is indicated by LSB d_2 (d2 = N-m+1) bits. The Eq. 5 gets modified as

$$\sin(B)_2 = \left(\sin(C)_2 - \sin(A)_2\right) \times \left(di[d_2 - 1:0]\right) + \sin(A)_2 \langle\langle (d_2) \quad (6)$$

$$\sin(B)_1 = \left(\sin(C)_1 - \sin(A)_1\right) \times \left(di[d_1 - 1:0]\right) + \sin(A)_1 \langle\langle (d_1) \quad (7)$$

The subscripts 2 and 1 indicate that the values under discussion are from ROM2 and ROM1 respectively. Shifting the $\sin A_2$ value by d_2 will make the output word length as k+d+1 bits. So in order to have uniform output the width of ROM2 is made k-1 instead of k. The memory requirements for this architecture are 2^{m-1} x k + 2^{m-2} x (k-1) bits. In the proposed architecture two major algorithms a) sine function quadrature symmetry and b) sine-phase difference algorithm have also been incorporated.

2. 2. Architecture with Linear Addressing (Single ROM)

As shown in Fig. 1 without losing generality, a phase precision of 15 bits and a ROM of 2^8 x 14 bits have been used to simulate the proposed architecture with a single ROM. The width of ROM has been reduced from 14 bits to 12 bits by using the sine-phase difference algorithm. This makes the ROM size 2^8 x 12 bits. As a ROM of length 2^8 has been used, the sine wave is divided in to 256 parts. Let the 15 bit output of the phase accumulator register be represented by variable S [14:0] where bit 14 is the MSB and bit 0 is the LSB. The first 2 phase bits out of the 15 bits indicate the quadrant of the sine wave. Hence the remaining 13 bits are used to address the sine wave between 0^o-90^o.

The output of phase accumulator register S [12:5] used for addressing the ROM points to a particular ROM value for 32 = 2^{13-8} clock cycles if frequency control word FCW = 1. The value thus obtained from the ROM is shifted left by 6 positions, which is same as multiplying it by 64, and later truncated according to the size of the DAC. The shifted ROM value is added to output of multiplier (or accumulator-counter) module, which acts as the interpolator to obtain the sine function output. The exact value that can be added to the ROM value to obtain the output is decided by the last 5 bits of the phase accumulator register S [4:0].

On the whole the sine value is represented with a precision of 14+5 = 19 bits. This value is truncated to 14 bits before sending it to the DAC. The truncation to 14 bits gives an optimal spurious response when compared to truncation to either 15 or 13 bits.

2. 3. Architecture with Non-linear Addressing (Dual ROMs)

For the architecture with two ROMs mentioned in Fig. 2, the sinusoid is partitioned in two parts; 0^0-45^0 and 45^0- 90^0. This architecture is simulated for dimensions of ROM1 (0^0-45^0) equal to 2^6 x 12 bits and ROM2 (45^0-90^0) equal to 2^5 x 11 bits. From the ROM sizes mentioned the number of values that have to be interpolated are around 64 and 128 for ROM1 and ROM2 respectively if FCW=1.

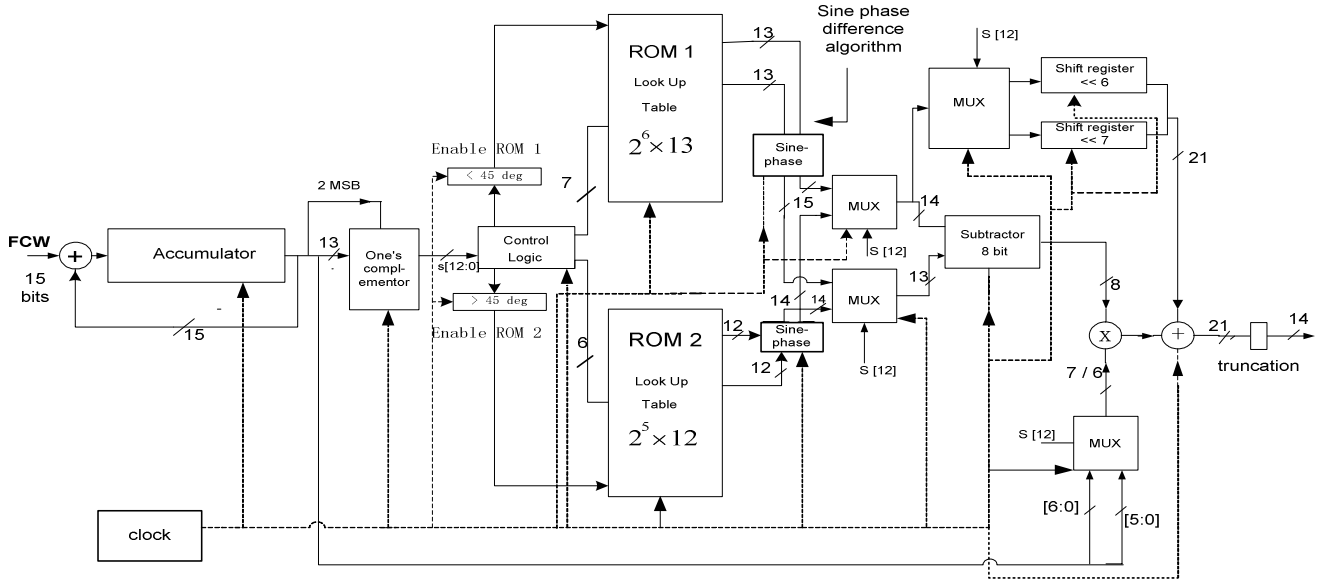

Figure 2. Phase to sine amplitude conversion architecture using non-linear addressing.

The address lines required to address ROM1 are 7 i.e., S [12:6] and that required for ROM2 are 6 i.e., S [12:7]. The values of ROM1 and ROM2 are shifted by 6 and 7 respectively before being added to the output of the multiplier to obtain the output sine value. The position of the sine value that has to be interpolated according to the value in the phase register is given by S [5:0] for sine phase between 0^o to 45^o and S [6:0] for sine phase between 45^o to 90^o. On the whole the sine value is represented with a precision of 15+6 = 21 bits. This value is truncated to 14 bits before sending to the DAC. This technique requires a 7x8 bit multiplier. The increase in the hardware overhead is the trade off for the great reduction in the memory requirement. The sinusoid can further be partitioned to 0^0-30^0, 30^0-60^0, 60^0-90^0 instead of 0^0-45^0 and 45^0-90^0, to obtain further reduction in the memory requirement. The values stored in the ROM are optimized to minimize the mean square error by computer simulations. Worst-case spur amplitude of about -88 dBc is achieved with this method. But the simulation results show that a ROM of 2^6 x 13 + 2^5 x 12 bits provides a spurious rejection of -90.3 dB which provides best compression ratio.

3. SIMULATION RESULTS

A computer program has been written in MATLAB to simulate the proposed architectures. The results hence forth are given for both the non linear as well as the linear addressing architectures. The results are presented for phase bits, P = 15. According to [2], an architecture having uncompressed memory with symmetry considerations, and having the above mentioned phase bits should have worst case spur of -90 dBc, which is obtained from the simulations as well. For the proposed linear addressing architecture with multiplier, ROM size is taken to be 2^8 x 12 (3072 bits). The worst case spur thus obtained in this case is also -90 dBc. For non linear addressing the ROM size used is 2^6 x 13 for ROM1 and 2^5 x 12 for ROM2 adding up to 1216 bits, thus saving 1856 bits as compared to the linear addressing scheme. The error thus obtained is of the order of 10^{-5}, which yields a worst case spur of -90 dBc. The ROM samples have been optimized to reduce the mean square error.

The graph in Fig. 3 shows the variation in the spurious response for different word lengths (width of each value stored in the ROM) of ROM1 and ROM2 with same lengths of 7 and 6 bits respectively. To attain the performance goal of -90dB of spurious rejection, the word lengths of 12 and 11 bits for ROM1 and ROM2 are optimal which result in a worst-case spur of -88dBc. From the graph it can be observed that as the word length of the ROMs is reduced the performance is degraded which is as expected.

From Fig. 4, it can be observed that memory lengths of 2^7 and 2^6 for ROM1 and ROM2 meet the requirement of -90dB of spurious rejection. It can be observed that even though the memory lengths are increased to 2^8 and 2^7 for ROM1 and ROM2 respectively, there is not much improvement in the performance. One reason for this might be the constant word length of the ROMs that limits the performance. By increasing the word length to 13 and 12 bits respectively for ROM1 and ROM2 with memory lengths 2^6 and 2^5 respectively a spurious rejection of -90. 6 dB can be achieved which gives a compression ratio of 94.3:1. The memory dimension is taken as the standard for comparison and considered to be the optimal.

Table 1. Comparison between Nicholas's Architecture and Proposed Architecture for P=15 Bits.

	Worst case spur (dBc)	Memory size (bits)	Compression ratio
Proposed Architecture	-90. 3	2^6 x 13 + 2^5 x 12	94. 3:1
Nicholas Architecture	-90	2^8 x 9 + 2^8 x 4	37:1

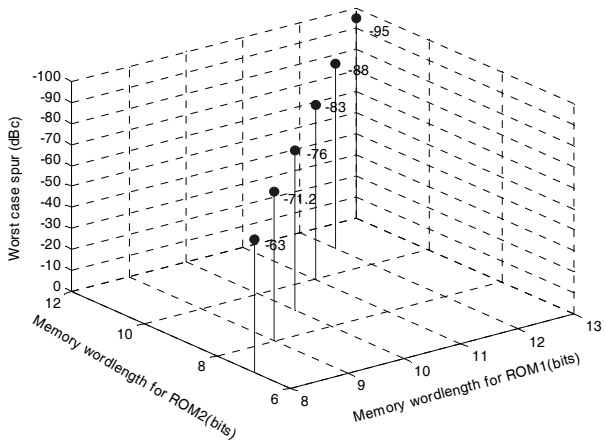

Figure 3. ROM word length vs. worst-case spurs for nonlinear addressing.

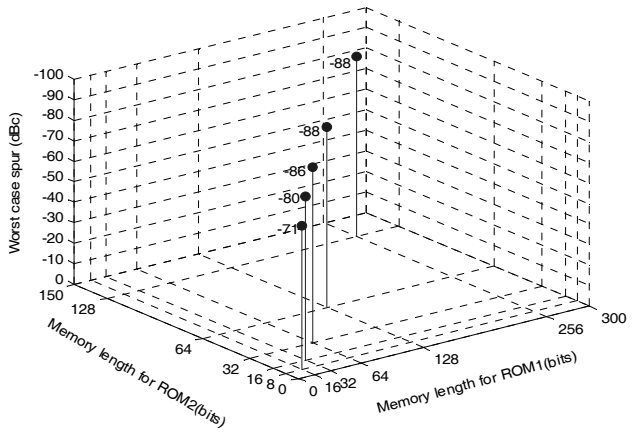

Figure 4. ROM length vs. worst-case spurs for nonlinear addressing.

Table 2. Comparison of the proposed DDS ROM architecture to prior art DDS ROM architectures for P = 12 bits.

Method	ROM Size	Total Compression Ratio	Spectral Purity	Comments
Uncompressed Memory	2^{12} x 8 bits	1:1	-72. 245	Used as reference for comparison
¼ Sine-Wave Symmetry	2^{10}x8 bits	4:1	-72. 245	2 adders required
Hutchison's Technique	2^{7} x 6 bits 2^{10} x 2 bits	11. 64:1	-72. 245	(3,4,3) phase segmentation, 2 adders required
Sunderland's Architecture	2^{7} x 8 bits 2^{6} x 3 bits	27:1	-72. 245	(3,4,3) phase segmentation, 2 adders required
Nicholas Architecture	2^{6} x 7 bits 2^{6} x 3 bits	51. 2:1	-72. 245	(3,3,4) phase segmentation, 2 adders required
Bellaouar's Architecture	2^{5} x 8 bits 2^{5} x 5 bits	78. 8:1	-72. 245	(5,5) phase segmentation, a 5x5 multiplier and 2 adders
This work (linear addressing)	2^{6} x 9 bits	56. 89:1	-71	5 x 7 multiplier, 2 adders
This work (nonlinear addressing)	2^{5} x 9 bits 2^{4} x 8 bits	78. 8:1	-71	6 x 7 multiplier, 2 adders

4. CONCLUSION

This paper presented a novel DDS ROM compression technique based on two basic properties of sine function: (a) piecewise linear characteristic of sinusoid for infinitesimal differences in phase angle, (b) variation in the slope of the sinusoid with phase angle. In the proposed architecture the first property is used to interpolate the values of the sinusoid that have not been stored in the ROM. The second property has been used to increase the number of values that can be interpolated as the slope of the sinusoid decreases. The ROM incorporated in the proposed architecture for a phase resolution of 15 bits is 1216 bits resulting in a spectral purity of -90. 6dBc. The output sine function has a word precision of 15 bits. The proposed architecture has a better compression ratio than the Nicholas architecture with the same hardware efficiency and spurious response.

5. REFERENCES

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