A ΔΣ Fractional-N Frequency Synthesizer with Multi-Band PMOS VCOs for 2.4 and 5GHz WLAN Applications

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Abstract – This paper presents a fully integrated multi-band frequency-synthesizer architecture. The synthesizer is a ΔΣ based fractional-N frequency synthesizer with three on-chip LC tuned VCOs to cover the entire frequency bands specified in IEEE802.11b, and 802.11a WLAN standards. The synthesizer includes a ΔΣ noise shaper, a dead-zone-free phase frequency detector and a fully differential charge pump. The measured in-band phase noise is lower than –93dBc/Hz and the VCO out of band phase noise is -120dBc/Hz at 1MHz offset.

I. Introduction

Over the last few years there has been much interest in monolithically integrated receivers for wireless local-area networks, such as 802.11a and 11b [1]. This market has the potential for high volumes, but for a radio to be successful it will have to be low cost, but provide acceptable performance to support high data rate modulations such as the 64QAM modulation scheme used by these standards. Some of the most crucial subsystems in the radio are the frequency synthesizers.

For multi-standard applications, it is often difficult to cover multiple frequency bands using an integer frequency synthesizer whose step size is limited by the reference frequency. In order to achieve fine step size to cover the multi-band channel frequencies, one has to lower the reference frequency in an integer-N synthesizer design, which results in high division ratio of the PLL and thus high in-band phase noise. In contrast, a fractional-N synthesizer allows the PLL to operate with a high reference frequency and meanwhile achieve fine step size by constantly swapping the loop division ratio between integer numbers, thus averaging the division by a fractional number. This improved performance comes at the penalty of fractional spurious tones, which occurs due to the periodical division ratio variation. Fractional spurs may be removable by using a high order loop filter if the closet spur is not too close to the carrier. Note that spacing of the closet spur to the carrier is determined by the synthesizer step size. For a synthesizer with a step size smaller than the LPF bandwidth, it is thus practically impossible to remove the fractional spurs by using loop LPF. Reducing the loop bandwidth to combat the fractional spurs will the pay the penalty of long lock time and increased VCO noise contributed to out-band phase noise. The best solution to remove the fractional spurious components for a synthesizer with fine step size is to employ a delta-sigma noise shaper in the fractional accumulator. A delta-sigma fractional-N architecture will thus be selected for our multi-band synthesizer designs with a multi modulus divider with a division ratio from 64 to 127 [2]-[4].

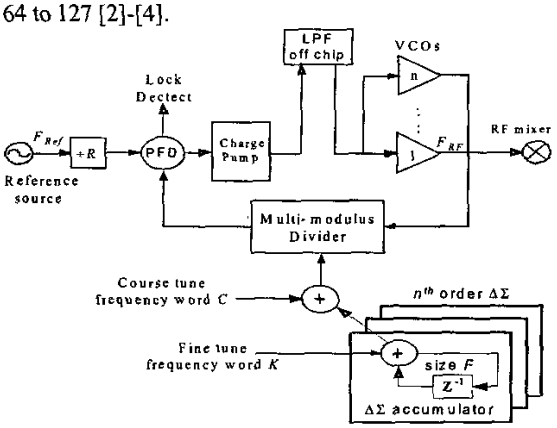

Fig. 1. Delta-sigma fractional-N frequency synthesizer for multi-band WLAN transceivers.

II. Phase Frequency Detector and Charge Pump

A SR latch based digital tri-state type phase frequency detector (PFD) is chosen to provide dead-zone-free phase and frequency comparison between the reference frequency and VCO divided frequency (Fig. 5). It contains an exclusive-OR gate that can be used as a lock indicator. This PFD has only one zero-crossing over its phase detection range, which ensures that the device does not lock to the 2nd and 3rd harmonics.

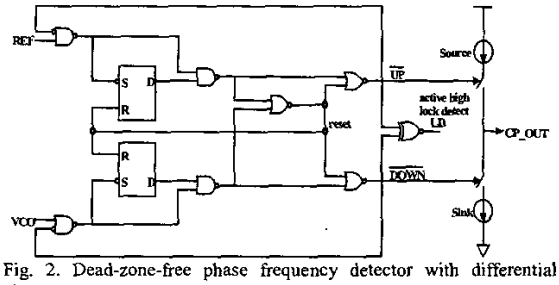

Fig. 2. Dead-zone-free phase frequency detector with differential charge pump.

A charge pump follows the PFD. The charge pump is fully differential with single-ended output as shown in Fig. 6. The PFD input phase error is represented by the PFD UP and DOWN output pulses, which control the CP source and sink current sources, resulting in current flow in or out of the charge pump. The gain of this PFD/charge pump combination is given by:

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$$K_{pdcp} = \frac{Icp}{2\pi} \quad (4)$$

The source/sink current I_{cp} can be programmed for 2 different settings, namely, 500μA and 850μA. These can be used to adjust the loop gain to compensate for VCO gain variations during wide band tuning.

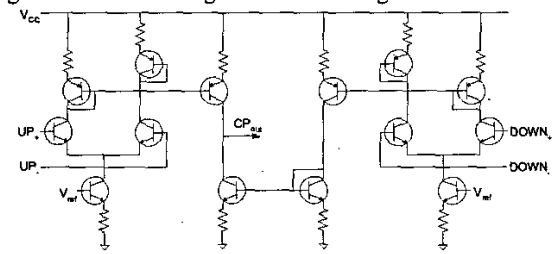

Fig. 6 Differential charge pump circuitry.

III. VCO Design

The core of the oscillator is formed using two PMOS transistors M_1 and M_2 connected in a negative resistance configuration and attached to the LC tank of the VCO as shown in Fig. 3. The tank itself consists of two inductors L and a pair of pn junction varactors C_{var}.

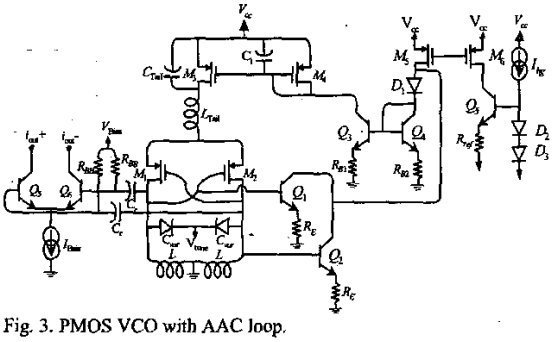

Fig. 3. PMOS VCO with AAC loop.

pn junction varactors are preferred in this technology because of their high Q at the frequencies of interest (in this case 2.5 and 5GHz). However, they have one critical draw back. They have a parasitic substrate diode associated with the p side of the junction that has a low Q and parasitic capacitance. Unless the n side of the diode is connected to ac ground, then the structure will include this lossy substrate diode impacting VCO performance [5]. This is the reason that the PMOS VCO core of Fig. 3 is preferred. In this case the tank can be connected to ground rather than DC so that the diodes can be connected in the proper polarity without the need for any additional biasing. PMOS also offers the advantage of higher output swing than bipolar provided high phase noise at offset frequencies below 100kHz (due to high flicker noise) can be tolerated. This is due to the fact that the PMOS transistors can be operated into saturation without affecting the VCO noise performance.

The tank inductors are made as large as possible to maximize the tank equivalent parallel resistance while still allowing the varactors to be large enough so that parasitic capacitance does not reduce the available frequency tuning range to an unacceptable level. The PMOS transistors themselves are sized so that they have a large DC V_{GS} voltage leaving enough headroom to accommodate the current source M_3. The inductor L_{Tail} and the capacitor C_{Tail} form a filter that is designed to filter out noise from the bias circuitry so that it does not affect the phase noise of the VCO [6].

The current through the VCO must be set large enough to maximize the voltage swing at the tank to minimize the phase noise of the circuit. The swing will be maximized when the transistors are made to alternate between saturation and cut-off at the top and bottom of the VCO voltage swing. Once the transistors reach this voltage swing level, raising the current will not cause the swing to grow any more, will reduce the phase noise, and will waist current.

It would be impossible to set the current in the VCO to an optimal level with any accuracy. Worse, the current required by the VCO to achieve a given output level will change over the frequency tuning range (with changes in varactor and inductor Q) over temperature and over process. Thus, some feedback mechanism must be implemented to set the current.

The automatic amplitude control (AAC) loop used in this design is also shown in Fig. 3. Here transistors Q_1 and Q_2 are set nominally in cut off and behave as class C amplifiers. They do nothing until the VCO amplitude reaches the desired level (set by choosing an appropriate value for R_E). Once this level is reached, Q_1 and Q_2 turn on briefly at the top of the swing and steal current away from Q_4. This in turn reduces the current flowing in the oscillator until it is just enough to provide that level of output swing. The diode D_1 is included to provide a level shift so that the transistors Q_1 and Q_2 are not in saturation. Resistors R_{B1} and R_{B2} are included to degenerate the current mirror formed by Q_3 and Q_4 and act to reduce the noise it generates. The current source I_{bg} is a reference current generated by the bandgap circuit on the chip. Diodes D_2 and D_3 are used to provide a low impedance to short out the noise generated by the bandgap and then the mirror formed by M_5, M_6, and Q_5 pass the reference current on into the AAC loop. C_1 is included to form a dominant and controllable pole in the feedback loop so that stability of the feedback loop is assured for all operating conditions. Note also that Q_1 and Q_2 are connected in such a manner so that they do not load the tank and provide additional loss when they turn on, impacting phase noise. This is a key advantage over previous designs that loaded the tank with the r_e of the limiting transistors [7]. Thus, in this case these transistors do not act as clamping diodes.

An output buffer is also included that isolates the tank from all the circuitry in the transceiver that it must eventually drive. This is a bipolar buffer with a current output that is combined with other cores so that they can be conveniently switched on or off without loading each other. The full circuit has three VCOs so a digital input to the VCO will control when the current sources are on and when the references are shorted out so that the circuit is not powered. The only other inputs are the

band gap reference current and the control voltage for the VCO frequency tuning port.

The complete VCO subsystem is shown in Fig. 4. Each one has its varactor and inductor size adjusted so that the appropriate frequency range can be covered. The lower VCO is tuned for the 2.4GHz band (3.216GHz-3.296GHz), while the upper two VCOs cover the 5GHz band (4.144GHz-4.256GHz and 4.596GHz-4.644GHz). There is a control in each of the VCOs that will short out the band gap current and so that VCO will only operate when this signal is high. Thus it is intended that only one of the VCOs will operate at a time. All three of the open collector buffers are tied together and brought to load resistors R_C. Next the signal is driven into two buffer transistors Q_{19} and Q_{20} that are driven with enough current to drive the 5GHz divider and three additional output buffers. The three buffers are fed to the receiver RF mixer the transmit mixer and to the synthesizer buffer. The 5GHz divider produces four outputs, but only two are used to drive another set of buffers which in turn drive the 2.5GHz buffer. All four of the outputs of the 2.5GHz buffer are used to produce quadrature differential signals that drive both transmit and receive IF stage mixers. Buffers are also included at the output of the divider to provide enough drive for these mixers.

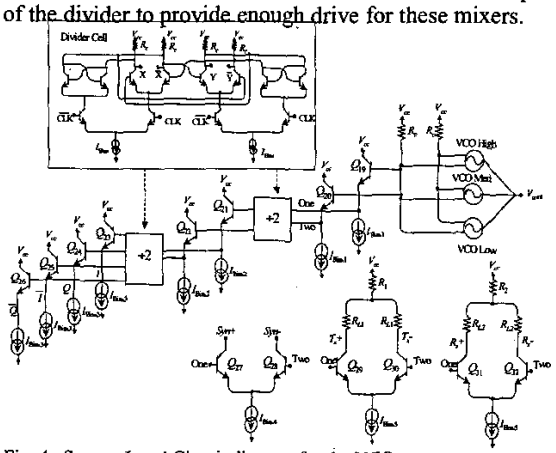

Fig. 4. System Level Circuit diagram for the VCO.

The divider circuits consist of two latch circuits connected in feedback. The input to the circuit is a differential square/sine wave fed into CLK and CLK bar inputs. The circuit produces two quadrature outputs at half the input frequency. The bias current (set using the band gap reference) and resistors were sized so that the circuit would run at either 2.5 or 5GHz and the transistors were made close to minimum size for fast switching and so they added minimal capacitance to the circuit.

IV. Synthesizer Phase Noise Analysis

The PLL noise is partitioned into six different blocks, which are modelled to predict the composite PLL noise. Fig. 5 illustrates the noise contributing blocks. The VCO (noise source 1) typically dominates the noise outside the PLL loop bandwidth and noise sources 2-6 contribute to the overall noise inside the PLL bandwidth. The bandwidth is typically set to lower the overall integrated noise, by choosing a bandwidth at the intersection of the total in band and out of band contributors. Fig. 6 shows the simulated phase noise contributors (labelled as shown in Fig. 5) and Fig. 7 shows the intersection of the total in band contributors with the VCO phase noise curve. This occurs at approximately 150kHz, which corresponds to the optimum loop bandwidth for lowest integrated phase noise. The total simulated jitter was .84° for a 100Hz to 10MHz integration bandwidth.

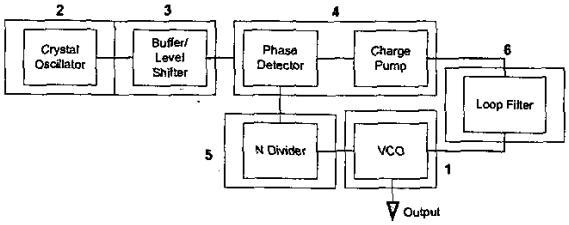

Fig. 5. PLL noise sources partitioning.

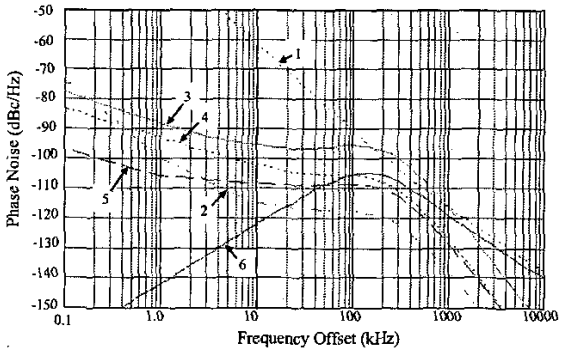

Fig. 6. PLL Noise Contributors.

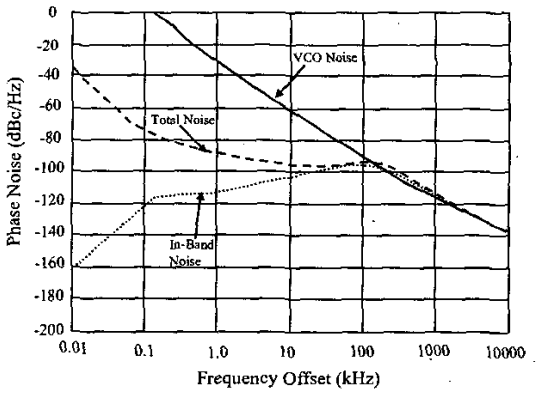

Fig. 7. Optimum Crossover Point (150kHz).

V. Measured Results

The synthesizer was fabricated in a 47GHz SiGe BiCMOS process with 0.5µm lithography. The back end of the process featured thick aluminium metallization designed to provide high quality inductors. The synthesizer was embedded in with the rest of the circuitry that formed the WLAN transceiver. A die photo of the chip is shown in Fig. 8. The chip measured 4mm by 3.1mm on a side and the synthesizer itself occupied an area of 2.3mm by 1.4mm.

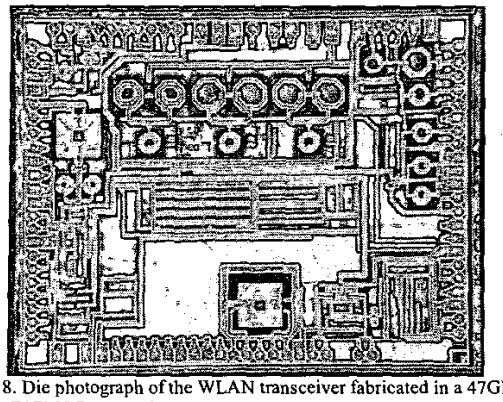

Fig. 8. Die photograph of the WLAN transceiver fabricated in a 47GHz SiGe BiCMOS processing.

Table I: Summary of Synthesizer Performance

Parameter	Performance
High VCO Tuning Range	4.93 – 5.35 GHz
Med VCO Tuning Range	4.47 – 4.91 GHz
Low VCO Tuning Range	3.52 – 3.87 GHz
VCO Phase Noise	-120dBc/Hz at 1MHz
In Band Phase Noise	-93dBc/Hz
Loop Corner Frequency	150KHz
Reference Frequency	40MHz
Channel Resolution	1MHz
Reference Spurs	- 56 dBc
Power Supply	2.75V
Current Consumption	84mA
Integrated Phase Noise	.8°rms

The synthesizer draws a current of 84mA from a 2.75V supply. Fig. 9 shows a plot of the measured phase noise of the system using the lower 5GHz frequency band. For comparison the simulated phase noise is shown on the plot as well. It this curve was derived from the analysis of section VI and shows close agreement with the measured results. From the plot it can be seen that it has an in band phase noise of –93dBc/Hz, and the VCO has an out of band phase noise of –120dBc/Hz at 1MHz offset. The integrated phase noise was less than .8°rms when integrated from 10Hz to 10MHz. Using the 2.5GHz VCO the phase noise was slghty better (.7°rms) and using the upper 5GHz band slightly worse (.9°rms). Some variation was noted due to VCO gain variation, but currently the loop and charge pump current are being optimised to remove these variations that are on the order of .3°rms. Reference spurs were less than -54dBc. The VCOs were tuneable from 3.52 to 3.87, 4.47 to 4.91 and 4.93 to 5.35GHz. They ran slightly fast (about 5-10%) from simulation and thus could not be locked over all channels. This will be corrected in the next chip iteration. Table I summarizes the synthesizer performance.

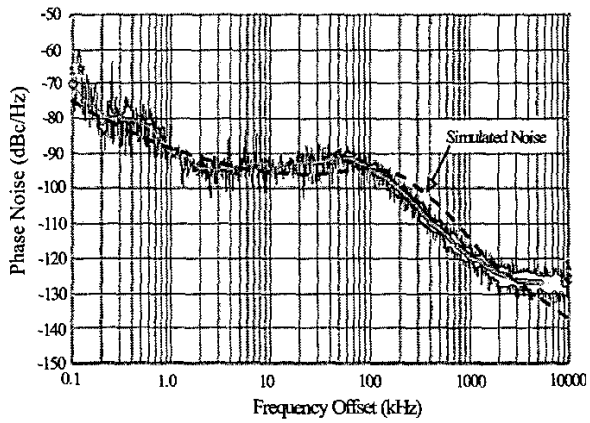

Fig. 9. Measured and simulated synthesizer phase noise plot.

VI. Conclusions

This paper has presented the implementation a ΔΣ based dual-band fractional-N frequency synthesizer for 2.5GHz and 5GHz WLAN applications in a 47GHz SiGe BiCMOS process. The synthesizer achieves an integrated phase noise of less than .8°rms.

Acknowledgements

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