

A Fully Integrated Multiband MIMO WLAN Transceiver RFIC

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Abstract—A multiple-input/multiple-output (MIMO) transceiver RFIC compliant with IEEE 802.11a/b/g and Japan wireless LAN (WLAN) standards is presented. The transceiver has two complete radio paths integrated on the same chip. When two chips are used in tandem to form a four-path composite beam forming (CBF) system, 15 dB of link margin improvement is obtained. The transceiver was implemented in a 47-GHz SiGe technology with 29.1-mm² die size. It consumes 195 mA in RX mode and 240 mA in TX mode from a 2.75-V supply.

Index Terms—802.11 a/b/g, multiple-input/multiple-output (MIMO), RFIC, SiGe, transceivers, wireless communications, wireless LAN (WLAN).

I. INTRODUCTION

THE ever-increasing demand for wireless and multimedia applications [1]–[9] such as video streaming keeps pushing future wireless LAN (WLAN) systems to support much higher data rates (100 MB/s up to 1 GB/s) at high link reliability and over greater distances. Next-generation wireless communication systems are focused on increasing the link throughput (bit rate), the network capacity, and the transmit range. A multiple-input/multiple-output (MIMO) system in combination with space–time signal processing allows increased data rate and/or improved transmission range and link reliability without additional costs in bandwidth or transmitted power. MIMO techniques include space–time coding (STC) and space division multiplexing (SDM). STC increases the performance of the communication system by coding over the different radio paths, whereas SDM achieves a higher throughput by transmitting independent data streams on the different radio paths simultaneously and at the same carrier frequency. MIMO systems using multiple antennas allow enhancements to the existing IEEE 802.11 WLAN technology [10], [11]. The next generation of WLAN standards could be based on MIMO technology to achieve high data rate and improved range. This

is especially important for 802.11a applications due to the 6-dB extra path loss at 5.2 GHz compared to 2.4 GHz under nominal conditions. Indoor environments, where most of the WLAN systems are deployed, are typically characterized by richly scattered multipath signals. Under these conditions, having MIMO will lead to dramatic performance improvements.

This paper presents an RFIC transceiver designed for MIMO WLAN applications. Two complete a/b/g dual-band radios are integrated on a single chip and can be used to form a two-radio-by-two-radio link. Additionally, two chips can be used together to form a 4 × 4 link. With the exception of the synthesizer loop filter, the LNA, and power amplifier (PA) matching networks, the entire 2 × 2 MIMO radio system is integrated in one chip with 29.1-mm² die size. Two chips may be used together in a master-and-slave configuration to form a 4 × 4 MIMO radio transceiver system.

II. OVERVIEW OF MIMO TECHNOLOGY

MIMO technology has received increased attention recently for wireless and radar applications. It allows greater transmission range at the same transmitted power level and for the same data rate [12]. Alternatively with MIMO technology, the system signal-to-noise-ratio (SNR) requirement can be relaxed for a given data rate. Fig. 1 compares the average SNR per antenna required for a given data rate using different radio configurations. In the graph a conventional single-input/single-output (SISO) 1 × 1 link, namely, one transmitter one receiver architecture is compared to various MIMO systems such as a 1 × 2 select diversity link (spatially separated receiver or transmitter antennas to select the strongest signal), a 4 × 4 link that uses composite beam forming (CBF) technology and maximal ratio combining (MRC), and a vector CBF (VCBF) link.

The term CBF is used here to describe the co-phasing and combining the data streams on the receive side of the link for each OFDM subcarrier, i.e., the MRC, and transmission of the complex conjugate of the receive antenna weights for each OFDM subcarrier in the transmit direction (the inverse MRC in the transmit direction). VCBF is a vectorized generalization of CBF. A 4 × 4 VCBF system transmits and receives four data streams at the same time and frequency, where each stream at the transmitter is weighted by the eigenvector of the channel response matrix (a 4 × 4 matrix in this case, which is full-rank in most real-world cases). With VCBF, each of the four “spatial streams” is beamformed on the transmit side and then MRC is performed on the receive side just like a CBF system. The advantage of CBF over VCBF is that it does not require both

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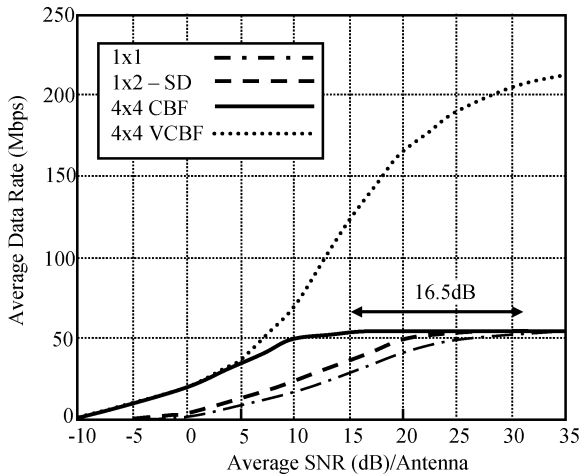


Fig. 1. Data rate versus required SNR for a SISO 1×1 link and various MIMO links including 1×2 , 4×4 CBF, and 4×4 VCBF.

the transmitter and receiver to have MIMO capability, thus making it more backward-compatible.

The RFIC implementation in this paper supports CBF technology. VCBF represents a potential future MIMO application, which could be used with this radio, but would require new technology in the baseband design. From Fig. 1, it can be seen that, at a data rate of 54 MB/s, the SNR required for a 4×4 CBF link is 16.5 dB lower than that required by a 1×1 link, clearly demonstrating the advantages of the proposed MIMO radio technology.

III. MIMO TRANSCEIVER DESIGN

As a tradeoff between the level of integration and complexity/yield, this work integrated two multiband dual-radio paths on the same die. A 2×2 MIMO link can therefore be formed using only two MIMO transceiver ICs, compared to four SISO chips. The presented MIMO WLAN transceiver IC supports the 802.11b/g and 802.11a lower and middle bands. In this system, only two radios were integrated, integrating more radios together would have led to more expensive packaging, lower yield, and, for many applications, a 2×2 MIMO system is sufficient. However, if more than two radios are desired in a particular application, then even two, three, or more dual-radio transceiver chips can be used in a single link, provided that their local oscillations (LOs) are all phase-synchronized. For instance, two pairs of dual-radio transceiver chips can be used to form a 4×4 MIMO radio system as shown in Fig. 2. Each transceiver pair consists of a master and a slave dual-radio transceiver chip. The slave chip synchronizes its LO to the master chip by means of the LO porting circuitry, in which the master chip's $\Sigma\Delta$ fractional- N synthesizer can be used to drive the slave chip's LOs for synchronization. To the best of the authors' knowledge, this work is the first WLAN MIMO integrated transceiver reported.

MIMO transceiver RFIC design is a challenge due to the following issues.

- 1) When multiple radios are integrated in the same die, interference among the transceiver building blocks will be a

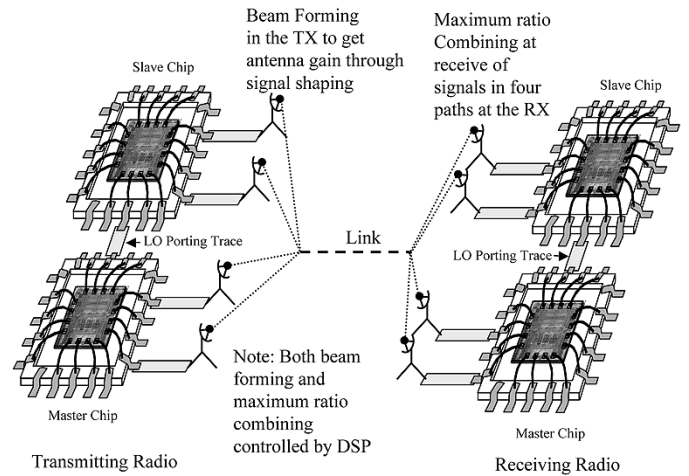


Fig. 2. 4×4 MIMO system for WLAN applications.

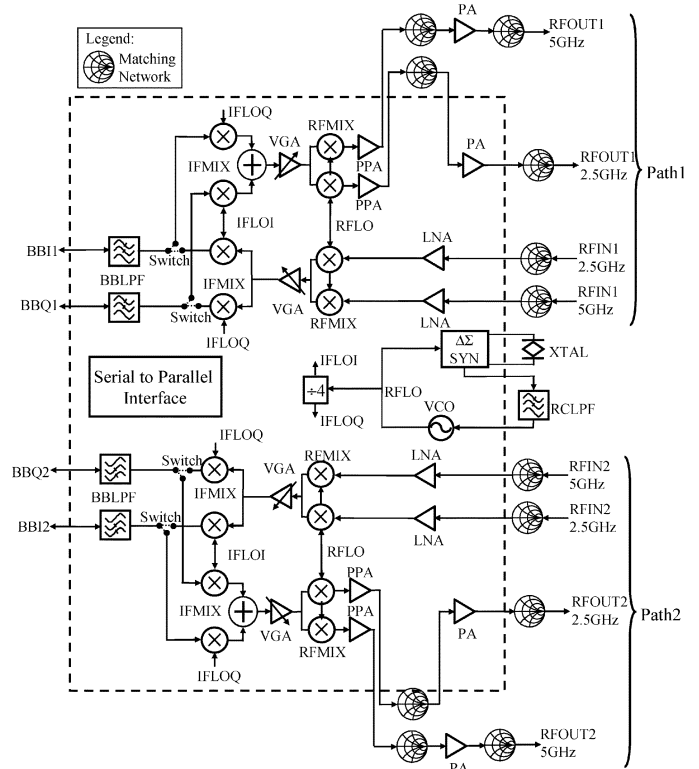


Fig. 3. MIMO transceiver architecture.

big concern. In particular, when multiband power amplifiers are in operation, their radiation may injection-lock the VCOs and generate crosstalk noise through substrate, package, power supply, or ground. Careful floor planning and proper isolation of the MIMO transceiver layout are critical. The on-chip synthesizer has been carefully designed so that all of the VCOs are operating at different frequencies from the PA transmit bands.

- 2) In a MIMO system, all of the LOs in different radio paths need to be synchronized. MIMO calibration requires a loop-back measurement through the transmit and receive paths. A loop-back measurement is performed by connecting the transmitter to one antenna and the receiver to the other antenna on the same chip and then matching

the gain and phase of both paths. To maximize the gain from transmitter beam forming and receiver MRC requires matching the gain and phase of each path being combined. If the LO phases of the MIMO radios shift relative to each other, the performance of CBF operation will be degraded. However, synchronizing the LOs at high frequencies such as 5.3 GHz for the 802.11a band is not trivial. If more than one PLL is used to generate the LO tones, static phase error and time-variant phase variations among the PLLs will occur. To avoid many of these LO phase drift issues resulting from the use of multiple PLLs, a single-frequency synthesizer is used to generate all of the RF and IF LOs. An optional LO porting block was added to the architecture, allowing for sharing of a common-system RF LO among multiple MIMO chips [7].

- 3) The isolation between transmitter paths must be as high as possible to maximize the gain from CBF. An isolation of 30 dB between transmitters at the PA outputs results in 1-dB degradation from maximum possible gain.
- 4) The isolation between receiver paths must be maximized in order to maximize the gain from MCR. In this application, it was desired to have an isolation of better than 40 dB.

The dual-radio MIMO transceiver block diagram is illustrated in Fig. 3. Each individual multiband radio consists of a receiver (RX), a transmitter (TX), a baseband filter, a shared frequency synthesizer, bandgaps, control logic, and a serial-to-parallel interface (SPI) for transceiver programming. The transceiver is a superheterodyne architecture with sliding intermediate frequency (IF). In this architecture, only one frequency synthesizer is required to generate the first LO [13]. The second LO is obtained by dividing the first LO by four. This reduces not only the number of frequency synthesizers, but also the number of LOs and IFs that require synchronization for a MIMO transceiver system. The drawback of the sliding IF architecture is that the system must tolerate a wider IF bandwidth. In this case, the IF signal varies from 800 to 1070 MHz.

The receiver consists of single-ended cascoded LNAs, down-conversion mixers, a variable-gain amplifier (VGA), an I/Q demodulator, and baseband filters. There are two LNAs, one for 2.4-GHz and another for 5-GHz bands. The RF mixer outputs drive the VGA, which provides up to 23 dB gain in 3-dB steps with a total of 15 steps. The VGA output drives the IF quadrature demodulators, which generate the I/Q baseband signals. Careful layout in the I/Q demodulator ensures good quadrature matching. Finally, the I/Q demodulator outputs drive the tunable baseband filters.

Each TX chain consists of IF quadrature modulators, VGAs, and two RF upconversion mixers, predrivers, and PAs for 2.4- and 5-GHz bands, respectively. The VGA has a gain range of 39 dB and a gain step of 3 dB. Each RF mixer is followed by an on-chip image rejection filter, which has a low-pass characteristic for the 2.4-GHz band and a bandpass characteristic for the 5-GHz band, respectively. The output power detectors are integrated with the PA, and no off-chip components are required. The matching network for the 2.4-GHz on-chip PA was off chip to provide access to the signal before the PA, to save

chip area, and to allow this network to be adjusted after fabrication. A future revision of the chip could move this matching network on-chip.

The baseband filters were implemented using active-RC circuits due to the demanding requirement for high linearity. The filter can be programmed to have a narrowband mode with a 9.8-MHz corner (fifth-order elliptic) and wideband mode with a 41.75-MHz corner (seventh-order Chebyshev). The filter corner frequency is digitally tunable in 16 steps in order to compensate for the variations over process and temperature. In order to save silicon area, a multiplexing scheme is implemented such that the same filter cores are used for both transmit and receive modes. The mixer dc offset is compensated using digital-to-analog converters (DACs) with feedback controls provided by the baseband IC.

IV. TRANSCEIVER BUILDING-BLOCK CIRCUITS

In the following sections, the major building blocks of the MIMO transceiver will be described in more detail at the circuit level.

A. Receiver Front-End

The multiband receiver front-end schematic is shown in Fig. 4 where bias circuitry is not included for simplicity. The LNAs are single-ended in order to reduce silicon area, reduce power consumption (only 5 mA of dc current per LNA), reduce the pin count for the chip, and remove the need for an off-chip transformer at the input. They are tuned cascode-common-emitter LNAs with inductive emitter degeneration for increased linearity. The 5-GHz LNA (Q_{11} , Q_{12}) has high gain only. The 2.4-GHz LNA has high-gain and low-gain modes that step the gain by 20 dB. For the high-gain mode, the cascode amplifier (Q_0 , Q_2) is powered while the common-base amplifier (Q_3) is off. For low gain, the NMOS switch is turned on and Q_3 is turned on while Q_0 is powered down. The LNAs were spaced as far apart as possible to reduce coupling, which was especially important, as they are single-ended. The RF mixers are Gilbert cell mixers with inductive degeneration for increased linearity with low noise. The 2.4-GHz and the 5.2-GHz mixers are connected together at their IF outputs in order to share external inductive pull-ups (L_{10} , L_{11}) which tune the IF port to 1 GHz as well as increase voltage headroom. This provided flexibility in the prototype design and the ability to test the front-end separately if need. These inductors would have been moved on chip in the next revision of the design. This creates a bandpass response at the IF output which removes higher order harmonics. The 2.4-/5.2-GHz front-ends provide 25/20 dB of voltage gain, respectively.

B. Receiver IF VGA

The VGA is designed to operate at frequencies of 800 MHz-1.2 GHz and it has 16 gain settings. The circuit level schematic of the VGA is shown in Fig. 5. It has three amplifiers that each consists of two differential pairs with their collectors tied together. A digital input to the block controls which of the two stages is on. Current flows through one differential pair, but never both. The gain of the stage is given roughly by the ratio

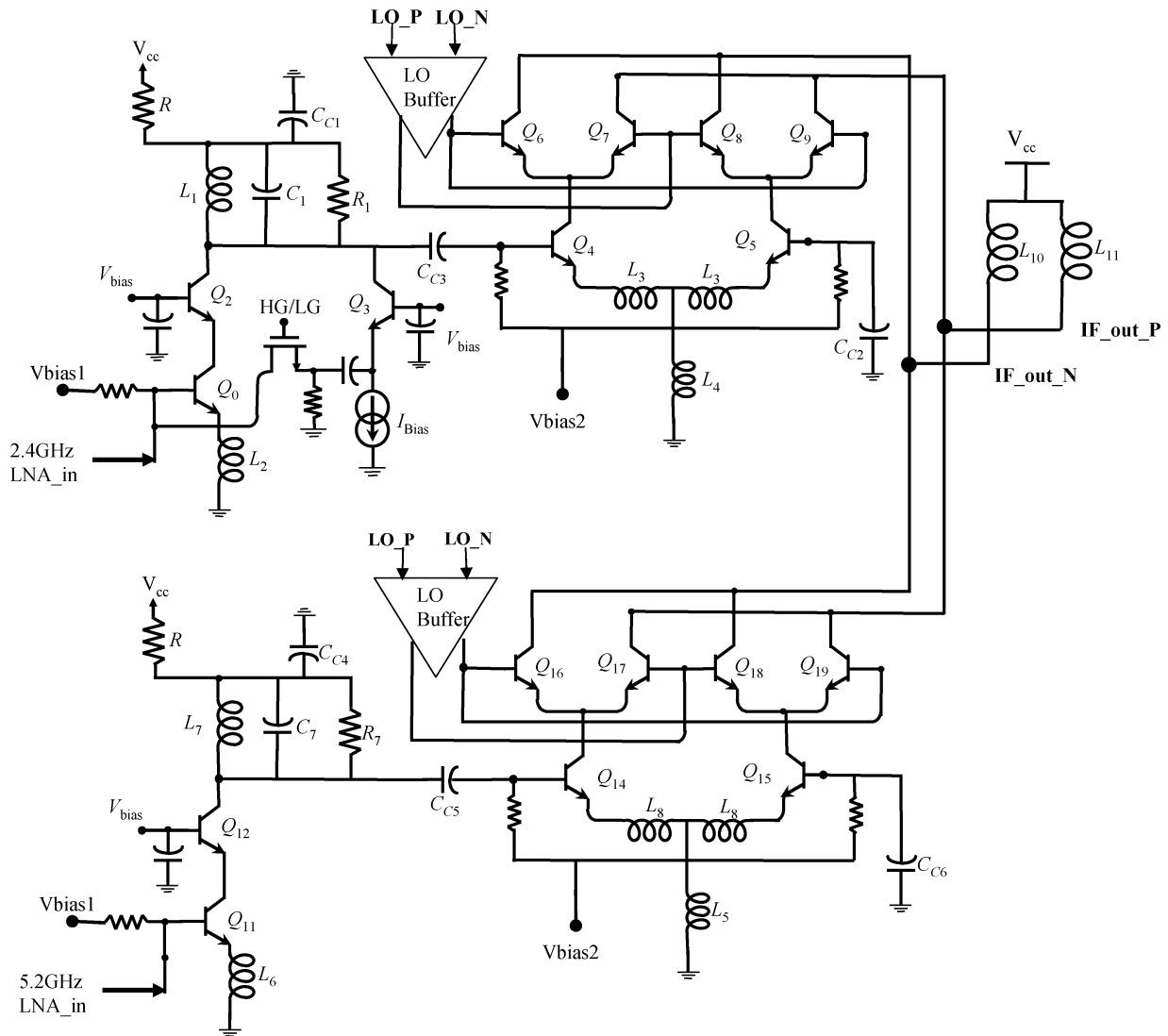


Fig. 4. Schematic diagram of the dual-band receiver front-end.

of the load resistors to the degeneration resistors. Stages 1, 2, and 3 step the gain by 25.6, 12.8, and 6.4 dB, respectively. The capacitor C_c is added to the circuit so that the output bias of the RF mixer does not affect the bias of the circuit. The stage-2 load includes two PMOS transistors M_3 and M_4 to adjust the total load resistance, stepping the gain by 3.2 dB. In order to drive the IQ mixer stage that follows the VGA, two output buffers are included in stage 3. The IQ mixer stage itself consists of two conventional Gilbert cell mixers driven by phase-shifted LO tones.

C. Tunable Baseband Filter

The core of the tunable baseband filter has two modes of operation: a narrowband mode with 9.8-MHz corner frequency mode where the filter is configured as a fifth-order elliptic ladder filter and a wideband mode with 41.75-MHz corner frequency mode where the filter is configured as a seventh-order Chebyshev filter made up of cascaded biquads. The wideband mode is designed to enable the patented features of spectrum management [14], which can detect the surrounding WLAN spectrum

such that the users can coordinate and manage the spectrum in a shared wireless environment. Switching between the two modes is accomplished by designing multiplexers into the input stages of the op-amps. The two modes of operation will be described individually first, and then the method of switching between the two modes will be discussed. The filter is switched from narrowband to wideband by means of a control register bit, which may be accessed through the I2C bus.

In the narrowband mode of operation, the filter core is a differential implementation of the fifth-order elliptic active RC ladder filter as shown in Fig. 6. The filter is built with five fully differential op-amps. The gains of -1 are simply implemented by cross-connecting the fully differential outputs of the op-amps.

In the wideband mode of operation, the seventh-order Chebyshev filter is constructed using cascaded blocks as shown in Fig. 7. The first block has a single time constant, while the other three blocks in the center are biquads and the last block is an output buffer. The filter implementation is fully differential. The five op-amps in this configuration are the same op-amps used for the fifth-order elliptic filter. The tuning is accomplished by

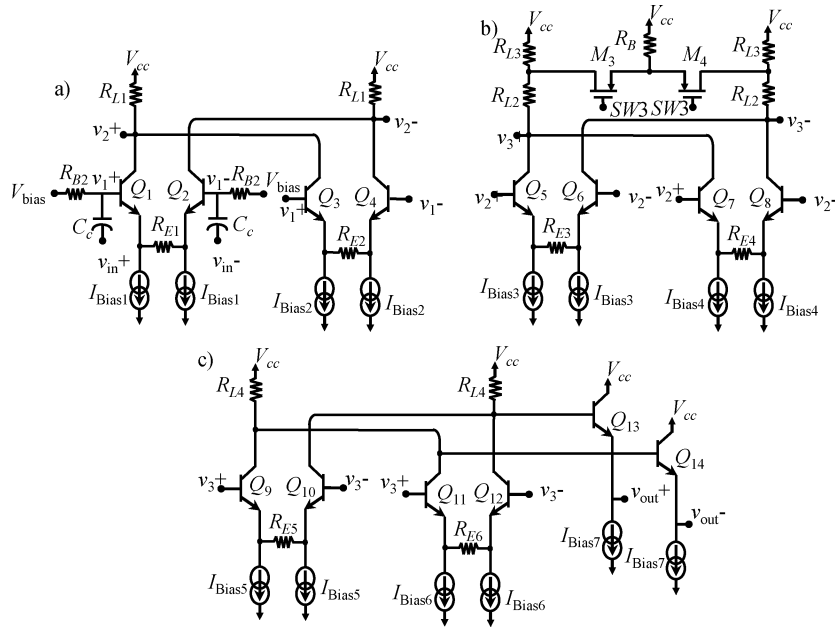


Fig. 5. Schematic diagram of (a) stage 1, (b) stage 2, and (c) stage 3 of the IF VGA.

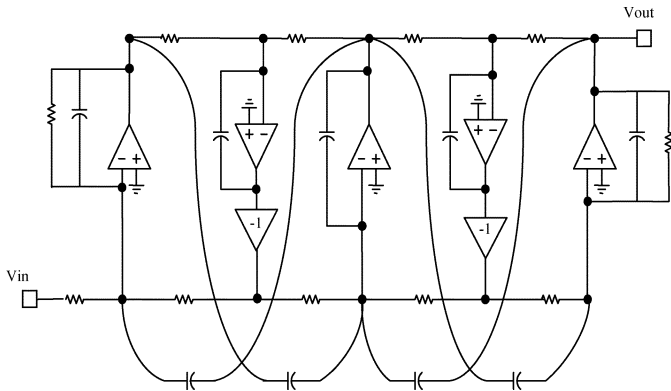


Fig. 6. Fifth-order elliptic filter for the narrowband mode.

adjusting the resistor values similar to [15]. A successive approximation algorithm selects an optimal setting.

D. IQ Modulator

The in-phase and quadrature phase (IQ) modulator upconverts two signals in quadrature from baseband (BB) to an IF signal in the range of 0.8–1.1 GHz. The I and Q signals are combined with an adder as shown in the block diagram of Fig. 3. In the mixer circuit, the adder is simply implemented by adding the output currents of the two mixers through the same load resistors R_L as shown in Fig. 8. The two mixers are two identical Gilbert cells with quadrature LO frequencies provided by the VCO divided by four.

Two input signals are fed differentially to the input terminals BB_I and BB_Q . The inputs are mixed with the frequencies in the LO upper quad, and the resultant currents are combined at the loads R_L provide differential outputs. The BB-input dc level is provided from the baseband filters. The mixers include the LO buffers that sharpen the transition of the LO signals and hence reduce the noise feeding through the quad transistors. The

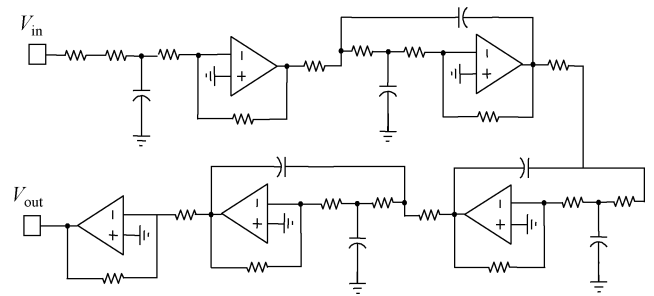


Fig. 7. Schematic of the seventh-order Chebyshev filter for wideband mode.

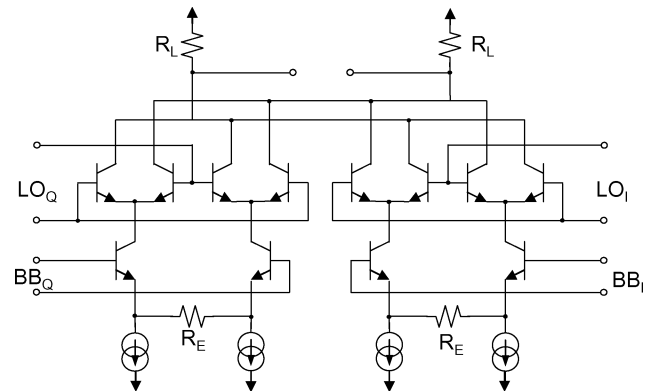


Fig. 8. IQ modulator circuit schematic.

required linearity is achieved by adjusting degeneration resistor R_E and bias current in the current sources.

E. Transmitter Variable Gain Attenuator

The transmitter variable-gain attenuator (TVGA) reads in a 4-b input and attenuates the input signal by 0 to 39 dB with a step size of 3 dB. The TVGA consists of translinear gain cells and a dc control block with digitally controlled current sources.

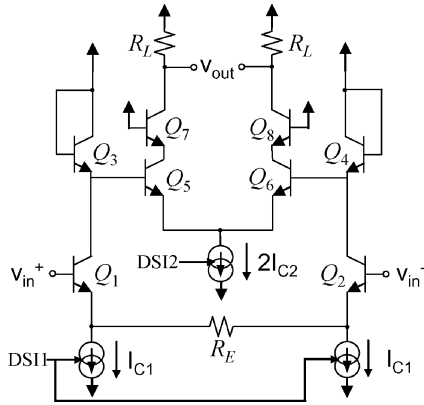


Fig. 9. VGA translinear gain-cell schematic.

The translinear gain cell is shown in Fig. 9. The differential gain is given by

$$A_v = \frac{I_{C2}R_L}{I_{C1}R_E}. \quad (1)$$

Therefore, the gain of the cell can be adjusted by changing the digitally switched input currents (DSI1 and DSI2). The cascode transistors (Q_7 and Q_8) are added to reduce the Miller capacitance and hence to improve the frequency response.

F. Upconverter Mixer and Preamplifier

The upconverter converts its 1.1-GHz IF input to 2.4- and 5.2-GHz RF output. The block consists of an upconversion mixer, a differential-to-single-ended converter, and a preamplifier to drive the 50- Ω input of the on-chip power amplifier as shown in Fig. 10(a)–(c), respectively. The 5.2-GHz preamplifier uses one inductor to provide image rejection, while the 2.4-GHz one has no image rejection.

G. Power Amplifiers

The PA is the major power consumption unit in an RF transceiver. Therefore, it is highly desirable to develop novel PA circuits with adaptive biasing schemes for low power applications. To achieve higher power-added efficiency (PAE), a linear RF amplifier is usually biased for class-AB operation. In a conventionally biased class-AB PA, the average bias supply current increases as the RF input power increases. The increased average current results in an increased voltage drop in the resistive part of the biasing circuit. This in turn reduces the average voltage drop across the forward-biased PN junction of the amplifying transistors and pushes the amplifier into class-B and possibly even class-C operation. Therefore, the output power will be saturated and the output signal will be more nonlinear as the input power further increases. To improve linearity at higher input power levels where the amplifier is operated in saturation or close to saturation, the bias of the amplifying transistor needs to be adaptively adjusted. For 2.4- and 5.2-GHz applications, bias-boosting schemes are implemented that adaptively boost the PA bias currents for better linearity as the input power increases. With bias boosting, the PA quiescent current needs to be biased at a small current that can handle the minimum RF input power, leading to a lowered average power consumption.

On-chip power amplifiers for 2.4- and 5-GHz bands are integrated in the transceiver IC. The on-chip PA includes an adaptive biasing scheme in order to reduce the power consumption and increase the PAE [16]. Fig. 11 illustrates the PA configuration with adaptive biasing scheme. The biasing circuit consists of transistors Q_4 , Q_2 , and Q_3 and voltage adjusting resistors R_3 , R_4 , and R_5 . Resistors R_1 and R_2 , capacitor C_2 , and the emitter area of Q_4 determine the adaptive biasing level and the sensitivity to the input power variation. The PA output at the collector of Q_1 is connected to a supply voltage through pull-up inductor L_1 . An RF input is applied to the base of the transistor Q_1 through capacitor C_1 that can be part of the matching network between the PA and its predriver. The biasing circuit controls the quiescent current of the amplifier transistor Q_1 through transistor Q_2 and resistor R_1 . The input matching is independent of the adaptive biasing circuit as long as the impedances looking into R_1 is sufficiently high. The operation of the adaptive biasing scheme can be explained as follows. As the input RF power increases, the current flowing through transistor Q_4 becomes larger, which reduces the base voltage of transistor Q_3 . As a result, the current flowing through transistor Q_3 decreases, which increases the base voltage of transistor Q_2 . Thus, the current flowing through transistor Q_2 increases, leading to an increased biasing current for amplifier transistor Q_1 . Therefore, the adaptive biasing circuit automatically adjusts the PA bias current according to the varying input power. Thus, the linearity of the amplifier is improved for large input signals. The bandwidth of the bias-boosting loop is much smaller than the signal bandwidth. It senses only the average input power variation and uses it to adjust the bias current accordingly. As shown in Fig. 11, the adaptive bias loop is low-pass filtered to extract only the average RF power, which also ensures the stability of the PA. It normally takes thousands of input RF cycles to observe the bias boosting effect. However, since the input signal strength variation is a slowly varying process, the bias-boosting scheme provides an efficient means for low-power PA designs.

H. Synthesizer

For multistandard applications, it is often difficult to cover multiple frequency bands using an integer- N frequency synthesizer whose step size is limited by the reference frequency. In order to achieve the fine step size to cover the multiband channel frequencies, one has to lower the reference frequency in an integer- N synthesizer design, which results in high division ratio of the phase-locked loop (PLL) and leads to high in-band phase noise. In contrast, a fractional- N synthesizer allows the PLL to operate with a high reference frequency and meanwhile achieve a fine step size by constantly swapping the loop division ratio between integer numbers, thus the average division ratio is a fractional number. A fractional- N synthesizer achieves fine step size and low in-band phase noise with the penalty of fractional spurious tones, which come from the periodic division ratio variation. The basic architecture for the synthesizer is shown in Fig. 12. Included in the design are three LC-based VCOs to cover all frequency bands, and dividers and buffers to drive both the RF and IF mixers. To remove the fractional spurious components for a synthesizer with a fine step size, a $\Sigma\Delta$ noise shaper in the fractional accumulator is employed.

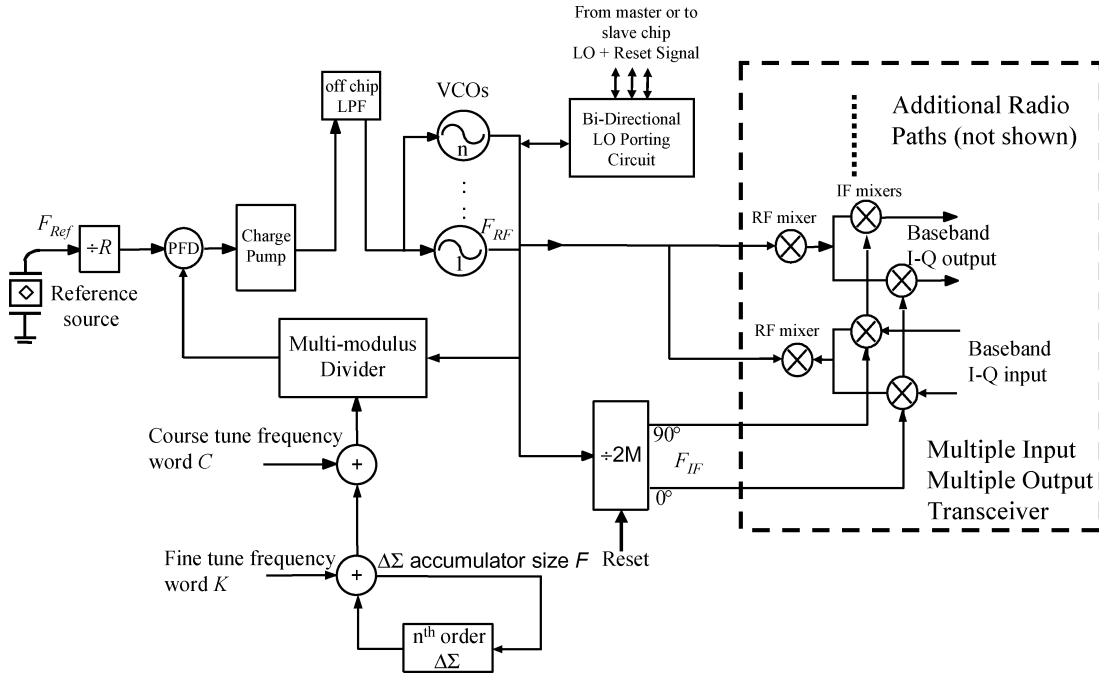


Fig. 12. Single $\Delta\Sigma$ fractional- N frequency synthesizer for a multiband MIMO walking-IF transceiver.

V. MEASURED RESULTS

The transceiver was fabricated in a 47-GHz SiGe BiCMOS process with 0.5- μm lithography. The back end of the process featured thick aluminum metallization designed to provide high-quality inductors. A die photograph of the chip is shown in Fig. 13. The entire MIMO transceiver chip is measured to be 5.4 mm \times 5.4 mm and the chip occupies a total silicon area of 29.1 mm². The 802.11a/b/g WLAN MIMO transceiver has been packaged in a 72-pin leadless plastic chip carrier (LPCC) package and mounted in a PCB for testing.

The total current consumption in the receive mode for one path was 195 mA for either the 2.4- or 5.2-GHz bands including the synthesizer power consumption. When two receiver paths in the dual-radio system were powered, the current went up to 320 mA. The current did not double because the two paths shared the synthesizer, which is one of the advantages of integrating multiradio MIMO system in one chip. Note that the receivers have higher than average linearity to deal with the situation of two in-band cordless phone interferers at a range of 1 m. This was an internal specification and resulted in slightly higher current consumption compared to some other receivers for WLAN. The receiver gain for the full path was 77 dB for the 2.4-GHz band and 72 dB for the 5.2-GHz band. The noise figure for the full receiver chain was 4.5 dB in the 2.5-GHz path and 7.4 dB in the 5.2-GHz path. The NF is slightly high in the 5-GHz band (although still acceptable) due to the connection of the LNA emitter inductor to ground. This ground is nonideal and it had inductance, which degrades the LNA gain and NF. This inductance is very hard to evaluate and predict as it depends on PCB vias and PCB ground routing, which were unknown before the chip was fabricated. It also reduces the common mode rejection of the circuit. This could be fixed in a revision of the design. The receiver path-to-path isolation was better than 40 dB in all cases. The receiver I/Q amplitude imbalance was 0.3 dB

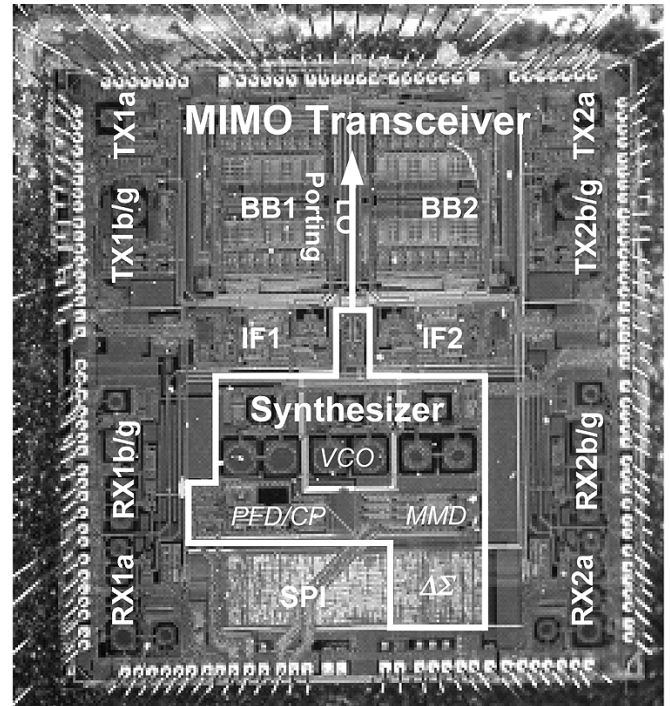


Fig. 13. Die photograph of the dual-radio MIMO WLAN transceiver.

and the quadrature error was 2.0°. A future revision of the chip would have included gain and phase calibration into the BB filters to achieve lower mismatch.

The tunable baseband filter was configured as a fifth-order elliptic ladder filter for a narrowband mode with 9.8-MHz corner frequency. The measured filter passband ripple below 6 MHz was 0.6 dBp-p and the group delay ripple below 6 MHz was 50 ns peak to peak, and it had an in-band gain of 25 dB in receive mode. The attenuation at 12 MHz was 15 dB, and attenuation

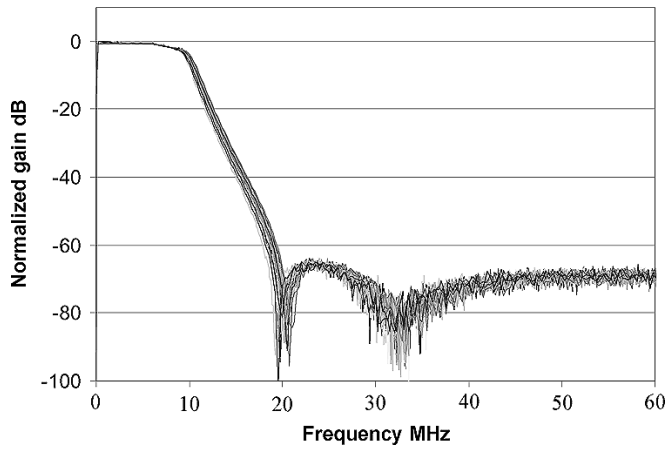


Fig. 14. Plot of the measured baseband filter response in narrowband mode for 32 devices. Note that the gain is normalized to 0 dB.

beyond 21 MHz was more than 60 dB. The noise of the filter was approximately $400 \text{ nV}/\sqrt{\text{Hz}}$ measured differentially at the receive filter output. The input and feedback resistors dominate the filter noise, with a lesser contribution from the input differential pair in the first gain stage of the BB filter. However, since there is significant gain in the RF/IF stages in front of the BB filter, the overall impact of the BB filter noise upon the overall noise figure is somewhat less than 1 dB. At full signal output amplitude, third-order mixing products were approximately 55 dBc down. A plot of the measured filter response normalized to 0 dB is given in Fig. 14 for 32 different chips.

The I–Q modulators achieved better than 40 dB of image rejection and 26 dB of carrier rejection. The TVGA has a gain range of 39 dB, a gain step of 3 dB, a gain variation smaller than 0.3 dB, and phase variation smaller than 25° . Each RF mixer has either an on-chip low-pass (2.4 GHz) or band-pass (5 GHz) filter associated, and the image rejection is better than 20 dB. The transmitter can deliver +10 dBm of linear power at 2.4 GHz with the on-chip PA, and +13.5 dBm of linear power at 5 GHz with an off-chip PA. The cross-coupling isolation between the two transmit paths is better than 40 dB. Since the PAs were single-ended, a substrate tap was added in the layout to improve the isolation between the paths. Fig. 15 gives the measured PA output power versus the input power for both 802.11a (PA A) and 802.11b (PA B) bands and for both linear PA (LIN) and bias-boosted PA (BB) designs. The 1-dB compression of PA A (LIN), PA A (BB), PA B (LIN), and PA B (BB) is 10.1, 9.8, 12.8, and 11.6 dBm, respectively. It is shown that the bias-boosting scheme does not degrade the PA linearity. In fact, the bias-boosted PAs provide comparable linearity to the linear PAs. The bias-boosted PAs achieve about the same gain as the conventional linear PAs. Fig. 16 shows the measured PAE versus the output power for both 802.11a and 802.11b bands and for all PA designs. It is evident that the bias-boosted PAs achieve better PAE for both the 2.4- and 5.2-GHz bands. The linear PAs are biased at a large current to handle the maximum input power, while the bias-boosted PAs are initially biased at a lower current and are adaptively tuned to larger currents only as input power increases. The PAEs for the two types of PAs are comparable only at larger inputs. When PA output power is smaller than

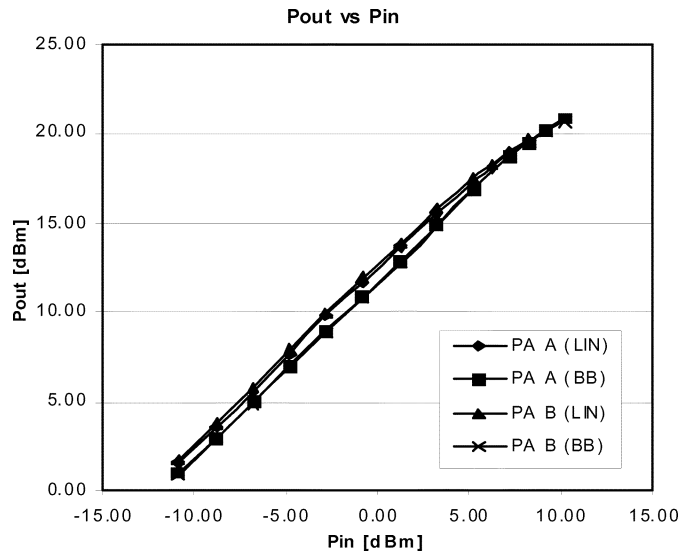


Fig. 15. Measured PA output power versus input power for both 802.11a and 11b bands and for both linear PA and bias-boosted PA designs.

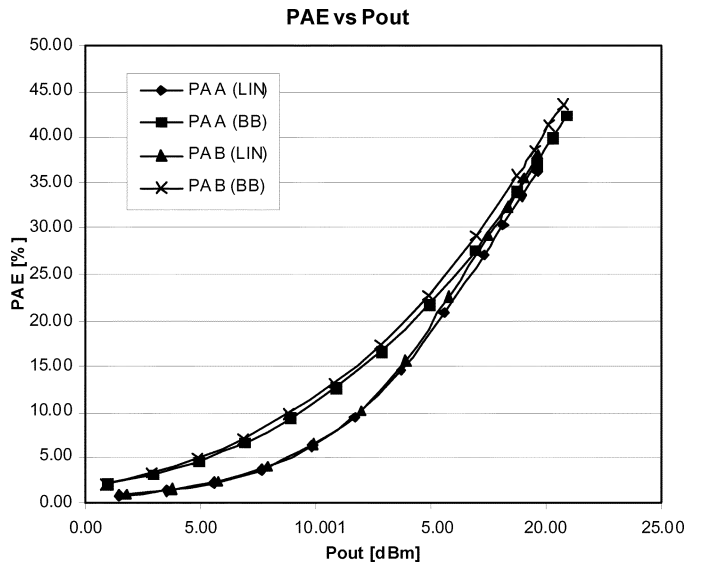


Fig. 16. Measured power amplifier PAE versus input power for both 802.11a and 11b bands and for both linear PA and bias-boosted PA designs.

about 17 dBm, the PAEs for the bias-boosted PAs are always better than those of linear PAs. The adaptive biasing scheme thus reduces the average power consumption and results in an enhanced PAE.

The total current consumption in transmit mode for one radio path is 240 mA for the 802.11b/g band and 255 mA for the 802.11a band. When two paths are powered, the current goes up to 400 mA in the 802.11b/g band and 430 mA in the 802.11a band. Fig. 17 shows a typical EVM measurement, which complies with the IEEE 802.11a WLAN standard requirements captured from the output of the 5-GHz predriver. Note that the PA caused negligible degradation in EVM. The frequency synthesizer itself consumed 36 mA of current and had an in-band phase noise of better than -98 dBc/Hz and a VCO phase noise of -120 dBc/Hz at 1-MHz offset. A phase-noise plot for the 802.11a lower 5-GHz band is shown in Fig. 18. The integrated jitter for the synthesizer was better than 0.43°_{rms}

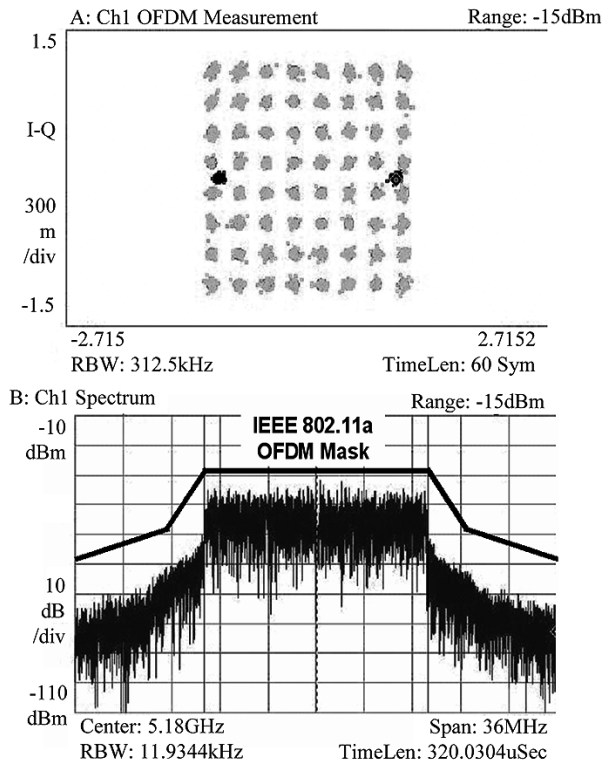


Fig. 17. EVM measurement for 802.11a channel 36. EVM = 4.3% meets the IEEE 802.11a OFDM requirement.

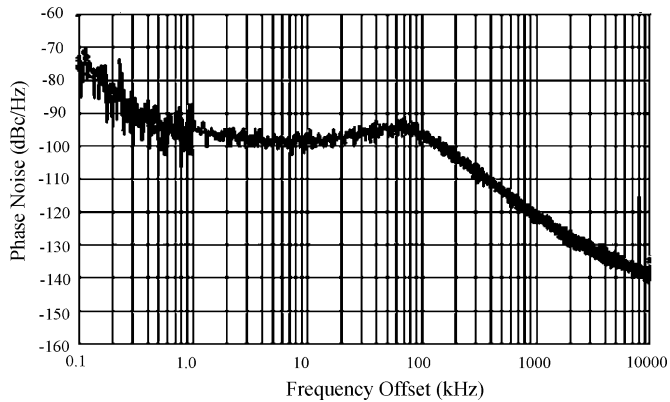


Fig. 18. Measured synthesizer phase-noise plot.

for the 802.11b/g band and better than 0.86° rms for the 802.11a band. The 802.11a channels have a fractionality of $1/5$. All of the 802.11a spurs were measured to be below -65 dBc. For the 802.11b/g channels, the worst fractional spurs occur with a fractionality of $1/30$. A novel scheme for spur reduction using second- or third-order $\Delta\Sigma$ modulators with precalculated accumulator seeds has been developed [7]. All of the 802.11b/g spurs were measured to be below -50 dBc. The I/Q quadrature error for both the transmitter and receiver was about 2° . This was achieved without the use of an IQ calibration loop since the down conversion to baseband is done from a 1-GHz IF. This is an advantage of walking IF over direct conversion.

TABLE I
SUMMARY OF TRANSCEIVER PERFORMANCE

Parameter	Performance	
	802.11b/g	802.11a
Band	802.11b/g	802.11a
Technology	0.5 μ m SiGe BiCMOS	
Voltage Supply	2.75V	2.75V
TX Chain Current Supply (1path/2paths)	240/ 400mA	255/ 430mA
RX Chain Current Supply (1path/2paths)	195/ 320mA	195/ 320mA
Synthesizer Current supply	36mA	36mA
TX output power	11dBm	13.5dBm
EVM at TX output power	4% (g only)	4%
TX Path to Path Isolation (measured at the PA outputs)	> 40dB	> 40dB
RX NF @ Max Gain	4.1dB	7.5dB
RX chain Max Gain	77 dB	72 dB
RX chain Min Gain	5.5dB	25dB
Rx IIP3 @ Min Gain	+8.8 dBm	-12.8 dBm
RX I/Q Amplitude Imbalance	0.3 dB	0.3 dB
RX I/Q Quadrature Error	2.0°	2.0°
Rx Path to Path Isolation (measured at the BB filter output)	>50dB	> 40dB
Max DC offset without correction (measured at the output of the BB filter)	90mV	90mV
Synthesizer Integrated Noise 100Hz to 10MHz	0.35~0.43 $^\circ$ rms	0.63~0.86 $^\circ$ rms
VCO Phase Noise	-120dBc/Hz @ 1MHz	-120dBc/Hz @ 1MHz
In Band Phase Noise	-98dBc/Hz @ 10kHz	-98dBc/Hz @ 10kHz
Synthesizer Reference Frequency	40MHz	
Synthesizer Step Size	468.75kHz	781.25kHz
Synthesizer Spurious	<-50 dBc	

Table I summarizes key performance parameters for the transceiver. The measurements presented can be considered 3σ as more than 30 parts were measured over temperature.

In order to demonstrate the MIMO radio link using the developed dual-radio RF transceiver ICs, a prototype link was tested to determine the improved range of a MIMO WLAN in the company's office building at 2.4 GHz. Fig. 19 shows the range improvements that were achieved by using different link configurations as measured from a central access point (AP). The range illustrated is for a data rate of 54 Mb/s comparing the range achieved for a 10% PER for a SISO radio, a radio with two-antenna diversity, 4CBF transmitter, and two-antenna switched diversity in the receiver, and finally 4CBF in the transmitter and 2CBF in the receiver. Note that a 4×4 link is not shown in the figure, as the office was not big enough to test the range limits using this type of link. As shown, the WLAN transmission range has been greatly improved using 4×2 CBF configuration, where four radio paths (two dual-radio RFICs) are used in the access point (AP) and two radio paths

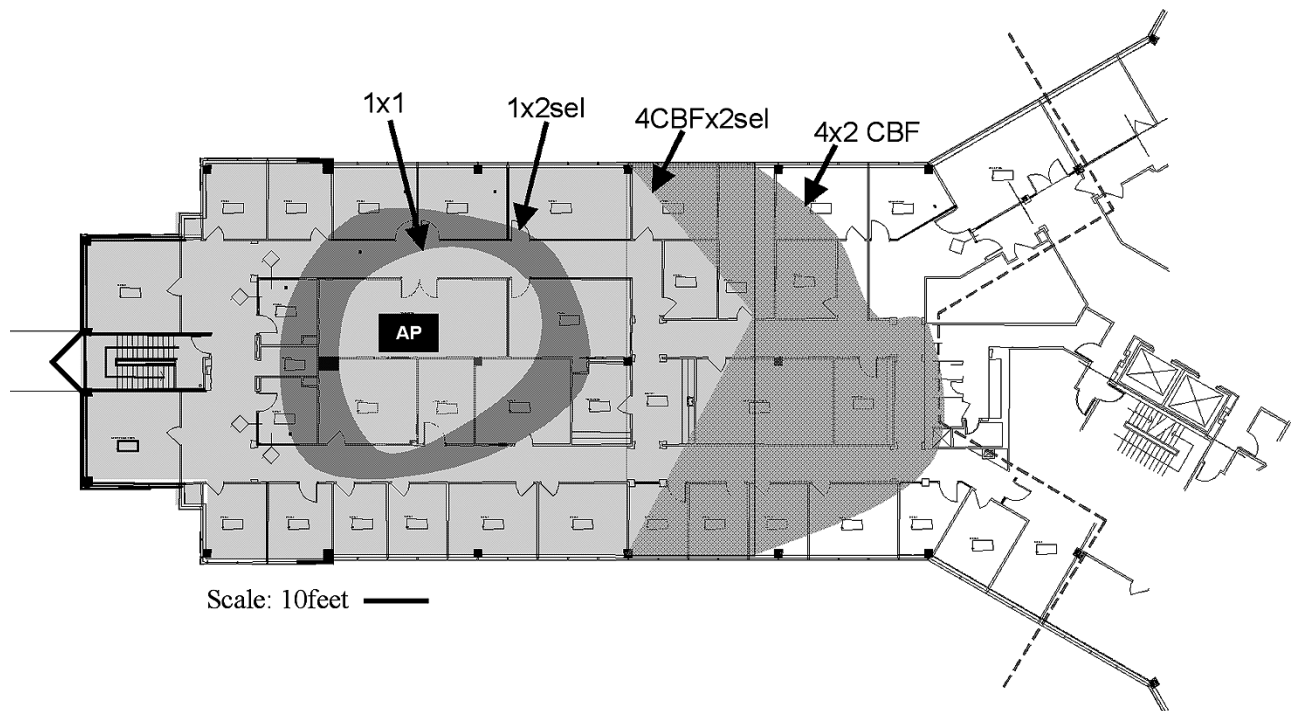


Fig. 19. Demonstration of improved WLAN range using the developed MIMO transceiver RFICs operating at 2.4 GHz.

(one dual-radio RFIC) are used at the user end. The total transmit power for any MIMO configurations under the test were within the IEEE 802 WLAN standard. The “2sel” refers to two-antenna selection diversity. This configuration uses two antennas and the receiver selectively picks the one with the strongest signal. Thus, a $4\text{CBF} \times 2\text{sel}$ is actually a 4×1 CBF configuration with the receiver antenna corresponding to the strongest signal out of a two-antenna selection diversity. Similarly, a $1 \times 2\text{sel}$ is a 1×1 configuration with the receiver antenna corresponding to the strongest signal out of a two-antenna selection diversity. For a 1×1 conventional SISO configuration, the WLAN range is limited within a few offices.

VI. CONCLUSION

This paper has presented the implementation of an IEEE 802.11a/b/g compliant transceiver RFIC in a 47-GHz SiGe BiCMOS process for 2.4- and 5.2-GHz multiband MIMO WLAN applications. To the best of the authors’ knowledge, the transceiver RFIC presented in this paper is the first published design for multiband MIMO WLAN applications. The transceiver RFIC includes two complete radio paths fully integrated on the same chip. Using a walking IF architecture, the dual-radio transceiver employs a single $\Sigma\Delta$ fractional- N synthesizer for RF and IF LO generations that cover the entire IEEE 802.11a/b/g WLAN bands. Using a total of two dual-radio RFICs, a 4×4 MIMO radio link has been implemented and tested under a typical indoor WLAN environment. The 4×4 MIMO radio achieves 15 dB of link margin improvement over a conventional SISO radio.

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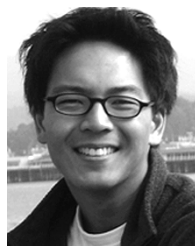
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