A Multiband $\Delta\Sigma$ Fractional-N Frequency Synthesizer for a MIMO WLAN Transceiver RFIC

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***Abstract*—This work presents a shared fractional-N synthesizer used by two dual-band 802.11 radios integrated on a single chip for 2×2 multiple-input multiple-output (MIMO) applications. Additional 2×2 MIMO chips can be used in a system by phase synchronizing the signal paths through a bidirectional LO porting scheme developed for this application. This synthesizer was fully integrated with the exception of an off-chip loop filter. The synthesizer is a $\Delta\Sigma$-based fractional-N frequency synthesizer with three on-chip LC tuned VCOs to cover the entire frequency bands specified in the IEEE 802.11a/b/g and Japanese WLAN standards. The radio uses a variable IF frequency so that both the RF LO and IF LO can be derived from a single synthesizer saving chip area and power. The synthesizer includes a programmable second/third-order $\Delta\Sigma$ noise shaper, a phase frequency detector, a differential charge pump, and a 6-bit multimodulus divider (MMD). The nominal jitter from 100 Hz to 10 MHz is 0.63–0.86° rms in the 5-GHz band and 0.35–0.43° rms in the 2.4-GHz band. The maximum frequency deviation of the synthesizer when enabling the transmitter is less than 150 kHz and the frequency error settles to 2 kHz in less than 12 μs. For MIMO applications requiring more than two full paths, a single synthesizer on one die can be used to generate the LOs for all other radios integrated in different dies.**

***Index Terms*—Fractional-N synthesizer, MIMO, RFIC, SiGe, sigma-delta modulator, voltage-controlled oscillators, wireless communications, WLAN, 802.11.**

I. Introduction

WIRELESS communications remain an important area of research and development, fueled by the emerging of wireless local area networks (WLAN) and the third generation W-CDMA technology [1]–[8]. The ever-increasing demand for wireless multimedia applications such as video streaming keeps pushing future WLAN systems to support much higher data rates (100 Mb/s up to 1 Gb/s) at high link reliability and over greater distances. Furthermore, the speed gap between "wired" and "wireless" LANs should be decreased so that WLAN can be seamlessly merged into high-data rate wired networks. A MIMO system in combination with space-time signal processing allows increased data rate and/or improved transmission range and link reliability without additional costs in bandwidth or power. MIMO systems using multiple antennas allow enhancements to the existing IEEE 802.11 technology. Discussion is also underway to include MIMO functionality in a future 802.11n WLAN standard. However, transceiver RFIC designs for MIMO systems are not trivial and many issues associated with MIMO such as synchronization of local oscillators (LOs) and relative phase drift between signal paths for different radios need to be carefully addressed.

With WLAN standards operating in very different frequency bands, market leading WLAN solutions have to offer multimode interoperability with transparent worldwide usage. Moreover, the frequency allocation of the WLAN standards in the "unlicensed" 5-GHz band is constantly evolving. In particular, the Japanese government recently proposed four additional RF channels in the 4.9–5.0-GHz band and further three channels in the 5.03–5.09-GHz band for this standard. This change could significantly increase the available channels for 5-GHz WLAN in Japan, and create yet another difficulty for WLAN chipmakers by requiring them to enable access to this lower frequency band. It is thus desirable to design a WLAN transceiver with a future-proofed multiband frequency synthesis scheme against evolutions and changes in allocated spectrum worldwide.

This paper presents a synthesizer designed for MIMO WLAN applications. It uses a $\Delta\Sigma$ fractional-N architecture to allow a high reference frequency, fine step size, and low divide ratio to achieve low in-band phase noise. The $\Delta\Sigma$ modulator can be programmed with different orders and can be loaded with precalculated seeds for spur reduction. Two PMOS-based *LC*-tuned VCOs with automatic amplitude control are designed to cover the frequency bands specified in IEEE 802.11a/b/g standards. The use of a resetable divide by four block in the synthesizer enables the use of a walking IF radio architecture and alleviates the need for an IF synthesizer in the radio. The synthesizer achieves an integrated phase noise of 0.4° rms for the 2.4-GHz band and 0.7° rms for the 5-GHz band, respectively, which is among the best results reported.

II. Synthesizer Architecture for MIMO Radio

For multistandard applications, it is often difficult to cover multiple frequency bands using an integer-N frequency synthesizer whose step size is limited by the reference frequency. In order to achieve fine step size to cover the multiband channel frequencies, one has to lower the reference frequency in an integer-N synthesizer design, which results in high division ratio of the phase-locked loop (PLL) and leads to high in-band phase

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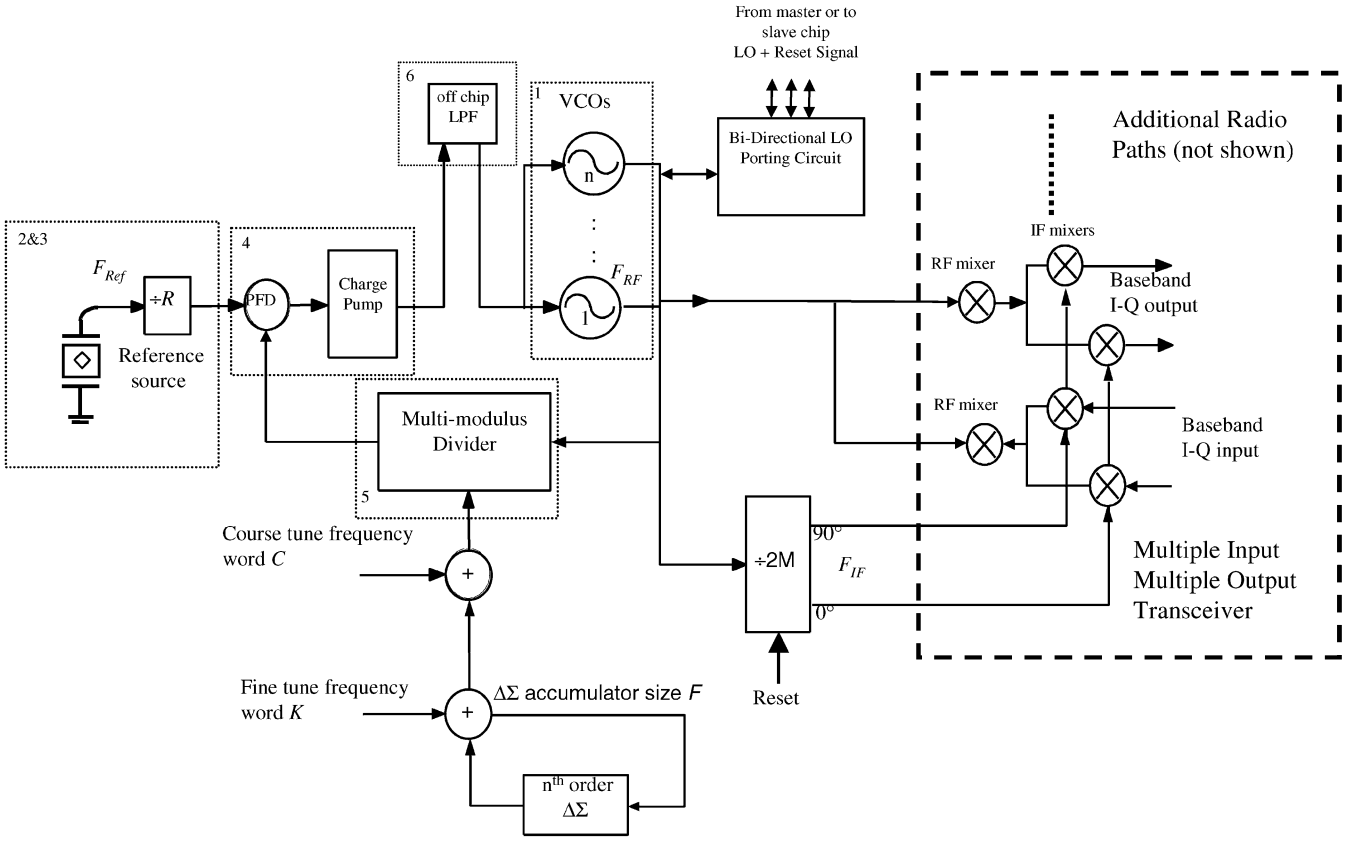

Fig. 1. Single $\Delta\Sigma$ fractional-N frequency synthesizer for a multiband MIMO walking IF transceiver.

noise. In contrast, a fractional-N synthesizer allows the PLL to operate with a high reference frequency and meanwhile achieve a fine step size by constantly swapping the loop division ratio between integer numbers, thus the average division ratio is a fractional number. A fractional-N synthesizer achieves fine step size and low in-band phase noise with the penalty of fractional spurious tones, which come from the periodic division ratio variation. Note that spacing of the closest spur to the carrier is determined by the synthesizer step size. For a synthesizer with a step size smaller than the loop's low-pass filter (LPF) bandwidth, it is practically impossible to remove the fractional spurs by using this filter. Reducing the loop bandwidth to combat the fractional spurs results in long lock times and increased VCO noise contributed to out-of-band phase noise. To remove the fractional spurious components for a synthesizer with fine step size, the best solution is to employ a $\Delta\Sigma$ noise shaper in the fractional accumulator [9]–[12]. However, different WLAN standards require a different order of the $\Delta\Sigma$ noise shaper and different size of the fractional accumulator. A programmable $\Delta\Sigma$ fractional-N architecture is therefore selected for this multiband synthesizer design.

Since this market is very cost-sensitive, if a radio is to be competitive it must be low cost and low power. Since the synthesizer can be a large part of both the die area and power budget, it is desirable to keep its contribution to a minimum. Choosing the transceiver architecture wisely can do this. Superheterodyne radios require two synthesizers, but have a high level of performance. Their inherent frequency diversity reduces dc offset and VCO pulling effects as compared to direct conversion receivers. Although by comparison direct conversion receivers require only one local oscillator, often mixing schemes are used to achieve similar frequency diversity, resulting in a more complicated synthesizer. A compromise between the two approaches is to use a walking IF architecture where the RF LO is $2M$ times the IF LO (in this case $M = 2$) [13]. Thus, both LOs can be derived from a single synthesizer, deriving much of the benefit of a direct downconversion radio, but retaining the performance advantages of the superheterodyne radio. The basic chip architecture for the synthesizer is shown in Fig. 1.

In this system, two transceiver paths are integrated on a single chip. Only two radios were integrated because more would have led to more expensive packaging and lower yield, and for many applications a 2×2 MIMO system with two radios is sufficient. However, if more than two radios are desired in a particular application, then even two, three, or more transceiver chips can be used in a single link, provided that their LOs are all phase synchronized. If multiple chips with separate synthesizers are used, then the phase drift of each of the PLLs relative to each other can be problematic. MIMO calibration requires loop back measurement through transmit and receive paths in order to calculate calibration coefficients for composite beam forming (CBF) operation. It is desirable to minimize the frequency of calibration. If the LO phases of the MIMO radios shift relative to each other excessively, the previously performed MIMO phase calibration will be invalidated. Due to static phase error variations between the PLLs in different chips, the relative phase between the two MIMO paths will drift with the variation in the static phase errors of the two PLLs. This static phase error variation

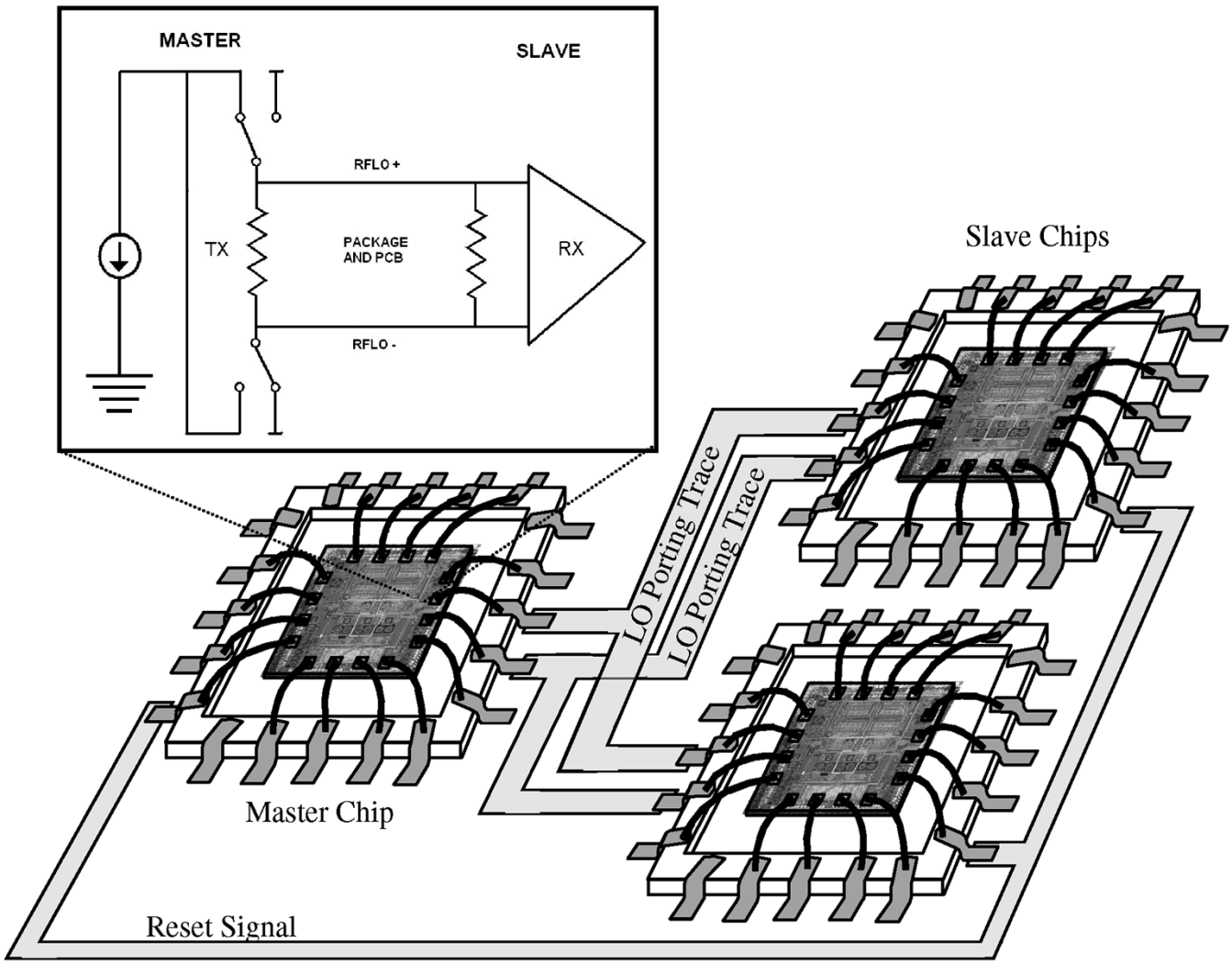

Fig. 2. Diagram showing the operation of LO porting for MIMO applications.

may result from propagation delay and/or leakage current variation due to temperature gradients. In addition, the two distinct PLLs could have different low-frequency offset noise characteristics, resulting in different low-frequency wander. To avoid many of these LO phase drift issues resulting from the use of multiple PLLs locked to a common reference, an optional LO porting block was added to the architecture, allowing for sharing of a common system RFLO among multiple chips as shown in Fig. 1. Although there is some fixed delay due to the LO distribution, many of the drift mechanisms are eliminated. In LO porting mode, the differential LOs from one master chip are ported to all the slave chips and are used to drive all their clock trees and dividers of all chips.

In addition, when two RFICs are used for 4×4 CBF operation, the IF LO divide by 4 circuits can have a 90° phase ambiguity if the two chips are not synchronized in a repeatable manner after lock. Due to variations in VCO frequencies and therefore the number of clock cycles during channel switching and prior to lock, the phase difference between the two IF LOs can assume any integer multiple of 90° until synchronization after lock. The divide by 4 circuits used in our designs are synchronized by using a one-shot circuit enabled through the serial port interface (SPI) and synchronized across the MIMO radio chips.

A bi-directional driver was designed to port the RFLO signals between two or more chips. A differential constant current mode design was adopted for improved electromagnetic and common-mode rejection properties (see Fig. 2). Two pins are used for differential RF LO signals and two pins are differential pulse signals for the IF LO divider reset. The driver is bi-directional, so the transmit driver and a line receiver are tied to the same nodes on each chip. For the master chip, the transmitter is enabled, and for the slave chip, the receiver is enabled. Or alternatively, the LO porting can be disabled for 2 CBF (single chip) operation or independent synthesizer (multichip) operation.

III. Frequency Plan for Multiband WLAN Applications

A fractional-N synthesizer gains advantages of low phase noise and fine resolution. The synthesized RF frequency and the IF frequency can be represented as

$$\begin{cases} F_{\mathrm{RF}} = F_{\mathrm{REF}}\left(C + \dfrac{K}{F}\right) \\ F_{\mathrm{IF}} = F_{\mathrm{RF}}/2M \end{cases} \tag{1}$$

where C is coarse tune frequency word (i.e., the integer part of the division ratio), and K is the input of the fractional accumulator with size of F. Note that the fractional-N synthesizer step size is equal to F_{REF}/F. M is chosen to be 2 for this WLAN system, namely, the RF frequency is four times the IF frequency.

This multiband frequency plan is based upon the assumption that the system can tolerate a walking IF. Thus, the IF filter needs to have a wider bandwidth, namely, from 804 to 1161 MHz for the presented synthesizer. The drawback of the walking-IF scheme lies upon the widened IF filter bandwidth which degrades the system signal-to-noise ratio (SNR) performance. According to the frequency plan, the maximum accumulator size is 30 (for 802.11b/g applications). Although the 5-bit accumulators can cover the current WLAN applications, a 6-bit second/third-order $\Delta\Sigma$ was designed to prepare for future WLAN standard evolutions. The 6-bit multimodulus divider (MMD) is programmed from 64 to 127. Therefore, the total division ratio of the fractional-N is

$$N = \left(C + 64 + \frac{K}{F+1} \right). \tag{2}$$

Thus, using a 40-MHz reference frequency, a 6-bit accumulator $(F + 1 = 64)$ and a 6-bit MMD, a RFLO step size of 625 kHz was achieved. Since for the 802.11b/g bands the channel frequency is equal to RFLO-RFLO/4, the effective minimum step is $625 \text{ kHz} * 0.75 = 468.75$ kHz. Conversely for the 802.11a low/mid bands the channel frequency is equal to RFLO + RFLO/4 and the effective minimum step is $625 \text{ kHz} * 1.25 = 781.25$ kHz.

The presented frequency plan also carefully explored any possibility of sharing VCOs for different bands. Only three narrow-band VCOs are needed to cover the 802.11a/b/g and Japan 2.4-GHz/5-GHz WLAN frequency bands. A narrow tuning range will greatly benefit the loop design since the VCO gain and charge pump transfer function are more linear within a narrow range. Any nonlinearity here can lead to undesired spurious tones as shown in [14] and should be minimized. As will be discussed in later sections, the source and sink transistors in the charge pump will be pushed into saturation at the edge of the VCO tuning voltages. Nonlinearity in the phase to current conversion and variation in the skew curve with time will cause LO phase drift at the synthesizer output, which may be acceptable in a synthesizer design for single-input single-output (SISO) applications, but it is not tolerable in a MIMO system where the LO signals in multiple transceivers need to maintain synchronization.

A low-cost crystal oscillator was used to generate the reference frequency at 40 MHz. To choose a proper reference frequency, the following issues were considered.

1) F_{ref} should be as high as possible to reduce the total division ratio and thus reduce the in-band noise.
2) F_{ref} cannot be too large due to the step size restriction.
3) To achieve a fine step size with large F_{ref}, a large accumulator is needed, which requires a high-order $\Delta\Sigma$ noise shaper for fractional spur rejection. Our design goal was to achieve -95 dBc/Hz in-band phase noise floor with no more than a third-order $\Delta\Sigma$ noise shaper.
4) F_{ref} should be smaller than about 50 MHz such that a low-cost crystal oscillator can be used.

With careful design, a minimum accumulator size of 5 for 802.11a bands and 30 for 802.11b/g bands was achieved. Our synthesizer assures low phase noise and low spurs for all available WLAN applications. To prepare for future frequency bands, the $\Delta\Sigma$ fractional-N accumulator was designed with 6 bits, which can handle a fractional denominator up to 64. With the flexibility of using various reference frequencies, the presented architecture thus provides a multiband frequency synthesizer that is future-proofed against evolutions and changes in allocated spectrum worldwide.

IV. Programmable $\Delta\Sigma$ Modulator With Precalculated Seeds

The synthesizer includes $\Delta\Sigma$ accumulators to shift the spurious components associated with fractional-N synthesis to a higher frequency band, where randomized spurs can be filtered by the loop filter, as shown in Fig. 1. The presented $\Delta\Sigma$ accumulator is a multiloop MASH structure as illustrated in Fig. 3. The MASH $\Delta\Sigma$ gains the advantage of superior close-in noise shaping capability [9], [10], [12]. It is unconditionally stable and can be easily implemented for high-speed applications. As shown in Fig. 3, the $\Delta\Sigma$ modulator consists of three cascaded accumulators with a single-bit carry from each accumulator. The carries from three accumulators are delayed properly and are then used to select coefficient banks derived from the MASH transfer function $(1 - z^{-1})^n$. Using pre-calculated coefficients speeds up the MASH calculation by eliminating a few adders. Moreover, every accumulator output is buffered, allowing pipelined operation. Thus, the speed constraint is reduced to only one accumulator calculation per $\Delta\Sigma$ clock cycle. The first accumulator in the MASH architecture provides fractional programmability with programmable accumulator size of F and accumulator input K. The three accumulators can be selected and powered down separately to allow programmable $\Delta\Sigma$ architectures in the following format:

1) an integer-N synthesizer, when only the coarse tune is selected and all three accumulators are powered down;
2) a fractional-N synthesizer without noise shaping, when coarse tune and the first accumulator is selected and the second and third accumulators are powered down;
3) a fractional-N synthesizer with second-order $\Delta\Sigma$ noise shaping, when coarse tune, the first and second accumulators are selected and the third accumulator is powered down;
4) a fractional-N synthesizer with third-order $\Delta\Sigma$ noise shaping, when coarse tune and all three accumulators are selected.

The programmable $\Delta\Sigma$ synthesizer architecture is desired for multiband applications, where different fractionality and noise shaping effects are required. A lower order of $\Delta\Sigma$ should be chosen as long as it has enough spur rejection. For a multistage MASH structure, a higher order $\Sigma\Delta$ modulator corresponds to more output bits, which dither the loop divisor ratio in a wider range around its desired value (the average value of the instantaneous divisor values). The charge pump would be

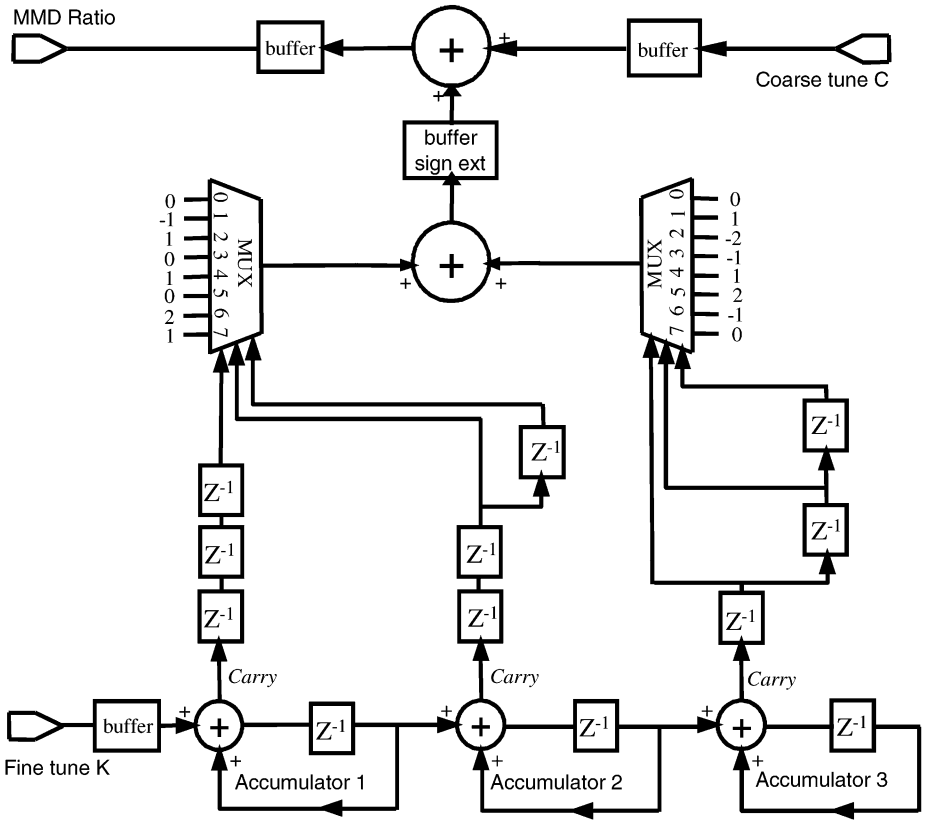

Fig. 3. Second-order and third-order multiloop MASH delta-sigma fractional accumulators.

turned off only when the divisor value is equal to the desired value. Dithering the divisor value in a wider range will upset the charge pump with larger source or sink currents, which needs a longer time to be corrected by the loop. Thus, a higher order $\Sigma\Delta$ increases the modulated turn on time of the charge pump in the locked condition, which makes the synthesizer more sensitive to substrate noise coupling and reference spur feedthrough [12].

The presented $\Delta\Sigma$ accumulator has a special feature of loading pre-calculated start values to three accumulators to avoid artificial spurs at the synthesizer output. It is known that any repetition of time sequence will cause artificial spurs in the spectrum with a frequency inversely proportional to the repetition's period. Loading different start values (seeds) to different accumulators can break the repetition in the time domain. Thus, artificial spurs can be reduced using a proper start value for each accumulator. In addition, a different order of $\Delta\Sigma$ noise shaper can be selected simultaneously. Resetting the first accumulator with a loaded seed is more important than for the second and the third accumulators, since only the first accumulator has a constant input, which may result in a repeated accumulator value, i.e., artificial spurs. The second and the third accumulators take the outputs from previous accumulators as their inputs, which are more like random numbers. Thus, the values in the second and the third accumulators are not likely to be repeated. All required WLAN channels have been carefully simulated and the desired order as well as seed values for the $\Delta\Sigma$ modulators has been determined for each channel to meet the spur requirement of less than -50 dBc. The proposed spur reduction scheme with pre-calculated accumulator seed values can be simply implemented with the existing accumulator reset and hence does not require additional hardware, while other spur randomization schemes such as dithering the LSB of the $\Delta\Sigma$ input not only require additional hardware, but also cause large frequency variation for small input words.

The $\Delta\Sigma$ fractional-N block is designed in 0.5-μm CMOS technology using a Verilog driven digital design flow. Fig. 4 gives Verilog simulation results of the MMD ratio and its spectrum for the worst spur case with $N = 81{+}63/64$, where coarse tune $C = 81 - 64 = 17$ (MMD ratio $= 64 + C$), fractionality $F = 64$, and fine tune $K = 63$. All three-accumulator outputs are selected and the fractional spurs are thus shaped by a third-order MASH $\Delta\Sigma$ fractional accumulator. Fig. 4 shows how the third-order $\Delta\Sigma$ dithers the division ratio around its average value ($17 + 63/64$, as shown by the straight line in the upper plot) in time domain. As a result, it clearly demonstrates the third-order noise shaping effect of 60 dB/dec (bottom plot) in frequency domain.

V. Programmable Multimodulus Divider Phase Frequency Detector and Charge Pump

A 6-bit programmable MMD is designed based on the topology of cascaded $2/3$ dual-modulus prescalers as shown in Fig. 5. The divide by $2/3$ cells can be implemented in various topologies such as those described in [15]. An SR latch-based digital tri-state type phase frequency detector (PFD) is chosen to provide phase and frequency comparison between the reference frequency and VCO divided frequency as illustrated in

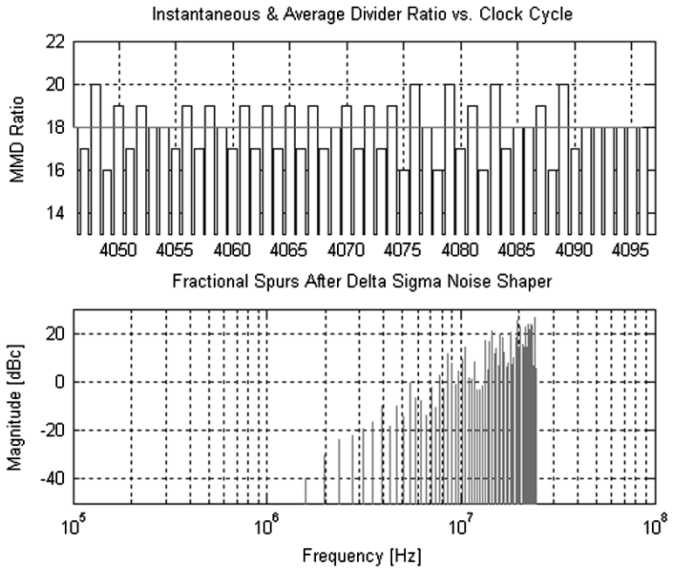

Fig. 4. Simulated division ratio and its spectrum shaped by a third-order MASH $\Delta\Sigma$ fractional accumulator for the worst spur case with $F = 64$.

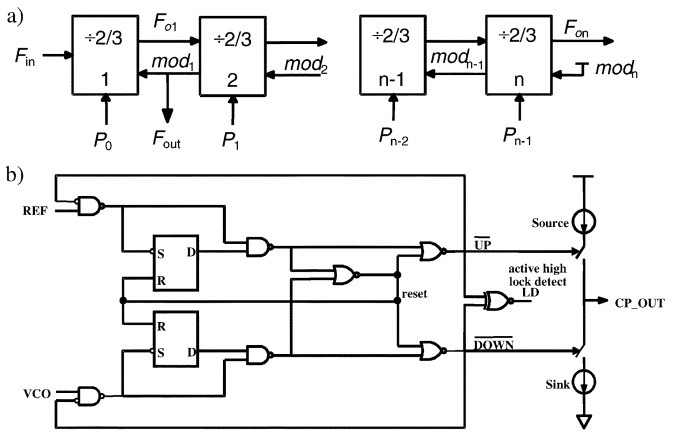

Fig. 5. (a) MMD using cascaded divide by $2/3$ cells and (b) PFD and CP.

Fig. 5. It contains an exclusive-OR gate that can be used as a lock indicator. This PFD has only one zero-crossing over its phase detection range, which ensures that the device does not lock to the second and third harmonics.

The charge pump following the PFD is differential with single-ended output as shown in Fig. 6. The PFD input phase error is represented by the PFD UP and DOWN output pulses, which control the CP source and sink current sources, resulting in current flow in or out of the charge pump.

The source/sink current $I_{\rm CP}$ can be programmed for eight different settings from 125 to 1875 μA. These currents can be used to adjust the loop gain and therefore to compensate for VCO gain variations. A 3-bit select signal controls the current mirrors whose transistor's size is binary weighted. Thus, $I_{\rm CP}$ can be adjusted in eight steps.

Nonlinearity associated with the phase detector and charge pump has a great impact on the synthesizer performance. Nonlinearity is even a bigger concern when the spur compensation is done in the analog domain where a correction signal is produced by a DAC and the CP needs to linearly transfer the spur content to analog signal for cancellation [20]. LO phase accuracy

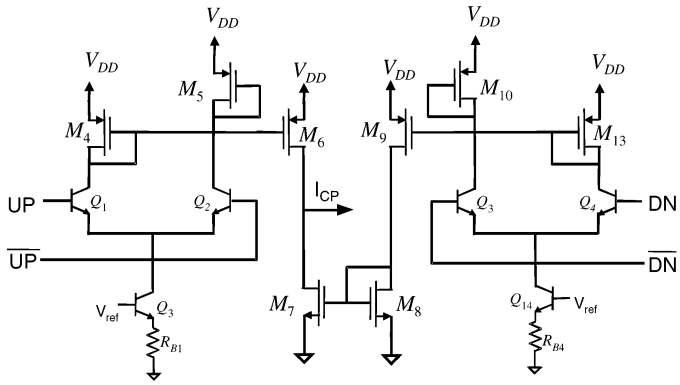

Fig. 6. Differential charge pump circuitry with CMOS current mirrors.

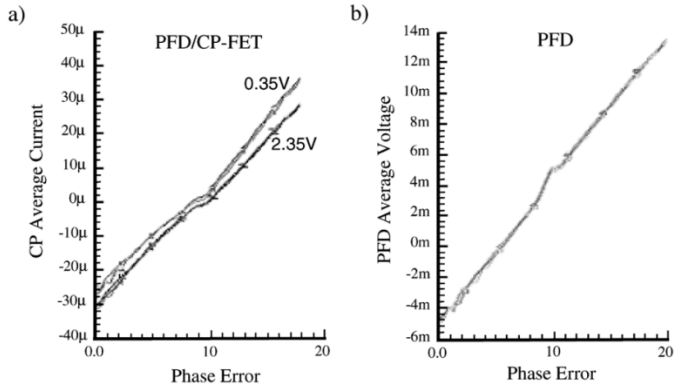

Fig. 7. Transfer functions of (a) PFD/CP-FET and (b) PFD at different temperatures (20°C, 30°C, 40°C) and VCO tuning voltages (0.35 V, 2.35 V). Charge pump current setting $I_{\rm CP} = 1.875$ mA.

is desired in MIMO applications where multiple synthesizers are used and their output phases need to be synchronized. There are many sources that can cause slow LO phase drift including PFD/CP, deadzone, and unbalanced propagation delay variation in separate synthesizer paths. Deadzone occurs when the PFD and CP gain drops to zero and thus the loop loses the sensitivity for any phase difference smaller than this range. PFD/CP gain deviates from the ideal linear curve is not necessarily a deadzone problem as long as the slope of the gain curve is not zero and the loop can still respond to the input phase difference. For a tri-state PFD, its output at lock contains narrow pulses and it is very difficult for a CP with a capacitive load to linearly convert those narrow pulses into corresponding currents. To minimize the deadzone problem, various anti-backlash circuitries can be added to the PFD and transistors in PFD and CP should also be optimized and balanced. As discussed earlier, the optional LO porting block eliminates many of these LO drift issues associated with separate PLLs locked to a common reference.

Fig. 7 compares the transfer functions of the PFD and PFD/CP designed with FETs at different temperatures and VCO tuning voltages. In the simulation, the input contains only one pulse with a width of 10 ns (50 MHz) and the output is averaged over one reference period (20 ns) right after the propagation delay. It can be seen that the PFD itself contributes very little nonlinearity under temperature variations. The CP dominates the nonlinearity. At the center of VCO tuning voltage ($\sim$1.35 V) and around room temperature (20°C–40°C), the

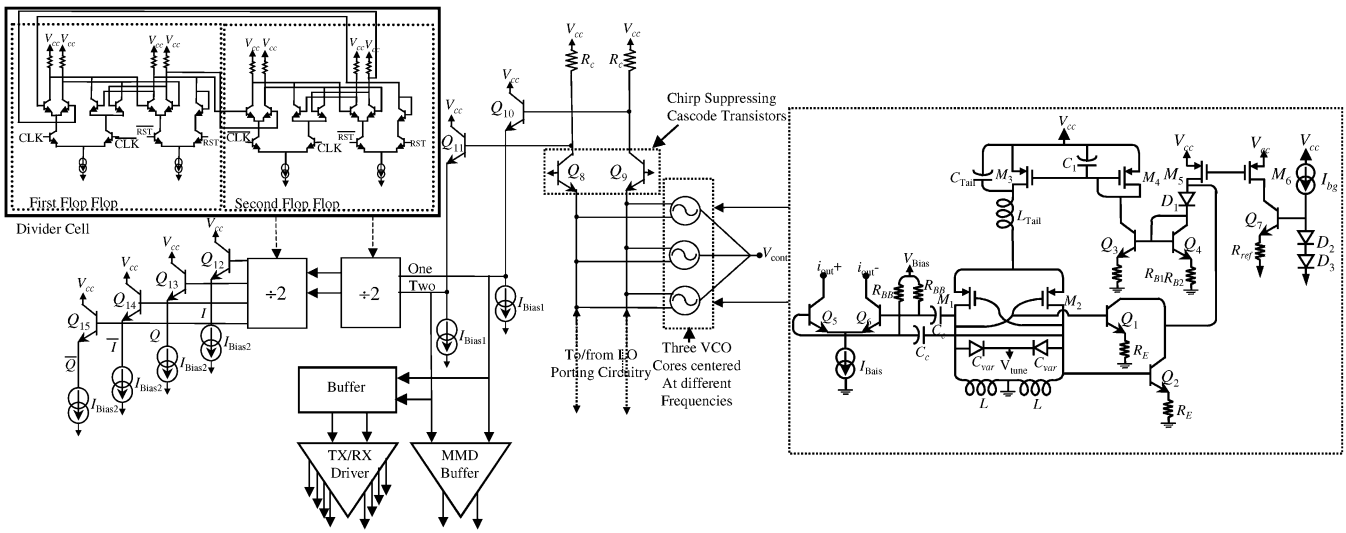

Fig. 8. System-level circuit diagram for the VCOs and clock tree.

temperature coefficient is about 0.037°/°C. Note that the flat part around the lock point corresponds to the deadzone of the PFD and CP transfer curve, where the loop loses the gain to correct any phase error smaller than the deadzone. As a result, the synthesizer output signal may jitter within the deadzone, causing phase error and phase noise. The speed limit of the CP transistors for responding to the narrow pulses at the PFD outputs and the imbalance between the charge pump source and sink mirrors are the major source of the CP deadzone. It is for this reason that the npn transistors at the CP input differential pairs were used although the FETs are used in CP mirrors. In addition to the deadzone problem, the leakage of the loop filter capacitor increases the CP average turn-on time in the lock condition, which degrades the spurs and phase noise due to increased substrate noise coupling. The nonlinearity of the PFD/CP is caused by the inability of the PFD/CP to respond to extremely narrow pulses due to bandwidth limitations. To improve the PFD/CP linearity, a delay unit can be inserted in the PFD reset path to increase the pulse width at the PFD outputs in the lock state. Thus, the switching of the CP transistors doesn't need to operate at high speed. Introducing a small amount of leakage current at the CP output can also widen the narrow PFD pulses. Both schemes increase the charge pump turn-on time in the lock state and thus degrade the loop noise and spur performance. Moreover, the delay unit degrades the frequency performance of the PFD as well.

VI. Multiband VCO Designs

The core of the oscillator is formed using two PMOS transistors M_1 and M_2 connected in a negative resistance configuration and attached to the *LC* tank of the VCO as shown in Fig. 8 [14]. The tank itself consists of two inductors L and a pair of pn junction varactors $C_{\rm var}$. PN junction varactors are preferred in this technology because of their high Q at the frequencies of interest. However, they have one critical drawback. They have a parasitic substrate diode associated with the n side of the junction that has a low Q and parasitic capacitance. Unless the n side of the diode is connected to ac ground, then the structure will include this lossy substrate diode impacting VCO performance [16], [17]. Specifically these diodes will cause a reduction in tank Q, and it was also observed that their presence can lead to significant power supply noise rejection issues. This is the reason that the PMOS VCO core of Fig. 8 is preferred. In this case, the tank can be connected to ground rather than $V_{\rm CC}$ so that the diodes can be connected in the proper polarity. PMOS also offers the advantage of higher output swing than bipolar provided high phase noise at offset frequencies below 100 kHz (due to high flicker noise) can be tolerated. This is due to the fact that the PMOS transistors can be operated into the triode region without affecting the VCO noise performance.

The tank inductors are made as large as possible to maximize the tank equivalent parallel resistance while still allowing the varactors to be large enough so that parasitic capacitance does not reduce the available frequency tuning range to an unacceptable level. The PMOS transistors themselves are sized so that they have a large dc $V_{\rm GS}$ voltage leaving enough headroom to accommodate the current source M_3. The inductor $L_{\rm Tail}$ and the capacitor $C_{\rm Tail}$ form a filter that is designed to filter out noise from the bias circuitry so that it does not affect the phase noise of the VCO [18].

The current through the VCO must be set large enough to maximize the voltage swing at the tank to minimize the phase noise of the circuit. The swing will be maximized when the transistors are made to alternate between saturation and cut-off at the top and bottom of the VCO voltage swing. Once the transistors reach this voltage swing level, raising the current will not cause the swing to grow any more, will increase the phase noise, and will waste current.

The automatic amplitude control (AAC) loop used in this design is also shown in Fig. 8. Here transistors Q_1 and Q_2 are

set nominally in cut-off and behave as class C amplifiers. They do nothing until the VCO amplitude reaches the desired level (set by choosing an appropriate value for R_E). Once this level is reached, Q_1 and Q_2 turn on briefly at the top of the swing and steal current away from Q_4. This in turn reduces the current flowing in the oscillator until it is just enough to provide that level of output swing. Diodes D_2 and D_3 are used to provide a low impedance to short out the noise generated by the bandgap. C_1 is included to form a dominant and controllable pole in the feedback loop so that stability of the feedback loop is assured for all operating conditions. Note also that Q_1 and Q_2 are connected in such a manner so that they do not load the tank and provide additional loss when they turn on, impacting phase noise. This is a key advantage over previous designs that loaded the tank with the r_e of the limiting transistors [19]. In this case these transistors do not act as clamping diodes. An output buffer is also included that isolates the tank from all the circuitry in the transceiver that it must eventually drive. This is a bipolar buffer with a current output that is combined with other cores so that they can be conveniently switched on or off without loading each other.

The complete VCO subsystem is also shown in Fig. 8. All three VCO core's open collector buffers are tied together and brought to load resistors R_C through cascode transistors which are included to increase isolation to the RF buffers and therefore reduce chirp. Next the signal is driven into two buffer transistors Q_{10} and Q_{11} that are driven with enough current to drive the 5-GHz divider and three additional output buffers. The three buffers are fed to the transceiver RF mixers, and to the synthesizer buffer. The outputs of the second divider are used to produce quadrature differential signals that drive both transmit and receive IF stage mixers.

VII. VCO Pulling (Chirp) During Transmit/Receive Transitions

When a radio switches from transmit to receive mode or *vice versa*, buffers connected to the VCO are turned on and off. This can result in an instantaneous change in VCO frequency, commonly called "VCO chirp". This happens as a result of the load on the VCO "pulling" it as it changes impedance during the transient. In addition to this conducted pulling by the VCO load, there can be radiated and substrate coupling effects which can contribute to VCO chirp. Essentially, the cause of the chirp is a phase perturbation in the feedback loop of the VCO. The transient disturbance causes either a reflected or coupled signal to shift the loop phase momentarily. The amount of frequency shift is governed by the loaded Q or more specifically the group delay $(\tau_{\rm g})$ or phase slope of the VCO tank. Higher Q or $\tau_{\rm g}$ circuits are more immune to load pulling for the same reasons they have lower phase noise. Generally, the more isolation between the VCO and the source of the disturbance, the less chirp there will be. This is the reason that Q_8 and Q_9 were added to the circuit in Fig. 8. They increase the isolation between the VCO and the RF mixers, thus lowering the chirp.

VCO chirp due to load pulling can be analyzed in terms of a reflected signal summing with the dominant signal in the VCO loop. Fig. 9 shows a diagram illustrating the load pull analysis.

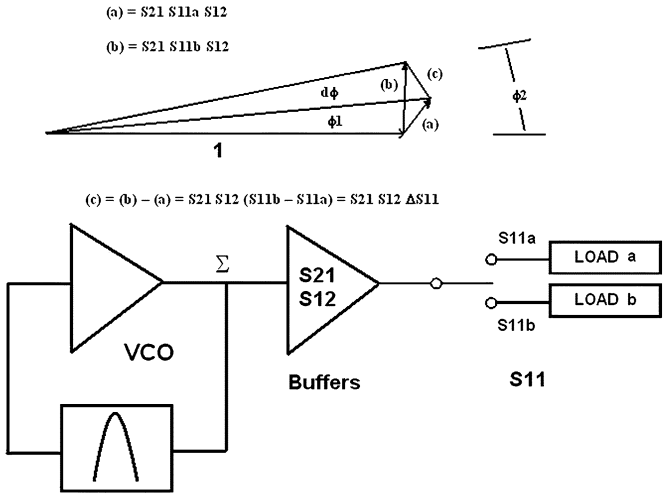

Fig. 9. Load pull analysis to determine frequency chirp.

The VCO tank has a loaded Q_l and buffer amplifiers with net gain S_{21} and reverse isolation S_{12} are cascaded between the VCO and the changing load. The instantaneous change in load impedance is represented by ΔS_{11} and the center frequency is represented by f_o.

Then a worst case reflected vector is determined and from this the net phase perturbation $d\phi$ can be calculated, which results from a summation of the incident vector and the reflected vector. Note the reflected vector is inherently normalized to the incident vector since it originates from it and the worse case reflected phase occurs for an orthogonal reflection. For the purpose of this calculation the incident vector is set to unity. Thus, starting from the definition of quality factor

$$Q_L = \pi f_o \tau_g = \pi f_o \frac{d\phi}{d\omega} = \pi f_o \frac{d\phi}{2\pi df} = \frac{f_o d\phi}{2df} \tag{3}$$

the change in frequency *df* can be determined:

$$\begin{aligned} df &= \frac{f_o d\phi}{2Q_l} \approx \frac{f_o \text{ang}(1 + S_{21}\Delta S_{11} S_{12})}{2Q_l} \\ &\le \frac{f_o \tan^{-1}(|S_{21}\Delta S_{11} S_{12}|)}{2Q_l} \approx \frac{f_o |S_{21}\Delta S_{11} S_{12}|}{2Q_l}. \end{aligned} \tag{4}$$

For close to unity gain buffers $S_{21} \approx 1$ and, therefore

$$df \approx \frac{f_o |\Delta S_{11} S_{12}|}{2Q_l} = \frac{f_o |\Delta S_{11}||S_{12}|}{2Q_l}. \tag{5}$$

The presence of the cascode transistors in Fig. 8 increased the reverse isolation through the buffers from approximately 50–80 dB. The change in S_{11} was simulated and (4) was used to estimate chirp as a function of buffer isolation (S_{12}). The worst case will be at low Q_l. To get close to 100–150-kHz VCO chirp at the worst case loaded Q point, with this analysis shows that 80 dB of isolation should be sufficient.

VIII. Synthesizer Phase Noise Analysis

The PLL noise is partitioned into six different blocks, which are modeled to predict the composite PLL noise. Fig. 1 illustrates the noise contributing blocks. The VCO (noise source 1) typically dominates the noise outside the PLL loop bandwidth

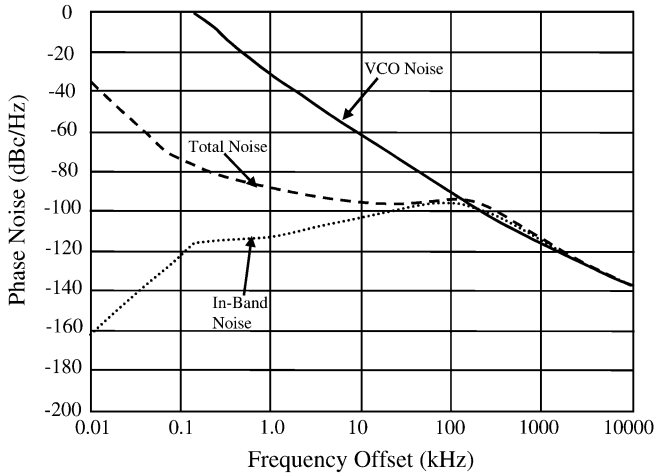

Fig. 10. Simulated optimum loop bandwidth at about 150 kHz.

and noise sources 2–6 contribute to the overall noise inside the PLL bandwidth. The bandwidth is typically set to lower the overall integrated noise, by choosing a bandwidth at the intersection of the total in-band and out-of-band contributors. Fig. 10 shows the intersection of the total in-band contributors with the VCO phase noise curve. This occurs at approximately 150 kHz, which corresponds to the optimum loop bandwidth for lowest integrated phase noise. The reason a wide loop BW could be achieved is due to the lowered in-band phase noise. The total simulated jitter was 0.5° to 0.6° for a 100 Hz to 10 MHz integration bandwidth. The loop filter is off-chip. Using external loop filter provides the flexibility of adjusting the close-loop performance and it saves a large amount of silicon area as well.

IX. Measured Results

The synthesizer was fabricated in a 47-GHz SiGe BiCMOS process with 0.5-μm lithography. The back end of the process featured thick aluminum metallization designed to provide high-quality inductors. The synthesizer was embedded with the rest of the circuitry that formed the 2-radio MIMO WLAN transceiver. A die photo of the chip is shown in Fig. 11. The entire MIMO transceiver chip is measured to be 4 mm $\times$ 3.1 mm and the synthesizer itself occupied an area of 2.3 mm $\times$ 1.4 mm.

The PLL settling times when the synthesizer switches from one WLAN channel to another have been measured. Fig. 12 shows the PLL settling time during various channel transitions. The loop bandwidth was set as 100 kHz and transition times on the order of 20–50 μs (2–5 time constants) were observed. Fig. 12(a) shows the transition between the end channels of the 802.11a band and Fig. 12(b) shows the transition between the end channels of the 802.11b band. Fig. 12(c) and (d) demonstrates the measured PLL settling process when the channel was switched from the 802.11a (5 GHz) to the 802.11b (2.4 GHz) bands and *vice versa*. Note switching between VCOs was involved in this transition and thus a longer setting time was observed.

The maximum frequency deviation of the synthesizer when enabling the transmitter is less than 150 kHz and the frequency error settles to 2 kHz in less than 12 μs. For the most part, the peak excursion has been reduced to 20–40 kHz with 2-kHz settling times of less than or equal to 5 μs. This can be compared to a previous prototype that did not include cascode transistors. Chirp in that experiment was as high as 500 kHz and the settling time was as high as 30 μs. Loop bandwidth cannot be optimized for fast settling time only. Fractional spur levels require bandwidths to be lowered for improved filtering and optimization of jitter places even a third constraint on the optimum loop bandwidth. This indicates that the additional buffering has effectively reduced the load pulling. Due to the asymmetry in the measurements, other mechanisms are starting to dominate the chirp such as proximity effects of the synthesizer to the various paths. These results are summarized in Table I.

To demonstrate the effect of loading pre-calculated seeds in $\Delta\Sigma$ accumulators, presented in Fig. 13 are the measured worst spur levels for the 802.11b channels, which correspond to the worst fractional spurs in this design with a fractionality of $1/30$. Fig. 13 clearly proves the proposed novel scheme of spur reduction using pre-calculated seeds. The 802.11a channels have a fractionality of $1/5$. All the 802.11a spurs were measured to be below -65 dBc.

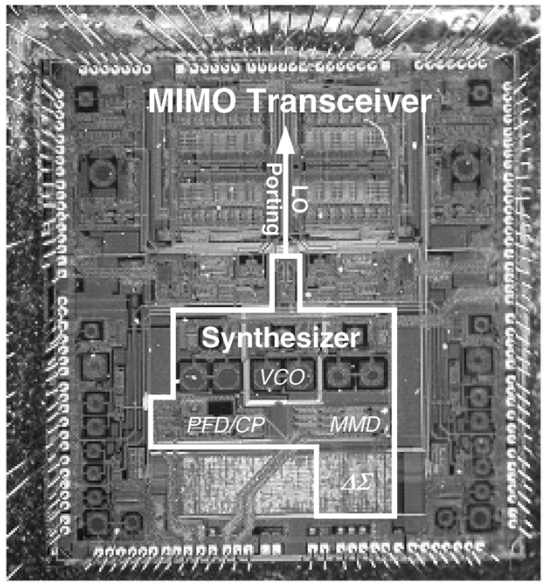

Fig. 11. Die photograph of the dual radio MIMO WLAN transceiver fabricated in a 47-GHz SiGe BiCMOS processing.

TABLE I
Transmit Enable Chirp Measurement

Path/Band	S12	BW	Chirp (kHz)	Settling Time (μs)
1/ 5GHz	79dB	100kHz	-13 to -20	3-13, 5 typ
2 / 5GHz	79dB	100kHz	-18 to -25	4-10, 5 typ
1/ 2.4GHz	79dB	100kHz	-20 to -150	<5
2/ 2.4GHz	79dB	100kHz	-27 to -43	<5
2.4GHz*	44-53dB	100kHz	500	30
2.4GHz*	44-53dB	200kHz	500	8

* Measurements from a previous prototype without cascode transistors.

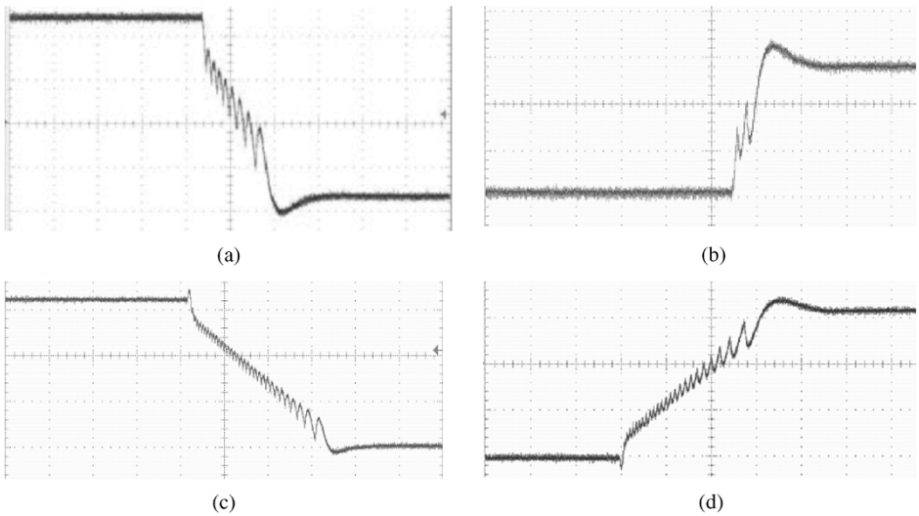

Fig. 12. Measured PLL settling times. Note the scale is 10 μs per division.

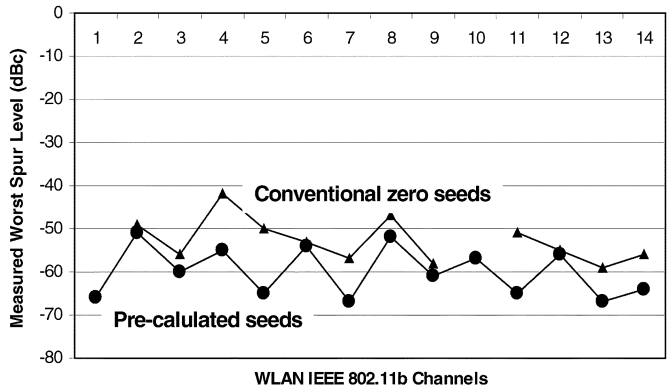

Fig. 13. Measured worst spur levels for 802.11b channels with pre-calculated seeds (bottom curve) and conventional zero seeds (top curve).

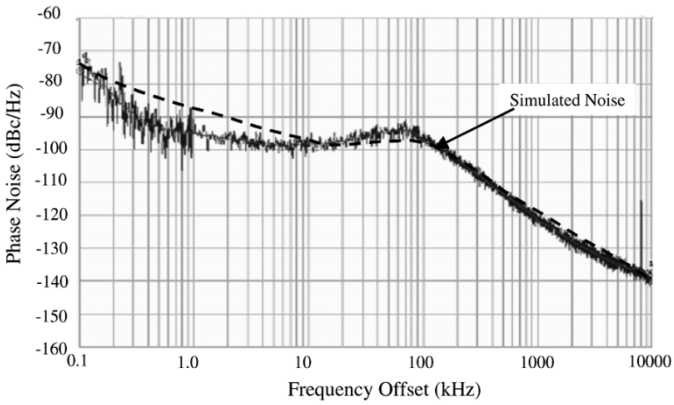

Fig. 14. Measured and simulated synthesizer phase noise plot.

The synthesizer draws a current of 36 mA from a 2.75-V supply. Fig. 14 shows a plot of the measured phase noise of the synthesizer output using the 802.11a band. For comparison, the simulated phase noise is shown in Fig. 14 as well. The simulated phase noise curve was derived from previous phase noise analysis and shows close agreement with the measured results. From the plot it can be seen that it has an in-band phase noise of −98 dBc/Hz at 10-kHz offset, and the VCO has an out-of-band phase noise of −120 dBc/Hz at 1-MHz offset. The phase noise was integrated from 100 Hz to 10 MHz. Using the 2.5-GHz VCO, the integrated jitter was less than 0.5° rms, and using the 5-GHz band, the integrated jitter was less than 0.9° rms. All spurious tones were less than −50 dBc in all bands and were less than −60 dBc for all 802.11a bands. The synthesizer performance is summarized in Table II and is compared to the most recently published WLAN synthesizer designs in Table III. Note that the presented work is the only synthesizer for MIMO applications reported so far.

TABLE II
SUMMARY OF SYNTHESIZER PERFORMANCE

Parameter	Performance
Technology	0.5μm SiGe BiCMOS
Supported Applications	IEEE 802.11a/b/g, Japan 2.4GHz and 5GHz bands
VCO Phase Noise	-120dBc/Hz @ 1MHz
In Band Phase Noise	-98dBc/Hz @ 10kHz
Loop Corner Frequency	100kHz
Reference Frequency	40MHz
No of accumulator/MMD bits	6
Order of ΔΣ accumulator	2^{nd} or 3^{rd}
Synthesizer step size	468.75kHz(802.11b/g) 781.25kHz(802.11a low/middle)
Spurious	<-50 dBc
Power Supply	2.75V
Current Consumption	36mA
Synthesizer die area	3.22mm^2
Integrated Phase Noise 100Hz to 10MHz	0.35~0.43°rms 802.11b/g 0.63~0.86°rms 802.11a

X. CONCLUSION

This paper has presented the implementation of a ΔΣ-based fractional-N frequency synthesizer in a 47-GHz SiGe BiCMOS process for 2.4- and 5-GHz multiband MIMO WLAN transceivers. To the best of the authors' knowledge, the synthesizer presented in this paper is the first published synthesizer design for multiband MIMO WLAN applications. Using a ΔΣ fractional-N architecture, a minimum synthesizer step size of 468.75 kHz (802.11b/g), and 781.25 kHz (802.11a mid/low), was achieved, which is sufficiently fine to cover the current

TABLE III
COMPARISON OF SYNTHESIZER PERFORMANCE

Ref.	Freq. Band GHz	Tech-nology	Phase Noise dBc/Hz @1MHz	Phase Noise dBc/Hz @10KHz	Integrated Phase Jitter
[1]	2.4, 5.1~5.8	0.25µm CMOS	-115	-105	0.7°rms, 5.3GHz 1KHz~10MHz
[2]	4.9-5.95	0.18 µm CMOS	-110	-90	
[3]	5.1~5.8	0.5 µm SiGe	-96	-90	
[4]	5.1~5.8	0.18 µm CMOS	-115	-92	0.8°rms 1KHz to 10MHz
[5]	5.1~5.3	0.18 µm CMOS	-110	-92	1.5~2°rms 10KHz~10MHz
[6]	5.1~5.3	0.18 µm CMOS	-110	-90	
This Work	2.4, 4.9~5.8	0.5 µm SiGe	-120	-98	0.4°rms, 2.4GHz 0.7°rms, 5.3GHz 100Hz~10MHz

WLAN standards with a step size of 5 MHz for 11b and 20 MHz for 11a. A an integrated phase noise from 100 Hz to 10 MHz of about 0.4° rms for 2.4-GHz band and about 0.7° rms for 5.3-GHz band was achieved. Using a single synthesizer with walking-IF architecture, the RF LO and IF LO for superheterodyne MIMO transceivers have been generated with a synthesizer current consumption of 36 mA. Also presented was the analysis and measurement of synthesizer locking time, phase noise, and VCO chirp performance.

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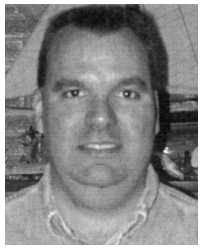
Dr. Dai has served as a Guest Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.



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