DVF4: A Dual-V_{th} Feedback Type 4-Transistor Level Converter

by

Karthik Naishathrala Jayaraman

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Approved by

Vishwani D. Agrawal, Chair, James J. Danaher Professor of Electrical and Computer Engineering
Victor P. Nelson, Professor of Electrical and Computer Engineering
Adit Singh, James B. Davis Professor of Electrical and Computer Engineering

Abstract

Power dissipation in digital circuits has become one of the primary concerns in electronic design. With the increasing usage of portable devices, there are severe restrictions being placed on the size, weight and power of batteries. Circuits consuming more power require batteries to be charged more frequently. It has therefore become important not only to optimize circuits for delay and area, but also for power. This has led to a growing interest in finding newer and more effective power reduction techniques. Power reduction techniques at various levels of abstraction have been used in modern digital world. The popular techniques include multiple supply voltages, multiple threshold voltages, clock gating, architecture techniques.

In this work we propose a *level converter* for dual supply voltages in digital designs in order to get a reduction in power consumption. This level converter can be used in circuit using multi supply voltages system where low supply gates are feeding high supply gates. The proposed level converter is compared with the existing level converter for power consumption and delay. The level converter is individually optimized for each supply voltage for low power consumption and then used with various simulation setups to indicate the advantage of using the proposed level converter. The saving on power consumption is upto 76% and the delay savings is upto 52% better than the existing level converters.

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"The essence of all beautiful art, all great art, is gratitude."

- Friedrich Nietzsche.

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And, Finally to the forever fascinating world, which keeps everyday interesting, thank you for keeping me alive and focused.

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Chapter 1

Introduction

The genesis of low power microelectronics can be traced to the invention of the transistor in 1947. The elimination of the crushing watts of heater power and several hundred volts of anode voltage in vacuum tubes in exchange for transistor operation in the tens of milliwatts range was a breakthrough of virtually unparalleled importance in electronics. The capability to fully utilize the low power assets of the transistor was provided by the invention of the integrated circuit in 1958. The motivation for low power electronics has stemmed from reasonably distinct classes of need, the earliest and most demanding of these is for portable, battery-operated equipment that is sufficiently small in size and weight and long in operating life to satisfy the user.

With much of the research efforts of the past ten years directed toward increasing the speed of digital systems, present-day technologies possess computing capabilities which make possible powerful personal workstations, sophisticated computer graphics, and multi media capabilities such as real-time speech recognition and real-time video. A significant change in the attitude of users is the desire to have access to this video on portable devices. A major factor in the weight and size of these portable devices is the amount of batteries, which is directly impacted by the power dissipated by the electronic circuits. Figure 1.1 shows the power dissipation against the critical dimension of various processors from the early days to the recent microprocessors.

Decreasing the supply voltage results in decreased performance. Hence, a trade off is necessary between power consumption and circuit delay. The use of multiple supply voltages to reduce energy consumption is a very commonly used technique in CMOS circuits. This results from the fact that the dynamic power of a CMOS circuit is directly proportional to

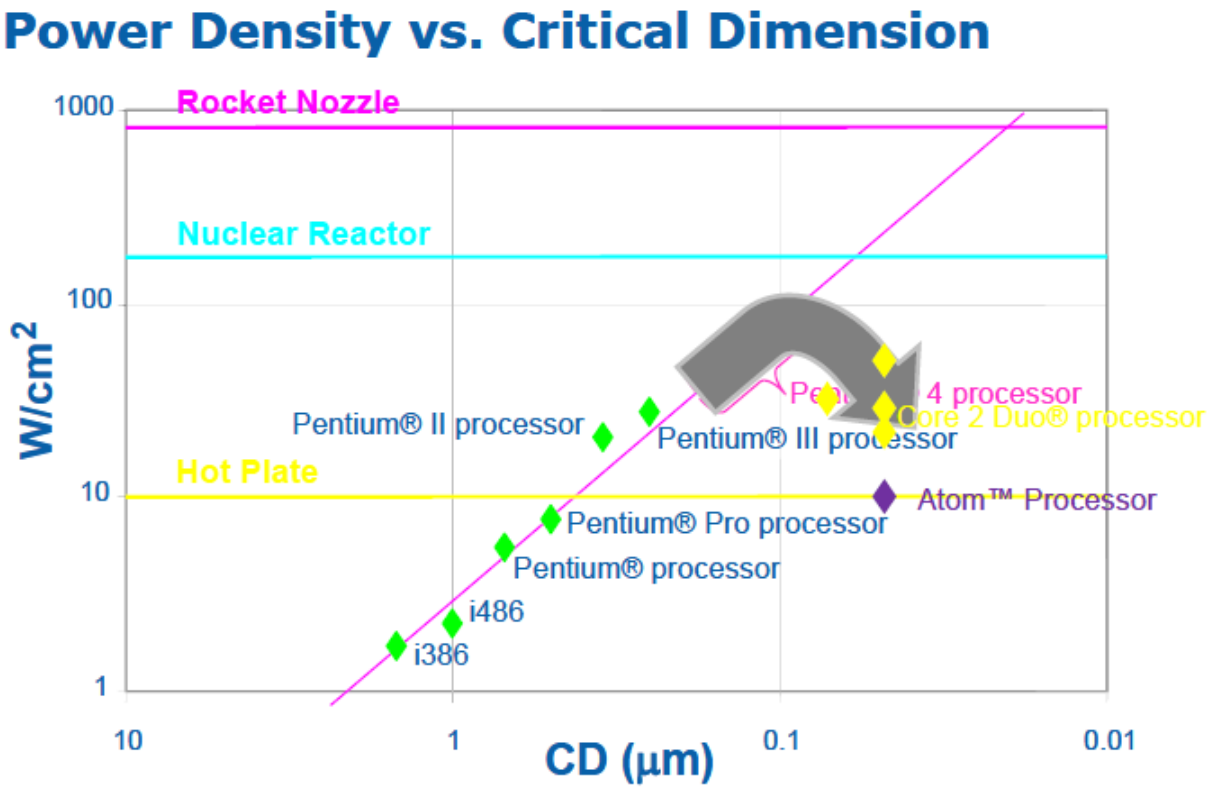

Figure 1.1: Power consumption in microprocessors [43].

the square of its supply voltage [8, 30]. Multiple thresholds and transistor sizing can be combined with voltage scaling to get more power savings, as described in articles [6, 11, 15, 19, 35, 39, 40, 41].

When using multiple supply voltages in a circuit we might need to convert the voltage level from one value to another voltage level, with level converters. There have been many level converters described in literature [13, 16, 21, 22, 23, 25, 32, 36, 42, 44, 48, 50]. The level converters either have high power consumption or high delay. The motive is to design a level converter that could save on power consumption and do not result in more delay. A good level converter is to operate the level converter at a low voltage level (preferably close to the threshold voltage), saving on power consumption and not causing high delay. We can use a slack based algorithm for dual voltage assignment and also allow level converter overhead and have energy savings.

1.1 Organization

The organization of this work is as follows:

In Chapter 2, we provide the background information on the various existing low power/energy-efficient design techniques. The sources of energy consumption in CMOS designs have also been detailed.

In Chapter 3, we discuss the various level converters described in literature and their relevant data is also discussed.

Chapter 4 discusses the proposed level converter and various advantages of using the level converter is discussed and the relevant data is provided.

Chapter 5 concludes the work by stating the advantages of the DVF4 level converter over the existing level converters.

Chapter 2

Theory and Background Work

2.1 Introduction

In the microprocessor world, performance is often measured in Millions of Instructions per Second (MIPS) or Millions of Floating Point Operations per Second (MFLOPS). The question of processor cost really depends on the implementation strategy being considered. For integrated circuits there is a fairly direct correspondence between silicon area and cost. Historically, the task of the VLSI designer has been to explore the Area-Time (AT) trade off attempting to strike reasonable balance between these often conflicting objectives. The Technology scaling has been and is of primary importance even today. Technology scaling not only makes if possible to integrate more transistors in a chip but also increase the performance of the devices. Now, with millions of transistors in a chip and with high frequency, the power consumption of devices becomes an important design constraint not only for the reliability of the chip but for making the packaging area smaller, mainly in portable devices. Technology scaling has directly impacted the power and energy constraints. With the increase in complexity of VLSI systems and limited amount of power available in certain scenarios like cell phones and digital cameras, minimizing power consumption has clearly become a priority. The passion for portable, powerful, yet durable devices gives us the motivation to find a design having acceptable power dissipation at compatible computational speeds.

2.2 Power Consumption

The power consumption of a CMOS circuit has two main components:

- Dynamic Power
- Static Power

All of the power consumed in a chip can be attributed to these two broad categories [10, 17, 37, 49]. In other words, It can be summarized as,

$$P_{Total} = P_{Dynamic} + P_{static} \tag{2.1}$$

Where,

P_{Total} is the total power consumed by the circuit

$P_{Dynamic}$ is the switching power due to the transitions and a small fraction of short circuit power from VDD to Ground.

P_{Static} is due to the leakage currents in the circuit.

2.2.1 Dynamic Power

Until the onset of 65nm technology, dynamic power dominated power dissipation in CMOS circuits [30]. It is caused by the charging and the discharging of the output node capacitance. Dynamic power can be written as,

$$P_{DynamicPower} = P_{Switching} + P_{Short-circuit} \tag{2.2}$$

Dynamic power is caused by three constraints, namely

1. Logic Activity or Switching Power

   Dynamic power due to logic activity can be expressed as

$$P_{Switching} = \alpha.f.C_L.VDD^2 \tag{2.3}$$

   Where,

   α is the switching or the activity factor

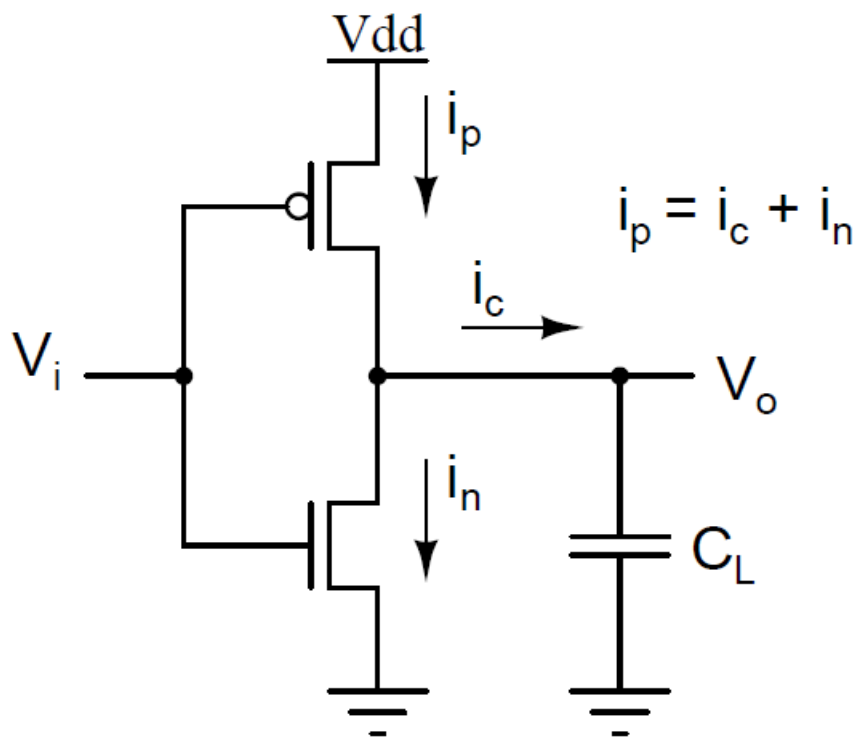

Figure 2.1: A CMOS inverter circuit.

f is the frequency at which the circuit operates

C_L is load capacitance of the circuit

VDD is the supply voltage

2. Glitches

   Dynamic power due to glitches occurs when there is unwanted signal activity due the timing variations at the inputs of the gates.

3. Short-Circuit Power

   Short-circuit power [26] occurs when both the PMOS and NMOS transistor are on at the same time. Figure 2.1 shows a CMOS inverter circuit and the currents associated with its operations. The inverter operates at VDD and an input voltage V_i, V_{th} is the

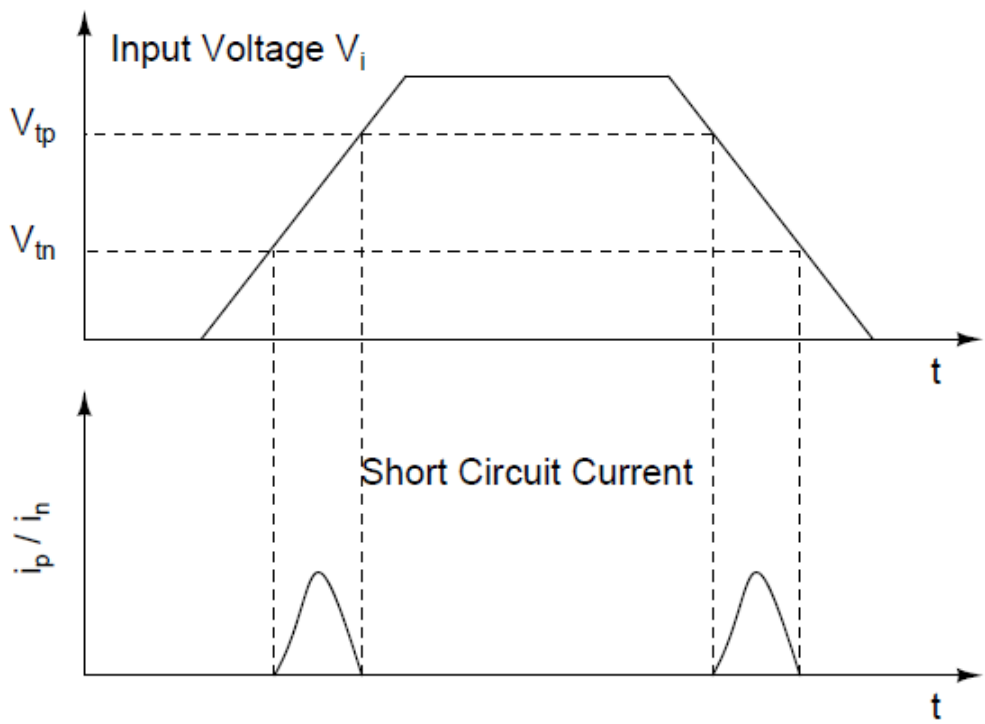

Figure 2.2: Short circuit current of a CMOS inverter during input transition.

threshold voltage of the NMOS transistor, V_{tp} is the threshold voltage of the PMOS transistor, and V_o is the output. When V_i is changed from Low (0) to High (1) there is short period of time where both the PMOS and NMOS transistors are on at the same time. During this time there is a conduction path from VDD to Ground. This phenomenon is illustrated in the Figure 2.2. The conduction period depends on two factors:

- Increases with the size of the transistors.
- Decreases with load capacitance of the inverter.

The short circuit power can be written as

$$P_{SC} = VDD.I_{SC} \tag{2.4}$$

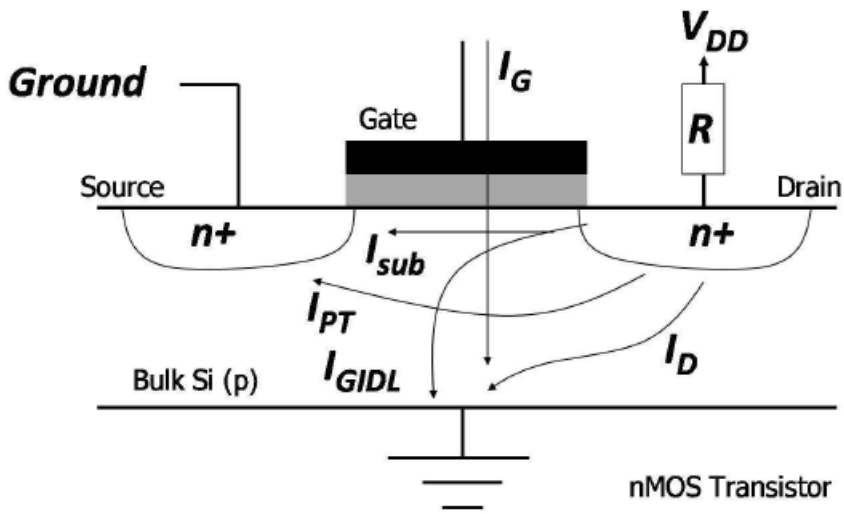

Figure 2.3: Leakage currents in an NMOS transistor.

Where,

I_{SC} is the short circuit current.

VDD is the supply voltage.

2.2.2 Static Power

CMOS has no static power when switching does not take place. But the semiconductor devices conduct or leak through the reverse biased channels and provide a path from VDD to ground and this constitutes static power consumption. There are various sources of leakage currents and we will be explaining the primary sources. The various sources of leakage currents are shown in Figure 2.3.

- Sub-threshold Leakage (I_{sub}) [29] In the OFF state, even though the transistor is logically turned off, there is a non-zero leakage current flowing through the channel. This is known as sub-threshold leakage current. The magnitude of this current depends on threshold voltage, v_{th}; gate voltage, v_{gs}; drain voltage v_{ds} and temperature. In the OFF state $v_{ds} \approx VDD$ so the sub-threshold current essentially depends on v_{gs}. It can

be written as

$$I_{sub} = \mu.c_{ox}.V_t^2.\frac{W}{L}.e^{\frac{(V_{gs}-V_T)}{n.V_{th}}} \tag{2.5}$$

Where

W, L are dimensions of the transistor.

V_{th} is thermal voltage.

n is a function of the device fabrication process which ranges from 1.0 to 2.5.

Sub-threshold current is becoming a limiting factor in low voltage and low power chip design. When operating voltage is reduced the device threshold voltage V_{th} has to be reduced accordingly to compensate for loss in switching speed.

- Gate Tunneling Current (I_G)

  With scaling of the channel length, a good transistor aspect ratio ($\frac{W}{L}$) can be maintained only by comparable scaling of oxide thickness, junction depth and depletion depth. Maintaining this aspect ratio is a challenge since the scaling in the vertical direction is difficult. Gate leakage occurs as a result of tunneling current through the gate oxide. Gate leakage flows directly from the gate through the oxide to the substrate due to gate oxide tunneling and hot carrier injection. The oxide thickness limit will be reached approximately when I_G becomes equal to I_{sub}.

  This limitation can be resolved by making use of different materials with high permitivity as the gate dielectric. This will result in thicker and easier to fabricate dielectric with potential for significant reduction in leakage current [28]. Such an implementation in high-k dielectric in 45nm technology by Intel for their processor series "penryn'.

- Reverse-biased PN-Junction current (I_D)

  Reverse-bias junction leakage occurs from source or drain to the substrate through reverse-biased diodes when a transistor is OFF. It is caused by minority carrier drift and generation of electron/hole pairs in the depletion regions. For instance, in the case

of an inverter with low input voltage, the NMOS is OFF, the PMOS is ON, and the output voltage is high. Subsequently, the drain to substrate voltage of the OFF NMOS transistor is equal to the supply voltage. This results in a leakage current from the drain to the substrate through the reverse-biased diode. The magnitude of the diode leakage current depends on the area of the drain diffusion and the leakage current density, which in turn are determined by the process technology. It can be expressed as [52]

$$I_D = I_S.(e^{\frac{v}{v_{th}}} - 1) \tag{2.6}$$

Where,

I_S is the reverse saturation current,

V_{th} is thermal voltage which is given by $V_{th} = kT/q$, where $k = 1.38$ x 10^{-38} Joule/K is Boltzmann constant, q is electronic charge in Coulombs and T is device operating temperature.

I_D is largely independent of operating voltage but depends in general on temperature, process, bias voltage and area of the PN-Junction.

Other sources of leakage current, such as Gate Induced Drain Leakage current (I_{GIDL}) and drain source Punch Through current (I_{PT}), also contribute to total leakage current. Leakage currents are exponentially increasing with the scaling of CMOS. They increase with the decrease in threshold voltages and the length of the transistors. The operating temperature increases during device operation. This causes an exponential increase in the leakage currents.

The power dissipated by CMOS digital circuits can be reduced while retaining the required functionality and performance. An outline of few of techniques proposed for the power reduction in CMOS circuits is given in the following section.

2.3 Power Reduction in CMOS Circuits

Low power methods for design of circuits can be classified in many different ways. One of the classic papers in this area [14] describes these techniques in three simple categories as,

1. Trade area or speed for power
2. Don't waste power and
3. Find a low power problem.

The generation, distribution and dissipation of power are now at the forefront of current problems faced by IC designers. Failure to meet the power budget of a chip exposes it to failures from packaging, cooling challenges, reliability issues, timing degradation and increased leakage. Minimizing power consumption in digital circuits can be done either by slightly altering the characteristics of transistors at the fabrication level, or by making changes at the implementation level, or the architecture of the basic building blocks of a complex CMOS system. In designing, power reduction can be achieved by making low-power dissipation the key objective of the design, by reducing the number of primitive gates and the resistive paths connecting them. This reduction decreases the overall power dissipation of the system.

2.3.1 Technology Scaling

This technique proposes to scale all the voltages and linear dimensions of the transistor by a constant factor (γ >1), so that the electric field remains the same as shown in Figure 2.4 [30, 31, 33].The energy scales by a factor γ^3, as both voltage and current are scaled by γ. The delay is improved by a factor γ. Hence the energy-delay product decreases by a factor γ^4. But this method requires all voltages to be scaled down, including the threshold voltage. But the threshold voltage is limited by the leakage current through the OFF transistors and allowable static power [14, 30, 31].

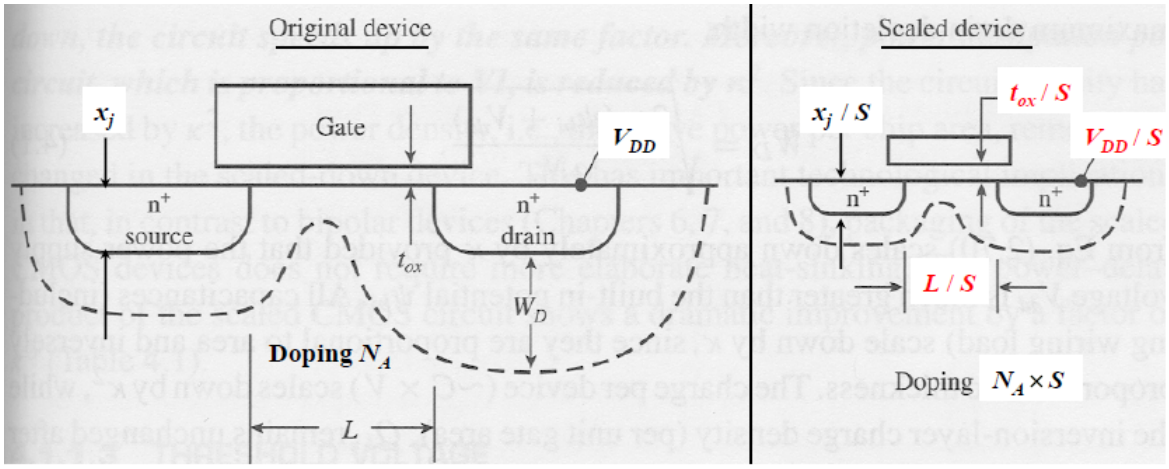

Figure 2.4: Scaling of transistor dimensions [1].

In recent technologies, the supply voltage has reached 1V. This has imposed physical limitations to scaling. The built-in potentials of the device and Si band-gap energy do not change with scaling. They can be adjusted to required levels by increasing the doping or forward biasing the substrate. Because of thermodynamic limitations, the threshold voltage of a device cannot be scaled further while keeping the leakage currents manageable. Reaching this ultimate level of scaling is stalled by increasing the electric field in the device by a factor $\epsilon(>1)$. But this increases the power dissipation and decreases the reliability of the device. Hence, there is a limit to this scaling process due to various physical phenomena and alternative methods should be chosen to overcome this [30].

2.3.2 Voltage Scaling

This method employs reduction of supply voltage. From Equation 2.3, we can see that the reduction in voltage will cause quadratic reduction in dynamic or switching power. Supply voltage scaling also reduces the leakage power since the gate leakage and GIDL and DIBL leakage components also decrease [29]. By reducing the supply voltage, and with capacitance and threshold voltage of the devices constant, the performance of the system decreases. At voltages near the device threshold, small supply changes cause a large change

in delay for a modest change in energy. The different voltage scaling methods are listed as follows [17].

1. Static Voltage Scaling (SVS) - Different blocks and sub-blocks in a design are given different fixed supply voltages. The block which fails the critical delay is given a higher voltage than the neighboring blocks. If two voltages are supplied then it can be called as Dual-VDD Design. If more than two supply voltages are given it can be called as Multi-VDD Technique.

2. Multi-level Voltage Scaling (MVS) - The technique is a mere extension of the static voltage scaling, where the blocks are operated between two or more supply voltages.

3. Dynamic Voltage and Frequency Scaling (DVFS) - This is an extension of Multi-level voltage scaling, where a larger number of voltage levels are dynamically switched between to follow changing workloads.

4. Adaptive Voltage Scaling (AVS) - An extension of DVFS where a control loop is used to adjust the voltage.

Figure 2.5 shows the impact of voltage scaling on the power-delay product. As noted from Equation 2.3, power per transition is proportional to v^2; this is seen from Figure 2.5, which is a plot of two experimental circuits which exhibit the expected v^2 dependence. Therefore for every possible reduction in supply voltage we get quadratic improvement in the power-delay product [7].

2.3.3 Clock Gating

This is a very popular technique used in many synchronous circuits to reduce power consumption. In synchronous CMOS circuits, at the block level, if the clock is gated to the functional blocks, the inactive blocks are effectively turned OFF by stopping the clock. This transition avoids the switching of the nodes in inactive blocks of the system while

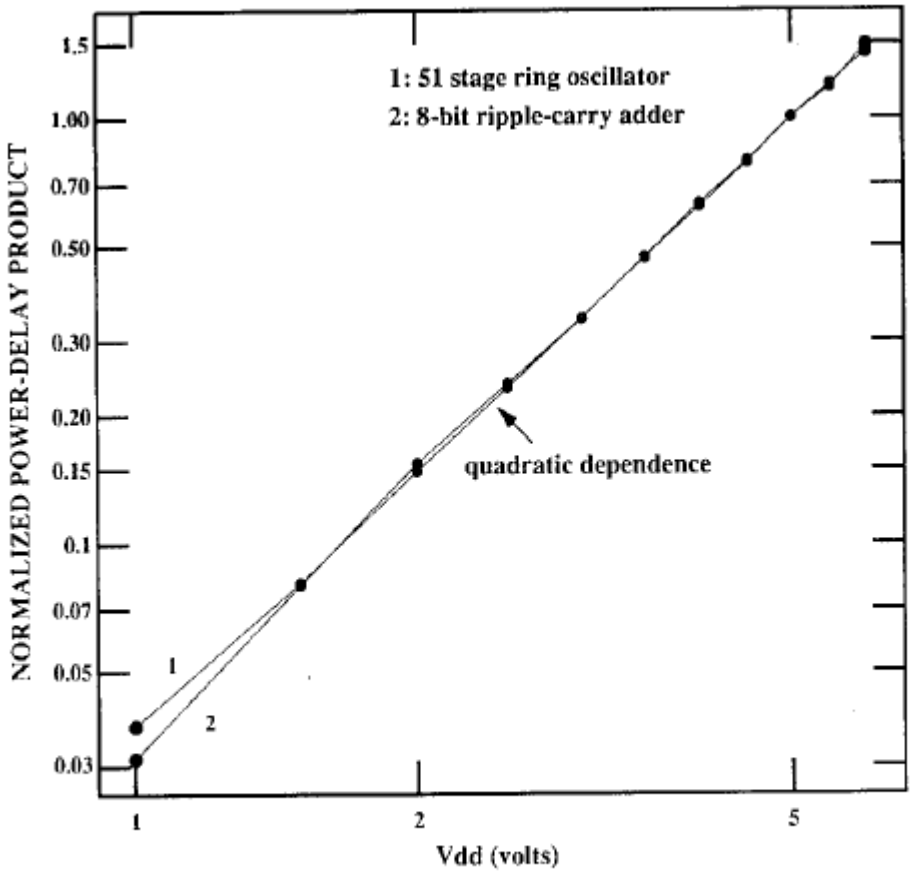

Figure 2.5: Impact of voltage scaling on power-delay product [7].

maintaining their logic values [29, 30]. From Figure 2.6, when the enable is 1, the circuit functions normally. When the enable is 0, the clock signal is cut off and the activity in the flip flop is stopped. Clock gating decreases the switching activity in the flip flops and the gates in the fan-out of flip-flops, thereby causing a reduction in the dynamic power of the circuit. The influence on performance of the CMOS circuit is minimal [30].

2.3.4 Power Gating

Power-gating is a technique used to reduce the sub-threshold leakage power of CMOS circuits. A high v_{th} PMOS transistor(header) or a high v_{th} NMOS Transistor(footer) controlled by a sleep signal, is used to isolate the supply VDD or the VSS, respectively, from the logic outputs and thereby stopping the flow of short circuit currents into the active blocks

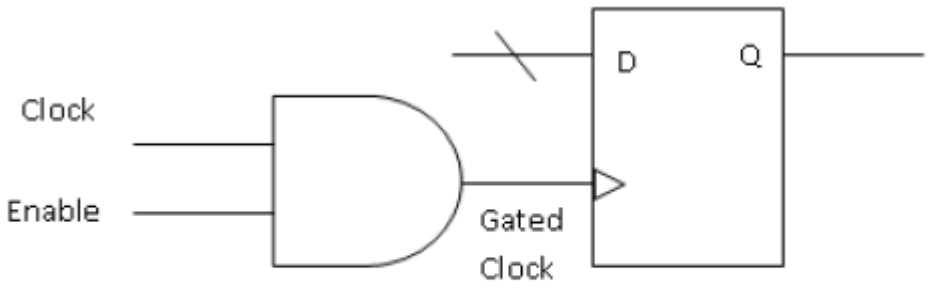

Figure 2.6: Clock gating in flip-flops.

connected to the power-gated block outputs [29, 38]. The above mentioned two implementations are shown in Figure 2.7. Usually, any one of the schemes is implemented. PMOS header is normally used when compared to NMOS footer to reduce leakage currents.

The sleep transistor has to be designed carefully so that the voltage drop is not very high during the active state. This ensures that the effective supply voltage to the logic block is maintained at VDD [30]. Since there is dynamic power consumption associated with the turning ON/OFF of the sleep transistor, the power savings associated with the stand-by mode of a power gated logic block should be more than the power consumed while turning ON/OFF of the sleep transistor. The grouping of logic blocks for power gating implementation is also important.

Power gating affects design architecture more than clock gating. It increases time delays, as power gated modes have to be safely entered and exited. Architectural trade-offs exist between designing for the amount of leakage power saving in low power modes and the energy dissipation to enter and exit the low power modes. Shutting down the blocks can be accomplished either by software or hardware. Driver software can schedule the power down operations. Hardware timers can be utilized. A dedicated power management controller is another option.

A header is recommended when a switch is sized such that lower delay penalty can be tolerated, but a footer is superior when delay penalty is larger [20]. When a low-V_{th} sleep

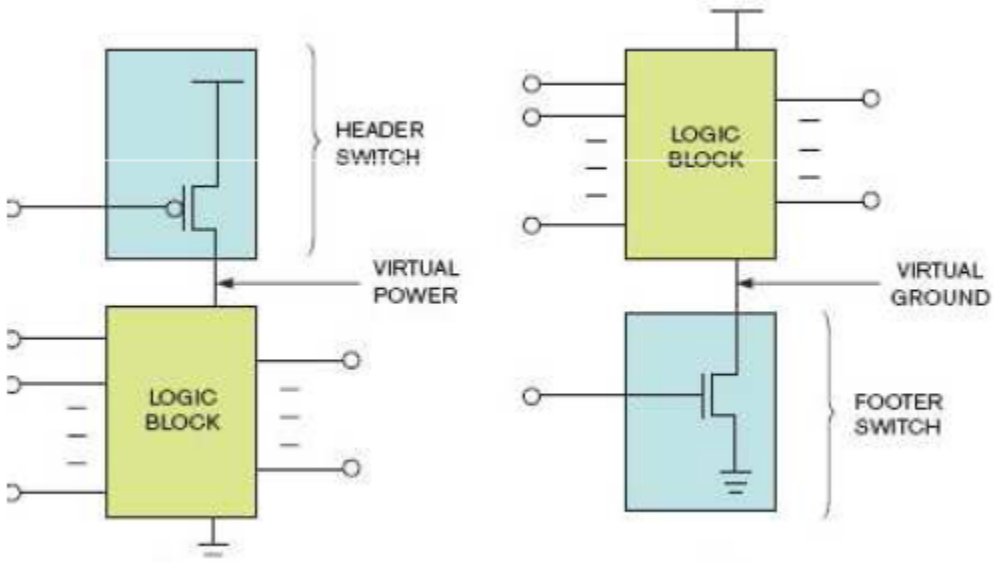

Figure 2.7: Power-gating with transistors (header and footer).

transistor is used instead of a high-V_{th} transistor, a footer is always better than a header. This is because the sub-threshold leakage current of a switch now makes up a large portion of the total leakage currents due to its exponential dependency on the threshold voltage, and the sub-threshold leakage current is smaller in a footer than in a header due to the smaller size of a footer with the same delay penalty.

The power consumption of power gating circuits can be further reduced by controlling primary inputs. By providing logic 1 to all primary inputs of a power-gated circuit with a footer (similarly logic 0 in the case of a header), input gate leakage currents can be virtually eliminated. However, the gate leakage current of a footer goes up due to the elevated voltage of a virtual ground. This is because the additional transistors in input control circuits induce current that flows through a footer in addition to the current from the logic block [20]. Also, when the logic is cut off from the ground using a leakier footer transistor, the difference in the potentials between this virtual ground and the VSS will cause ground noise resulting in signal integrity problems [17, 38].

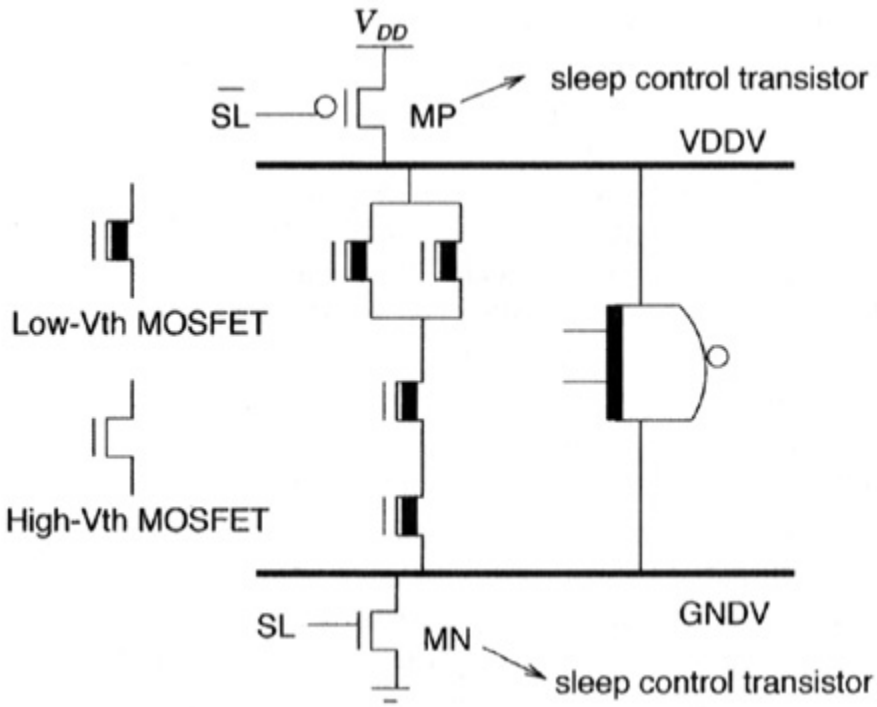

Figure 2.8: Schematic of Multi-threshold CMOS [34].

2.3.5 Dual/Multi-threshold Designs

The threshold voltage of a transistor is given by

$$v_{th} = v_{th0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F}) \tag{2.7}$$

where v_{th0} is the the zero source-bulk bias threshold voltage,

V_{SB} is the source-to-body substrate bias

ϕ_F is the substrate Fermi potential,

γ is the body-effect coefficient.

This shows that reverse body biasing a transistor increases threshold voltage and thus decreases the leakage current [30]. Multi-threshold CMOS uses both high and low-threshold voltage MOSFETs in a single chip and a sleep control scheme is introduced for efficient power management.

In Figure 2.8, in the active mode, SL is set high and the sleep control transistors (MP and MN) are turned on. The on resistances of the sleep transistors are small. Hence VDDV and GNDV function as real power and ground lines. In the standby mode, SL is set to low, MN and MP are turned off, and VDDV and GNDV are floating. The leakage current is suppressed by the high-V_{th} MOSFETs MN and MP. The technique is simple and achieves a large improvement in leakage current. However one of the main disadvantages is the use of sleep control transistors, which can affect performance. It should also be noted that the sleep transistors can be large and hence, the capacitance being switched for turning on or off those transistors can be large.

2.3.6 Variable Threshold CMOS (VTCMOS)

In this technique a zero body bias is used in the active mode and a high reverse body bias is applied in the standby mode to increase the threshold voltage, thereby decreasing the standby leakage. This capability of reverse body biasing to reduce the leakage current lowers as the technology scales [18, 29]. This is because of the exponential increase in the band-to-band tunneling current at the source-substrate and drain-substrate junctions in scaled technologies [18, 29].

Authors in [45] have described a technique which reduces the standby leakage by using high-V_{th} devices and during active mode a forward body bias is applied to reduce the V_{th}. This reduces the short channel effects, limiting the reduction of the leakage current. It has been shown that forward body biasing with high-V_{th} and reverse body biasing reduces leakage 20 times while only reverse body biasing with low-V_{th} reduces leakage only 3 times [29].

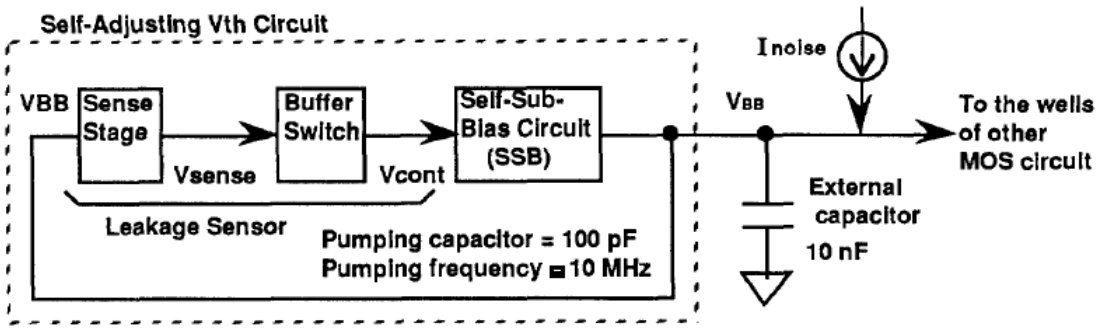

Figure 2.9: Block diagram of self-adjusting threshold-voltage scheme (SATS) [34].

2.3.7 Self-Adjusting Threshold-Voltage Scheme (SATS)

Figure 2.9 shows a block diagram of the self-adjusting threshold voltage scheme (SATS). A leakage sensor senses a representative MOSFET and outputs a control signal to the self-sub-bias (SSB) circuit. Consider an nMOSFET transistor. When the leakage current is higher than a certain value, the SSB will be triggered and will reduce the substrate bias of all the other nMOSFETs, which in turn will increase the threshold voltage and reduce the leakage current. For pMOSFETs, a similar technique can be used.

2.3.8 Dynamic Threshold Voltage

Body biasing techniques are used to change the threshold voltage according to the performance requirements. When performance demand is low, clock frequency is lowered and the threshold voltage is increased to reduce run-time leakage. In standby the threshold voltage is increased to its maximum limit to reduce the standby leakage. A zero body bias with lowest possible threshold is used when the performance requirements are the highest [29].

2.3.9 Variable supply and threshold voltages

The threshold voltage and the supply voltage can be varied simultaneously to get required power and timing efficiency. The ON current of a transistor is given by,

$$I_{DS} = \mu.C_{ox}.\frac{W}{L}.\frac{(V_{GS} - V_{th})^2}{2} \tag{2.8}$$

where μ is the mobility,

C_{ox} is the gate oxide capacitance,

V_{th} is the threshold voltage,

V_{GS} is the gate-to-source voltage.

As we reduce the supply voltage, the input voltage swing, V_{GS} is also reduced. To maintain the performance, the current drive, I_{DS}, has to be maintained. For this, the threshold voltage also has to be decreased. If we use low-VDD and low-Vth, the power dissipation will increase because lowering Vth results in exponential increase in the sub-threshold leakage current. Hence, we require lower VDD and higher Vth on non-critical paths to reduce power and maintain performance on the critical paths. We can also use dynamic supply scaling and dynamic threshold scaling together to reduce power [31, 30].

2.3.10 Transistor Stacking

Using a stack of transistors in the OFF state reduces the leakage current because of the negative gate-to-source biasing, body-effect induced threshold voltage increases, and increased threshold voltage due to reduced drain-to-source voltage. The time required for the leakage current in the transistor stacks to converge to its final value depends on the intermediate node capacitances and the threshold voltages of the transistors [51]. Turning off more than one transistor in the stack increases the source voltage of the stack and thus,

reverse biases the source. These reverse biases reduce the leakage currents through the transistors [29].

2.4 Conclusion

A reduction of power dissipation is important to save energy. Lower power dissipation decreases the heat generated within the chip, in between the individual transistors. This reduction in heat further increases the level of integration and thus, contributes towards further reduction of size. Besides, the lower dissipation allows the packaging to be done using light plastics and there is reduction in the size of devices by eliminating the need for cooling such as fans, etc. Hence, to increase the portability of the electronic devices power dissipation must be lowered. This allows their manufacturing to be done at lower costs and also reduces the chip area.

Chapter 3

Level Converters for Dual-Voltage Design

3.1 Introduction

Dynamic power dissipation in CMOS circuits is proportional to the square of the supply voltage (VDD) [30]. A reduction in VDD thus considerably lowers the power dissipation of the circuit. Dual-VDD (or more generally multi-VDD)design is an important scheme that exploits this concept to reduce power consumption in integrated circuits (ICs) [46, 9]. Since reduction in VDD degrades the circuit performance, inorder to maintain performance in dual-VDD designs, cells along critical paths are assigned to the higher power supply ($VDDH$), while cells along noncritical paths are assigned to the lower power supply ($VDDL$). In a dual-voltage design level converters are required whenever a low voltage gate feeds a high voltage gate or vice versa. High to low level converters are used when a low voltage gate feeds a high voltage gate to eliminate the undesirable short-circuit flows from VDD to GND in dual-VDD design. From Figure 3.1 where two inverters are connected together. When the output of first stage is high, the upper PMOS of the second stage is not completely turned off because its gate-source voltage is not equal to zero and the static power would be increased. Static power is an ascending function of the difference between $VDDL$ and $VDDH$. Therefore, while a smaller $VDDL$ gives rise to less dynamic power consumption, it increases the static power in the interface of low to high supply voltage stages. According to the number of these connections, the total power consumption may be increased or decreased. In this chapter we will discuss various level converter designs available in the literature.

Figures 3.6 through 3.11 show various designs of level converters proposed in the literature. For each level converter, average power dissipation, rise delays and fall delays have

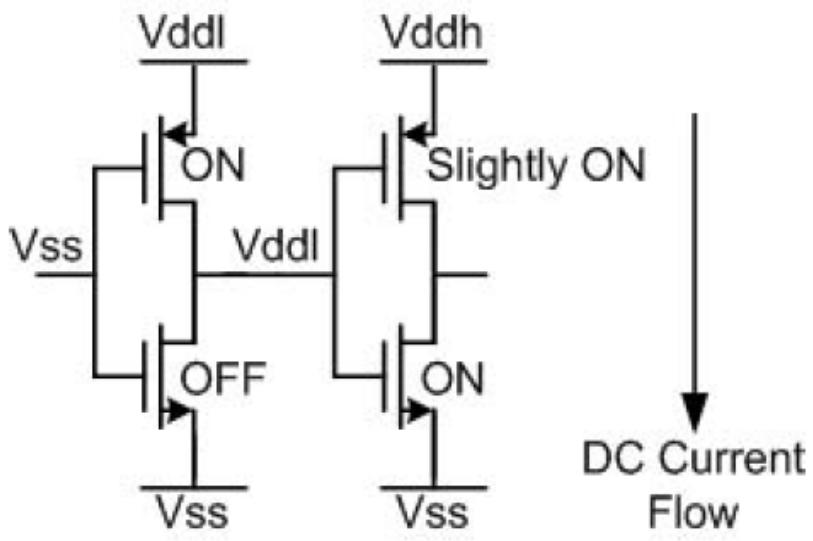

Figure 3.1: Short circuit current in Dual-VDD design.

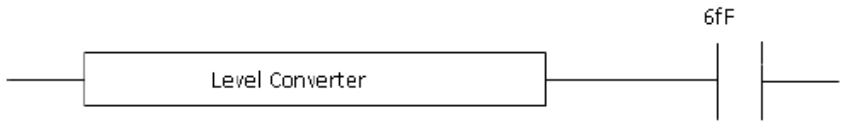

Figure 3.2: Experimental setup for level converter simulations.

been recorded in Tables 3.1 through 3.6 for various designs at various voltage values. The simulations are done in HSPICE [3]. For the simulations, the level converter output is loaded with a capacitor of 6fF as shown in Figure 3.2, which is equivalent to a inverter, which is the size of four standard inverters at the output as shown in Figure 3.3. The technology used for the simulation is the 32nm Predictive Technology Model with 0V for logic 0 and VH for logic 1, which is 1.0V. The simulation is done for 10 cycles. If the level converter functionally fails there is no data that can be recorded for comparison. The motivation is to have an inverter as a target for power consumption and delay. The simulations of various level converters are compared with one inverter for both power consumption and delay.

A level converter can be used in two ways: High to Low converter and low to high level converter. For most cases high to low level converters are not used, because the high voltage

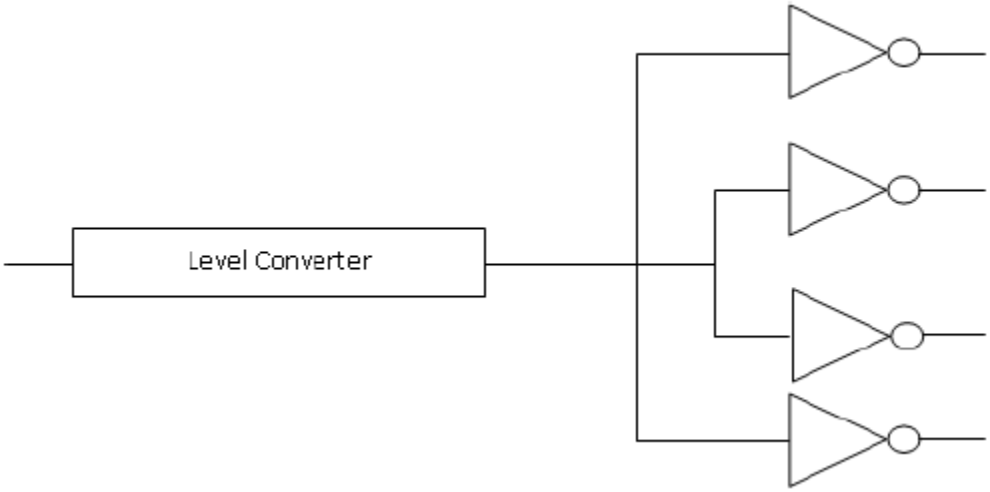

Figure 3.3: Equivalent to standard inverter.

is sufficient for feeding the low voltage gates for the gates to function to its requirement. So low to high level converters are preferably used [24].

There are two algorithms that are primarily used in assigning VDD to gates so that level converters can be used. They are,

1. Clustered voltage scaling (CVS) [24]

   In CVS, the cells driven by each power supply are grouped (clustered) together and level conversion is needed only at sequential elemental outputs.

2. Extended Clustered Voltage Scaling (ECVS) [47]

   ECVS, the cell assignment is flexible, allowing level conversion anywhere (not just at the sequential element outputs) in the circuit.

Level converters are of two types:

1. Feedback Based Level Converters [42]

   Feedback based level converters as the name suggests depend on some form of feedback circuitry. When a low-swing signal directly drives a gate that is connected to a higher

supply voltage, the pull-up network of the receiver cannot be fully turned off. The receiver therefore produces static DC current. In order to suppress this DC current, feedback-based level converters isolate the pull-up network from the low-swing input signal. These traditional level converters, however, suffer from high short-circuit power and high propagation delay due to the typically slow response of the feedback circuitry. Furthermore, the pull-down network in these circuits is driven by low voltage swing signals while the pull-up network is driven by full-swing signals. At very low input voltages, the widths of the transistors that are directly driven by the low-swing signals need to be significantly increased in order to balance the strength of the pull-up and the pull-down networks. This causes further degradation in the speed and the power efficiency of the conventional level converters.

2. Multi-Threshold Level Converters [42]

   Unlike the level converters that depend on feedback circuits multi-threshold level converters employ on Multi-V_{th} CMOS technology in order to eliminate static DC current. This enables the level converter to save more power and delay is also reduced.

A level converter can be used in two different ways between a low voltage gate and a high voltage gate. We can use a level converter at the fan-in of each high voltage gate that comes from a low voltage, as shown in Figure 3.4, and by putting a level converter at the output of low voltage gates that feed into at-least one high voltage gate. This is shown in Figure 3.5

3.2 Various Level Converters

3.2.1 Standard Level Converter

Standard level converter is shown in Figure 3.6 [32, 48]. The circuit operates as follows. When the input IN is at 1V transistor TN1 is turned ON and hence node OUT1 would assume a low value. This turns on transistor TP2. The low output from the inverter which is supplied with a low voltage turns off transistor TN2 and hence node OUT2 assumes a high

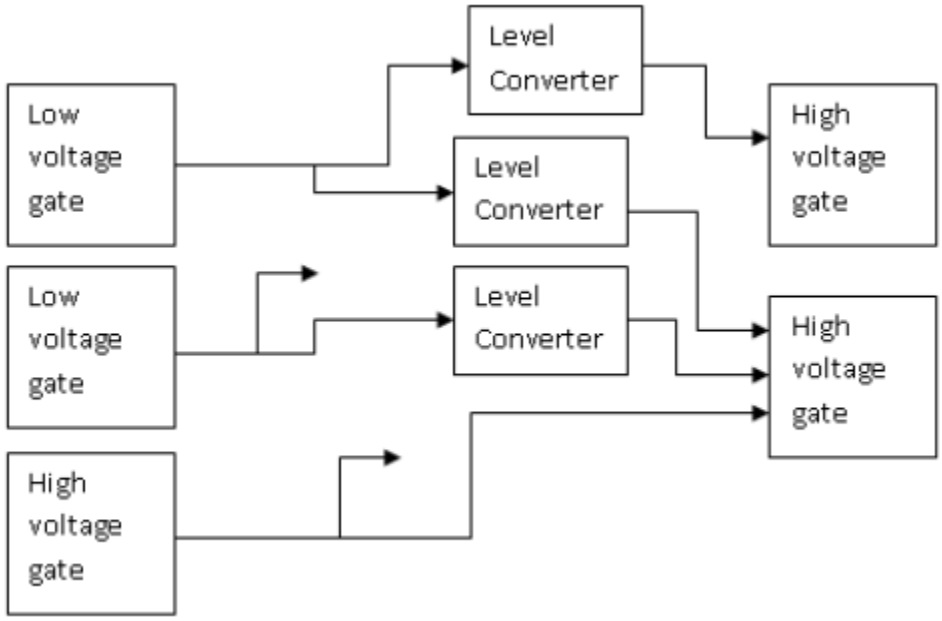

Figure 3.4: Level converter inserted before each fan-in of a high voltage gate.

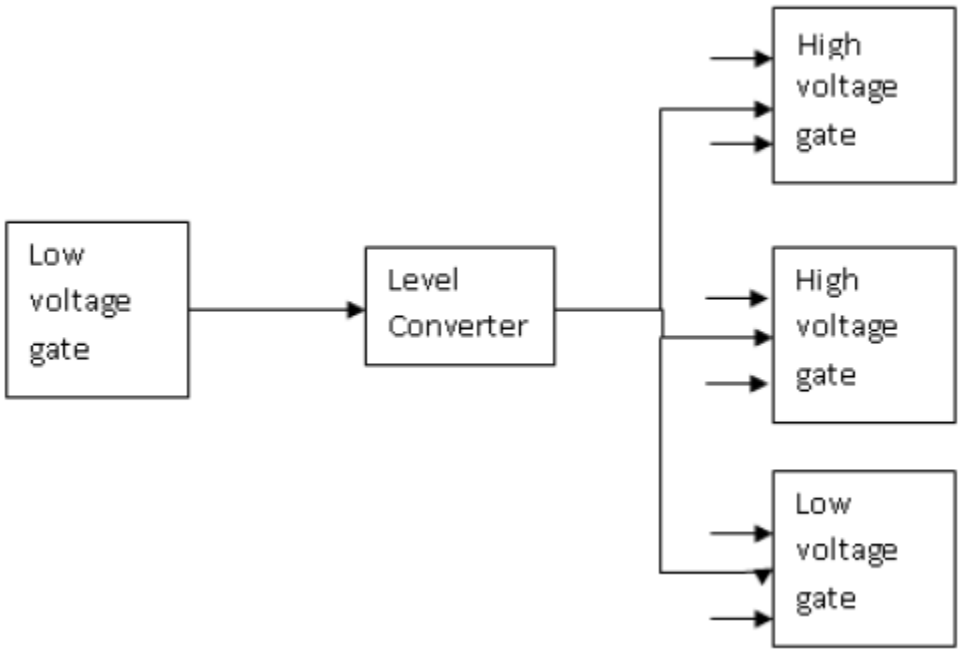

Figure 3.5: Level converter inserted at the output of a low-voltage gate.

Table 3.1: Standard level converter, V_H = 1.0V.

InputVoltage V_L volt	Average power μW	Rise delay ps	Fall delay ps
1.0	0.457	18.0	16.92
0.9	0.430	21.0	17.3
0.8	0.409	24.3	24.1
0.7	0.452	32.9	36.3
0.6	0.508	49.3	61.4
0.5	0.755	108	144
0.4	2.247	584.3	806.5

value of VDD2. This in turn would turn off transistor TP1. Thus, a high input at a lower voltage level is converted into a high output of VDD2. When the input is low (0V), this makes the output of the inverter high, this high signal is fed to the input transistor TN2. This makes the node OUT2 to be a low voltage, which will turn on TP1, so OUT1 will be high. This high will turn OFF the TP2 transistor making node OUT2 to remain at 0V [27]. The HPICE simulations are tabulated in Table 3.1 for various $VDDL$ with 1.0 as V_H and using the 32nm predictive technology model [2]. It can be seen from Table 3.1 that as the input voltage is scaled down the power consumption goes down, but as the input voltage reaches near the threshold voltage, the power consumption starts to increase. The delay of the level converter also increases as we scale down the voltage as expected.

3.2.2 Pass Transistor Logic

Figure 3.7 shows a level converter described in [16, 22, 23] which is based on a weak feedback pull-up device (M4) and an NMOS pass gate (M1). The purpose of the pass gate device is to isolate the input of the PMOS M3 from the previous logic stage. The feedback device M4 can then pullup the internal node without consequence to the prior logic that is running at $VDDL$. This level converter consumes less energy than the DCVS level converter due to its fewer devices and reduced contention. The results are shown in Table 3.2. From Table 3.2 power consumption and delay of pass transistor is less when compared with

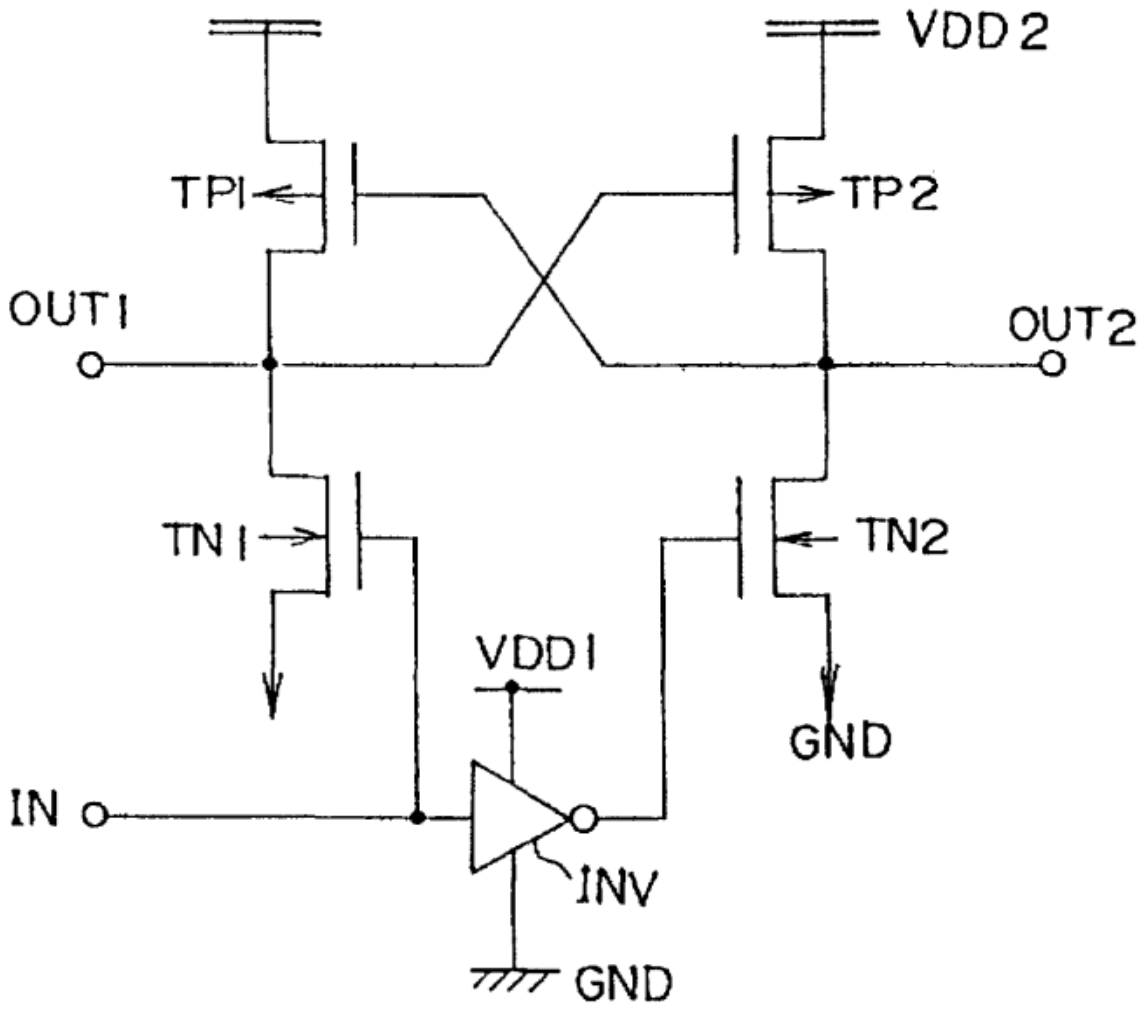

Figure 3.6: Standard level converter or dual cascaded voltage system.

standard level converter is less. The rise time of pass transistor is high when the voltage is scaled down.

3.2.3 Conventional Type II Level Converter

Another conventional low to high level-shifter is depicted in Figure 3.8 [21, 50]. Unlike the cross-coupled level-shifter, the current driving capabilities for M3 and M4 are decided by gate source voltage (Vgs of M3) regardless of VDD voltage level, and the saturation current of M1 determines Vgs of M3. The current driving abilities of M3 and M4 are not affected

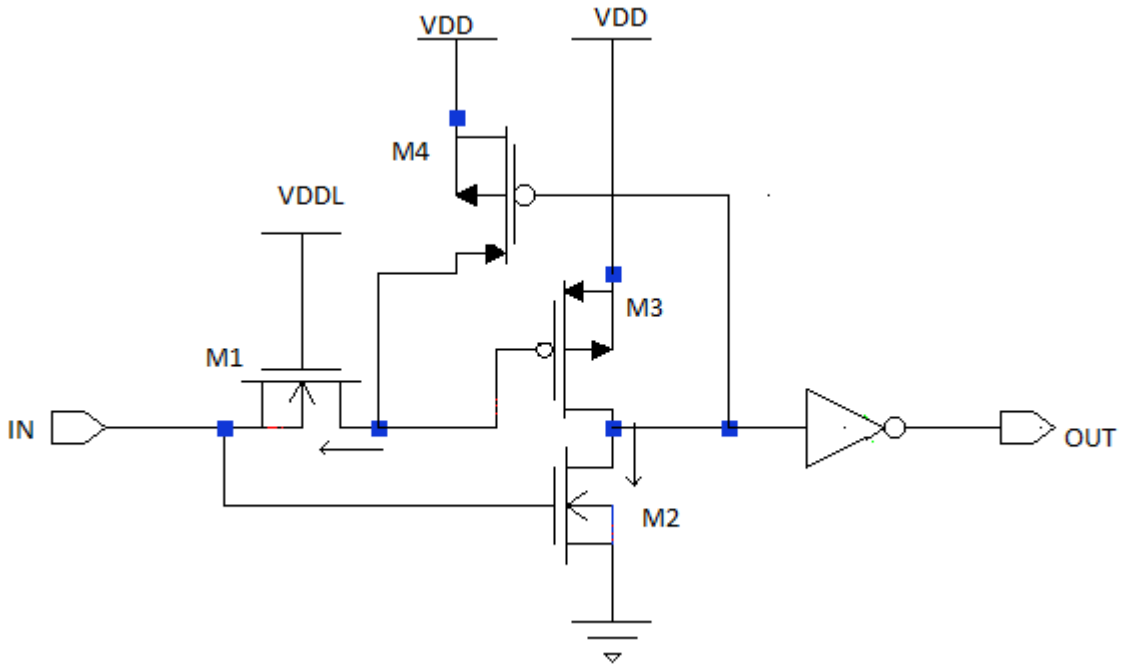

Figure 3.7: Pass transistor logic.

Table 3.2: Pass transistor logic, $V_H = 1.0$V.

Input voltage V_L volt	Average power μW	Rise delay ps	Fall delay ps
1.0	0.639	5.14	20.3
0.9	0.641	7.48	19.8
0.8	0.646	10.41	16.6
0.7	0.664	14.2	23.9
0.6	0.709	20.2	25.2
0.5	1.22	28.2	39.47
0.4	3.99	51.34	38.45

by I/O voltage (VDD) but depend on M3 and M4 threshold voltages, resulting in a stable current driving capability. The results are tabulated in Table 3.3. As seen from Table 3.3 the power consumption of the level converter is high when compared with standard level converter but the delay is low. The power consumption of the level converter is high because of the stacked PMOS transistors.

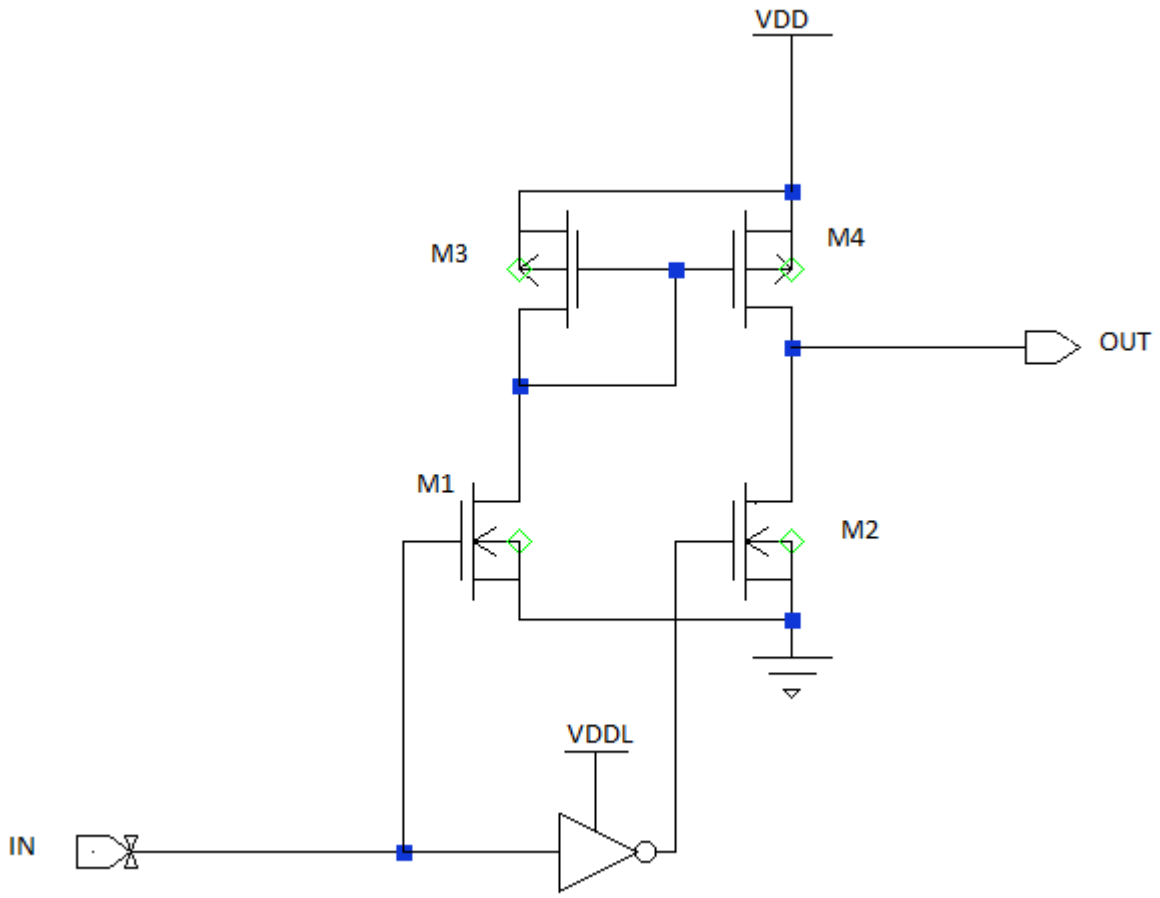

Figure 3.8: Conventional Type II level converter.

Table 3.3: Conventional Type II level converter, $V_H = 1.0$V.

Input voltage V_L volt	Average power μW	Rise delay ps	Fall delay ps
1.0	32.6	2.8	10.7
0.9	31.7	3.32	15.84
0.8	30.78	13.5	17.9
0.7	28.77	18.33	22.22
0.6	24.7	25.93	29.46
0.5	19.06	28.36	46.7
0.4	12.9	34.89	85.68

3.2.4 Contention Mitigated Level Shifter

Figure 3.9 shows the contention mitigated level shifter (CMLS) [13, 25, 44]. In the CMLS, the above-mentioned contention is reduced, since M1 and M3 (M2 and M4) comprise

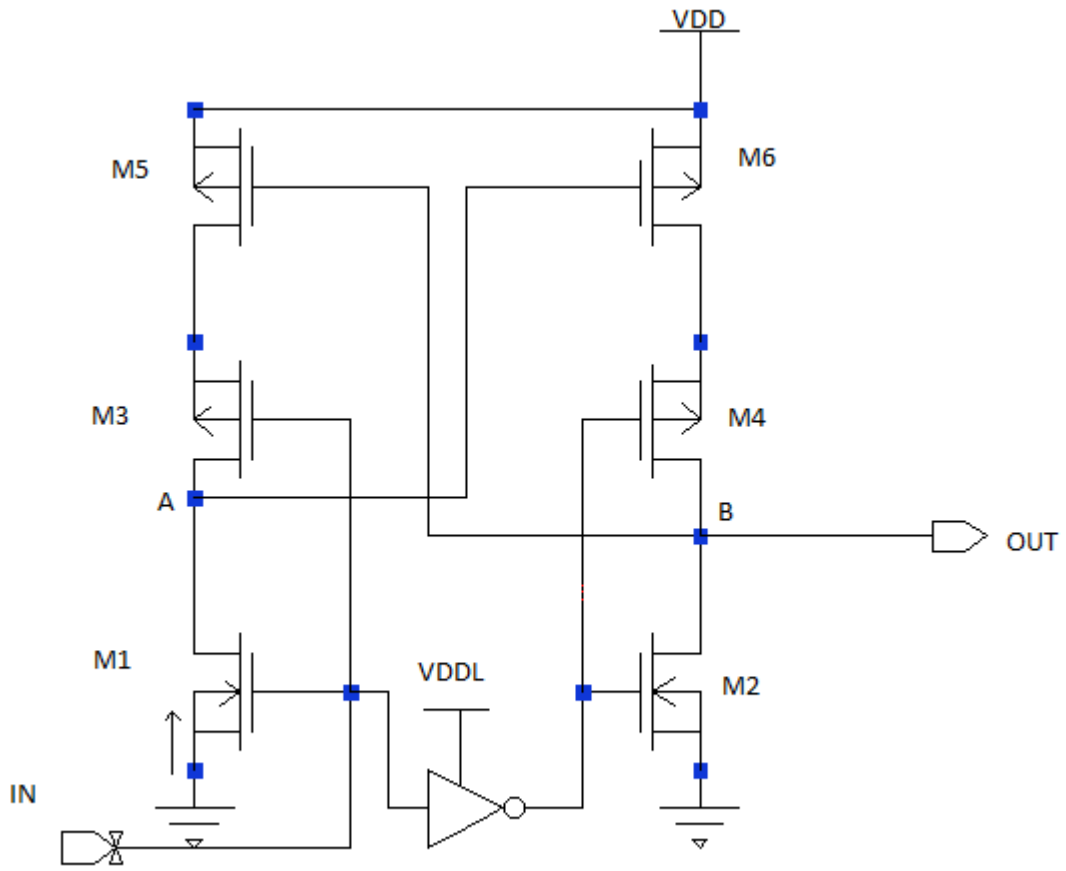

Figure 3.9: Contention mitigated level shifter (CMLS).

a quasi-inverter. Therefore the logical values of node A and B are established faster than that of the conventional level shifter. Thus the delay of CMLS is less than that of the conventional level shifter. The power consumption of the CMLS is reduced compared with that of the conventional level shifter, because the contention reduction also brings in the crowbar current reduction. The results are shown in Table 3.4. Table 3.4 shows that the power consumption in contention mitigated level shifter is less than the conventional type II converter as the input voltage is scaled down.

3.2.5 Dual-v_{th} Cascaded Inverter Level Converter

Unlike the previously published level converters that rely on feedback, this level converter employs a multi-V_{th} CMOS technology in order to eliminate the static DC current.

Table 3.4: Contention mitigated level shifter (CMLS), $V_H = 1.0$V.

Input voltage V_L volt	Average power μW	Rise delay ps	Fall delay ps
1.0	1.13	9.83	14.79
0.9	0.95	10.4	12.97
0.8	0.845	12.11	19.13
0.7	0.797	15.5	23.1
0.6	0.778	20.08	31.55
0.5	0.771	26.07	53.42
0.4	0.837	34.7	191.7

The pull-up network transistors in the new level converters are directly driven by the low-swing signals without producing a static DC current problem. The level converter [42] is shown in Figure 3.10 and is composed of two dual-v_{th} cascaded inverters. The threshold voltage (v_{th}) of M2 is high for avoiding static DC current in the first inverter when the input is at $VDDL$. Vth-M2 is required to be less than $VDDL - VDDH$ for eliminating the static DC current. In the figure, the thick line indicates high V_{th}. When the input is 0V, M2 is turned on. M1 is cut-off. Node 1 is pulled up to $VDDH$. The output is discharged to 0V. When the input transitions to $VDDL$, M1 is turned on. M2 is turned off since V_{GS}-M2 > V_{th}-M2. Node 1 is discharged to 0V. The output is charged to $VDDH$. The results are shown in Table 3.5. From Table 3.5 we can see that as the input voltage is scaled the power consumption is high than our target(standard inverter). The power consumption for the range (0.7V-0.4V) is high from 0.866V to 5.01V.

Table 3.5: Dual-V_{th} cascaded inverter level converter, $V_H = 1.0$V.

Input voltage V_L volt	Average power μW	Rise delay ps	Fall delay ps
1.0	0.735	0.2	18.34
0.9	0.719	2.44	19.13
0.8	0.732	5.00	17.51
0.7	0.866	8.62	15.23
0.6	1.08	12.77	10.90
0.5	2.32	18.02	2.82
0.4	5.01	25.07	1.5

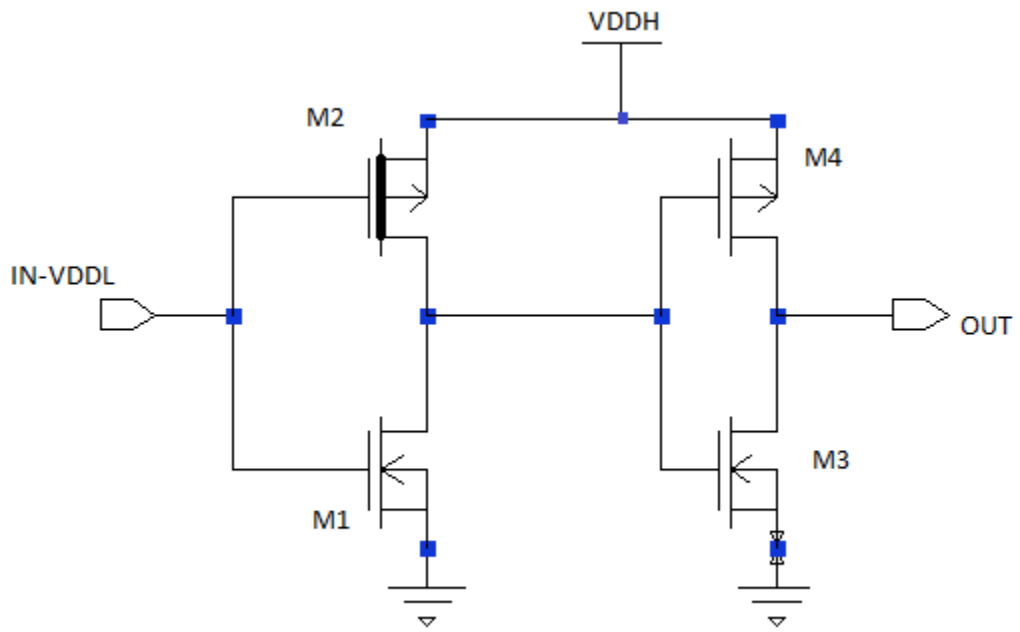

Figure 3.10: Dual-v_{th} cascaded inverter level converter. Thick line indicates high V_{th}.

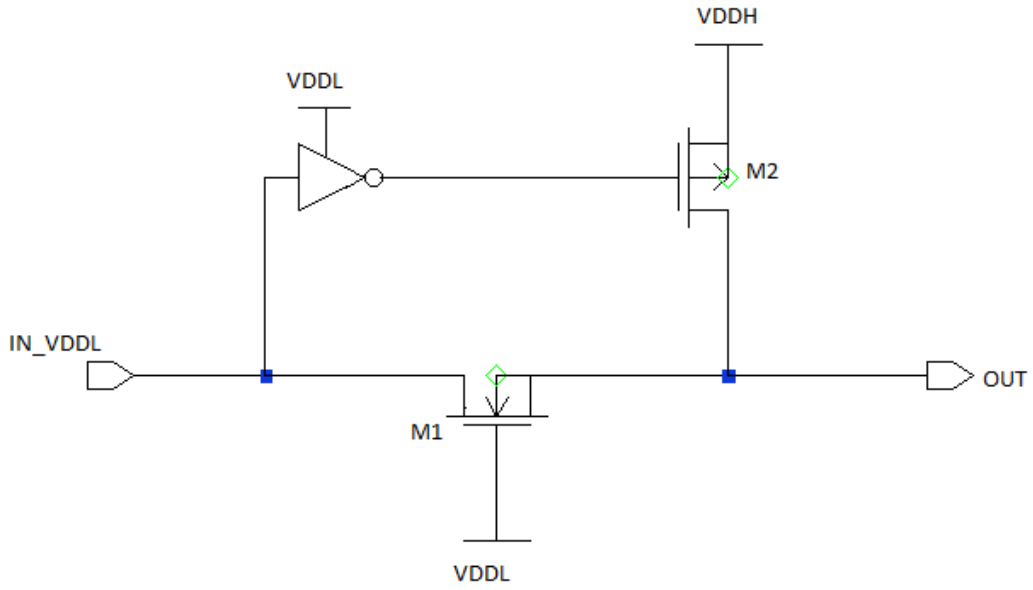

Figure 3.11: Multi-V_{th} level converter (a recently published level converter). Thicker line indicates high V_{th} device.

3.2.6 Multi-V_{th} Level Converter (A Recently Published Level Converter)

Figure 3.11 shows a recently published multi-V_{th} level converter. In this converter [36] the inverter is supplied with $VDDL$. The NMOS transistor (M1) gate is supplied by $VDDL$

and the PMOS (M2) gate is connected to the inverter output, with the source connected to VDDH. When there is a $VDDL$ at the IN, then the inverter turns on, producing a '0' at the gate of M2, which turns M2 ON, giving an output of '1'. When there is a logic '0' at the input, the output of the inverter is '1' turning the PMOS M2 off and the output has a '0' because of M1. In this design we use multi-Vth CMOS technology in order to eliminate the static DC current. The results are given in Table 3.6. The power consumption is reduced in Multi-V_{th} level converter than the Dual-V_{th} cascaded inverter level converter as seen from Table 3.6. As seen from Table 3.6 we can see that the transistor reduction has caused the power reduction in Multi-V_{th} level converter, as the input voltage is scaled down the power consumption increases.

Table 3.6: Multi-V_{th} level converter (recently published), $V_H = 1.0$V.

Input voltage V_L volt	Average power μW	Rise delay ps	Fall delay ps
1.0	0.225	1.558	11.80
0.9	0.162	5.88	6.59
0.8	0.171	7.41	6.77
0.7	0.332	13.40	14.37
0.6	0.403	15.77	12.9
0.5	1.89	17.20	17.98
0.4	4.73	17.07	28.6

The level converters are compared with a standard inverter in Figures 3.12 and 3.13. From Figure 3.12 we can see that the multi-V_{th} level converter has the lowest in terms of power consumption (in the range of 0.6V - 1.0V) and from Figure 3.13, It can be seen that the multi-V_{th} level converter has the lowest delay. Multi-V_{th} level converter has less power consumption than the target for some of the input voltage values , but delay is more than a inverter for most of the input voltage values. Based on the results, the multi-V_{th} level converter was selected to compare with the proposed level converter in the next chapter.

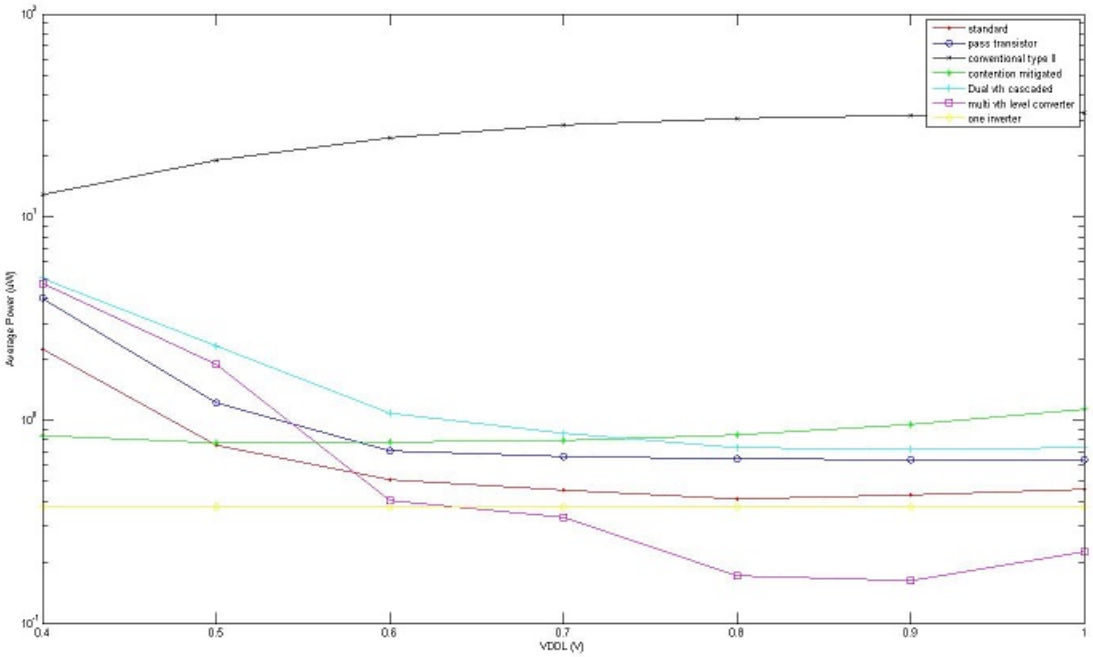

Figure 3.12: Power consumption (μW) against $VDDL$ (V).

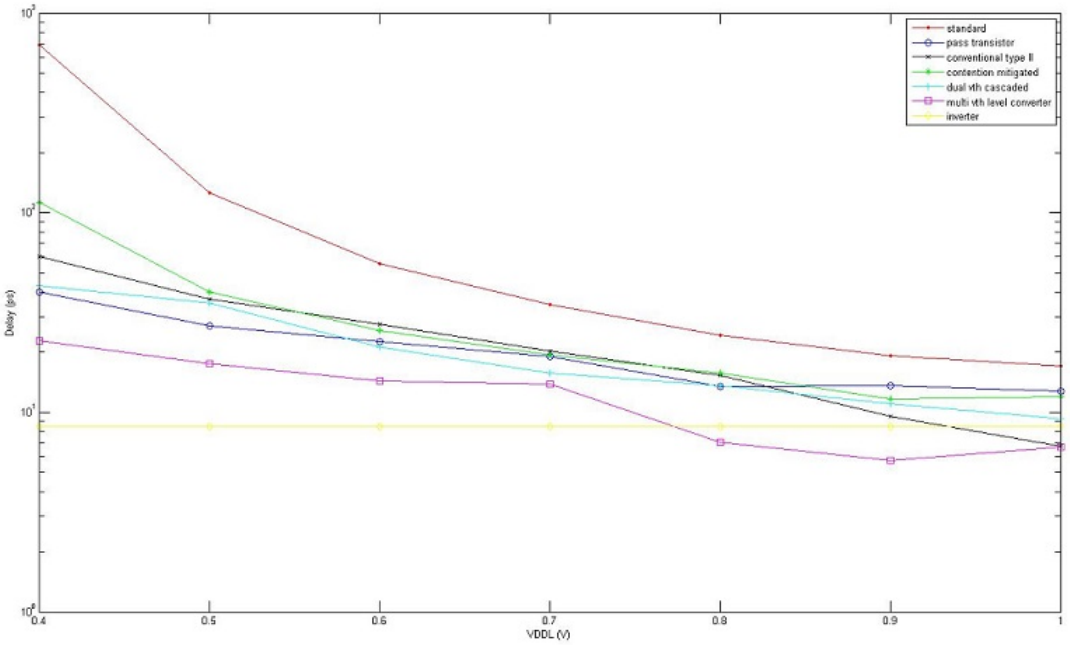

Figure 3.13: Delay versus $VDDL$ for level converters.

Chapter 4

DVF4: A Dual-V_{th} Feedback Type 4-Transistor Level Converter

The proposed level converter will be discussed in this chapter in detail. This level converter will also be compared with the multi-V_{th} level converter, as it is lowest both in terms of power consumption and delay as discussed in Chapter 3. The level converter is based on a feedback pull-up device [12]. Feedback-based level converters suffer from a delay penalty. Inorder to overcome the delay penalty we use multi-V_{th} to reduce the delay when compared with other level converters.

4.1 DVF4: A Dual-V_{th} Feedback Type 4-Transistor Level Converter

The proposed level converter is shown in Figure 4.1. The level converter consists of an NMOS pass gate M1. The pass gate is used to allow a logic '0' to be passed from input to output as NMOS is a perfect switch for a '0'. The pass gate is supplied with VDDL on the gate of the transistor, so M1 is always ON. The gate of NMOS transistor M2 is connected to the input and the drain is connected to the gate of PMOS transistor M3 (high V_{th}). The source of M3 is connected to the VDD, and the drain is connected to the output. The output is also connected to the gate of PMOS transistor M4 (High V_{th}), the drain of M4 is connected to the drain of the M2, the source of M4, and is connected to VDD. We use M4 to restore the drain of M2 to logic '0' if the previous state is VDD.

When there is $VDDL$ on the input, M2 is ON forcing the drain of M2 to be '0'. This turns M3 ON, the output node goes to High (Logic '1'). A logic '1' on the output keeps M4 OFF making no change to the gate of M3. Therefore we have a stable '1' at the output. Now, when we have a logic '0' at the input of the level converter, the '0' is passed by the M1, since M1 is always ON. A '0' at the output turns M4 ON, keeping the gate of M3 at

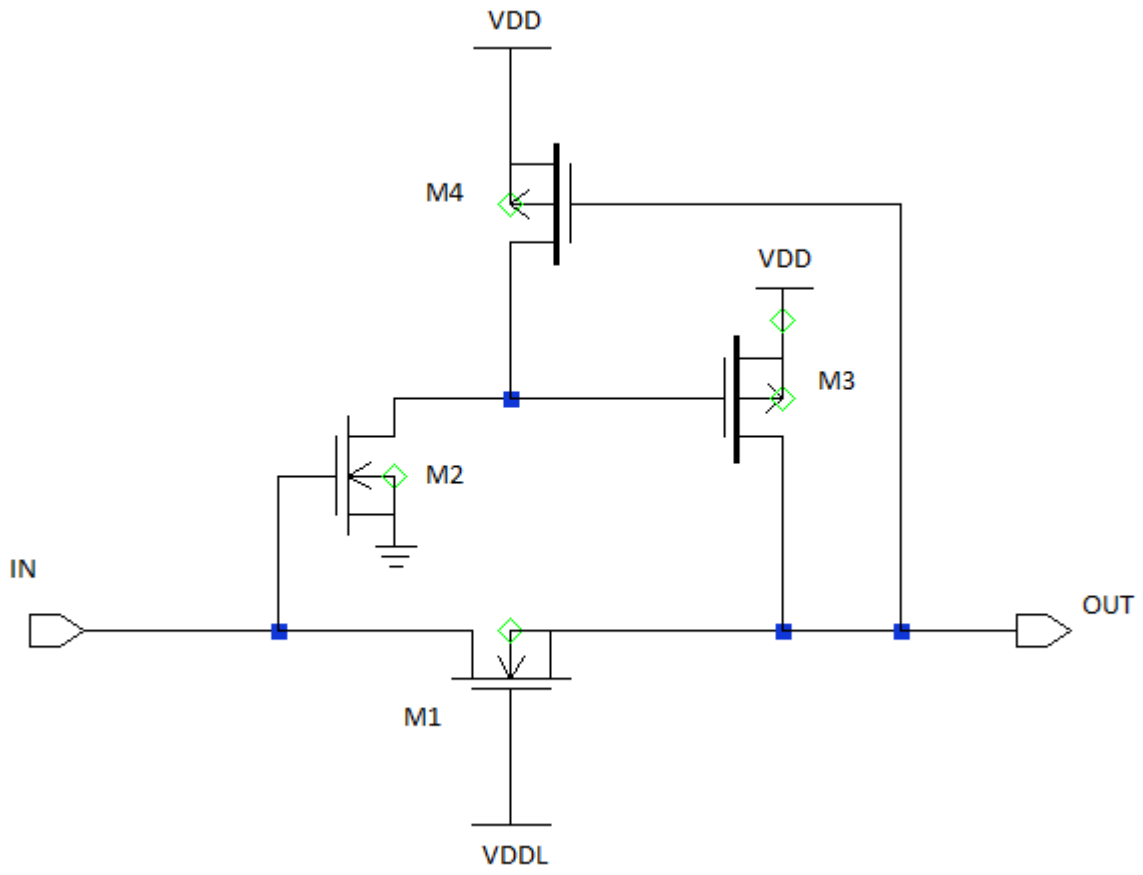

Figure 4.1: DVF4: Dual-V_{th} feedback type 4-transistor level converter. Thicker lines on transistor denote high V_{th} devices.

'1', so that M3 is OFF, providing a proper '0' at the input. If M4 is absent, then the gate of M3 will be at an intermediate voltage caused by the leakage from VDD by the previous logic state, so we will not have a proper '0' at the output.

The level converter is optimized using an optimizing program written in PERL for power consumption and delay, by changing the widths of transistors M3 and M4, and the threshold voltages of M3 and M4 individually for each $VDDL$. After the optimization the width of the M4 transistor was found to be approximately constant at 0.110μ. The simulation setup is the same as done for the level converters discussed in Chapter 3. The results for various $VDDL$ are tabulated, along with the optimized width of the transistor for M3 and V_{th} of M3 of the level converter, in Table 4.1. As seen from Table 4.1, when the input voltage is scaled down

Table 4.1: DVF4: Dual-V_{th} feedback type 4-transistor level converter, V_H = 1.0V.

Input voltage V_L	M3 width μ	M3 V_{thp} V	Average power μW	Rise delay ps	Fall delay ps
1.0	0.120	-0.715	0.170	0.41	6.2
0.9	0.120	-0.715	0.133	3.12	7.33
0.8	0.120	-0.710	0.135	5.1	8.21
0.7	0.106	-0.715	0.187	11.6	9.91
0.6	0.118	-0.68	0.229	14.30	11.92
0.5	0.116	-0.72	0.585	17.7	14.3
0.4	0.120	-0.69	1.80	35.9	23.61

close to threshold voltage the power consumption reduces in range of (1.0V-0.8V), and then increases, when the voltage is scaled down further than the threshold voltage (0.7V-0.4V).

4.2 Comparison of DVF4 Level Converter and the Multi-V_{th} Level Converter

We compared DVF4 level converter with the multi-V_{th} level converter. The simulation setup is same as we discussed in Chapter 3. The results are tabulated in Table 4.2. From Table 4.2, It can be see that the power consumption of DVF4 is comparatively lower as we scale down the input voltage. A maximum saving of 57.66% is observed with respect to power consumption of the whole circuit than the power consumption of the multi-V_{th} level converter. The delay saving for 0.4V could not be made because the multi-V_{th} level converter failed at 0.4V. The power consumption and delay of the level converters are shown in Figures 4.2 and 4.3. DVF4 performs better than multi-V_{th} level converter in all input voltage as it can be inferred from Figure 4.2. Figure 4.3 shows that DVF4 performs better when compared with multi-V_{th} level converter for most of the input voltage except for 0.4V.

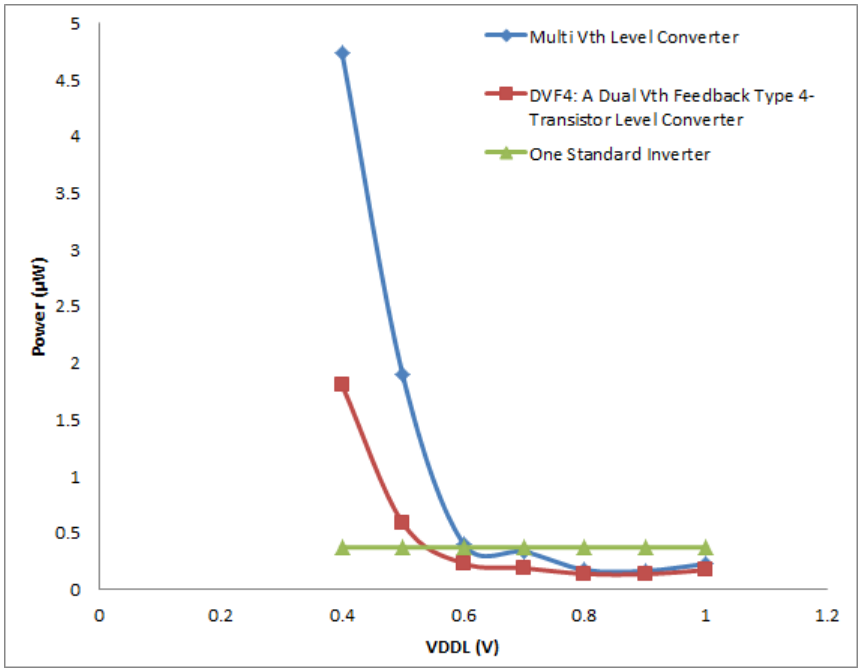

Figure 4.2: Comparison of power consumption of DVF4 level converter against multi-V_{th} level converter.

4.3 Simulation setup for comparison of level converter with two cascaded inverters

To demonstrate the advantages of the DVF4 level converter, a HSPICE simulation is set-up as shown in the Figure 4.4, where the size of the driver and load inverters are 4X the size of a minimum size inverter (Wn = 4Wmin and Wp = 10Wmin [42]). The technology used for the simulation is 32nm with 0V for logic 0 and V_H for logic 1, which is 1.0V. The

Table 4.2: Comparing DVF4 level converter with the multi-V_{th} level converter.

Input voltage V_L	DVF4 level converter		Multi-V_{th} level converter		Power saving %	Delay reduction %
	Power μW	Delay ps	Power μW	Delay ps		
1.0	0.170	3.305	0.225	6.679	24.3	50.51
0.9	0.133	5.225	0.162	6.735	17.44	22.4
0.8	0.135	6.655	0.171	7.09	20.94	21.6
0.7	0.187	10.75	0.332	13.885	43.52	22.57
0.6	0.229	13.11	0.403	14.335	43.08	8.5
0.5	0.585	16.0	1.89	17.59	53.4	-9.09
0.4	1.80	34.75	4.73	22.835	57.66	-34.28

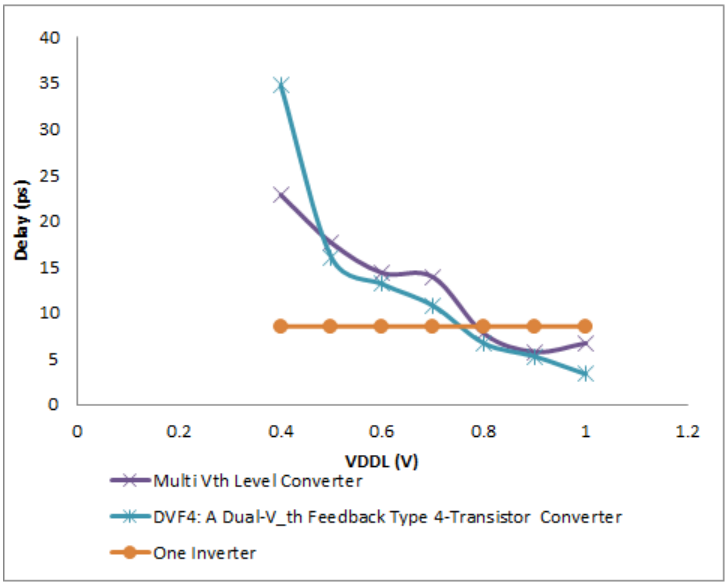

Figure 4.3: Comparison of delay of DVF4 level converter against multi-V_{th} level converter.

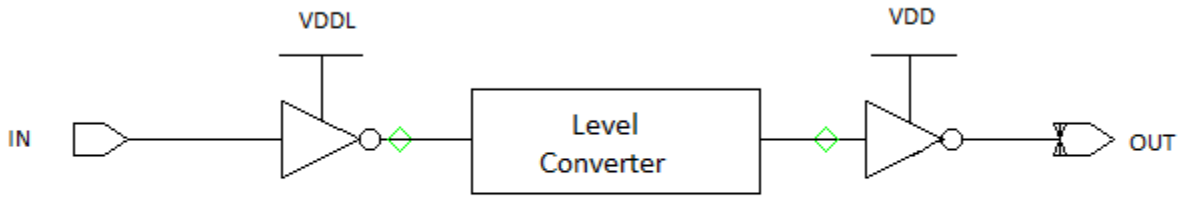

Figure 4.4: Simulation setup for demonstrate the advantage of the proposed design.

simulation is done for 10 cycles. The power consumption and delay values of both the DVF4 level converter and multi-V_{th} level converter are given in Table 4.3. From Table 4.3 it can be seen that the power consumption is reduced when simuated using DVF4, the maximum reduction in this case is about 77% and the maximum delay reduction is 52.4% . The power and delay values are shown in Figures 4.5 and 4.6. In both the figures 4.5 and 4.6 we can see that the power consumption is considerably low than multi-V_{th} level converter and the delay is comparatively lower than the multi-V_{th} level converter.

Table 4.3: Comparing DVF4 level converter with the multi-V_{th} level converter using cascaded inverters.

Input voltage V_L	DVF4 level converter		Multi-v_{th} level converter		Power saving %	Delay reduction %
	Power μW	Delay ps	Power μW	Delay ps		
1.0	2.90	28	4.23	26	31.44	-7.69
0.9	2.20	35	3.48	38	36.7	8.5
0.8	1.71	33	3.10	50.32	44.83	52.4
0.7	1.47	48.8	2.92	62.6	49.65	28.27
0.6	1.435	72	2.90	82.2	50.5	14
0.5	1.54	113	3.62	104	57.4	-8
0.4	2.03	252	8.66	159	76.55	-58.4

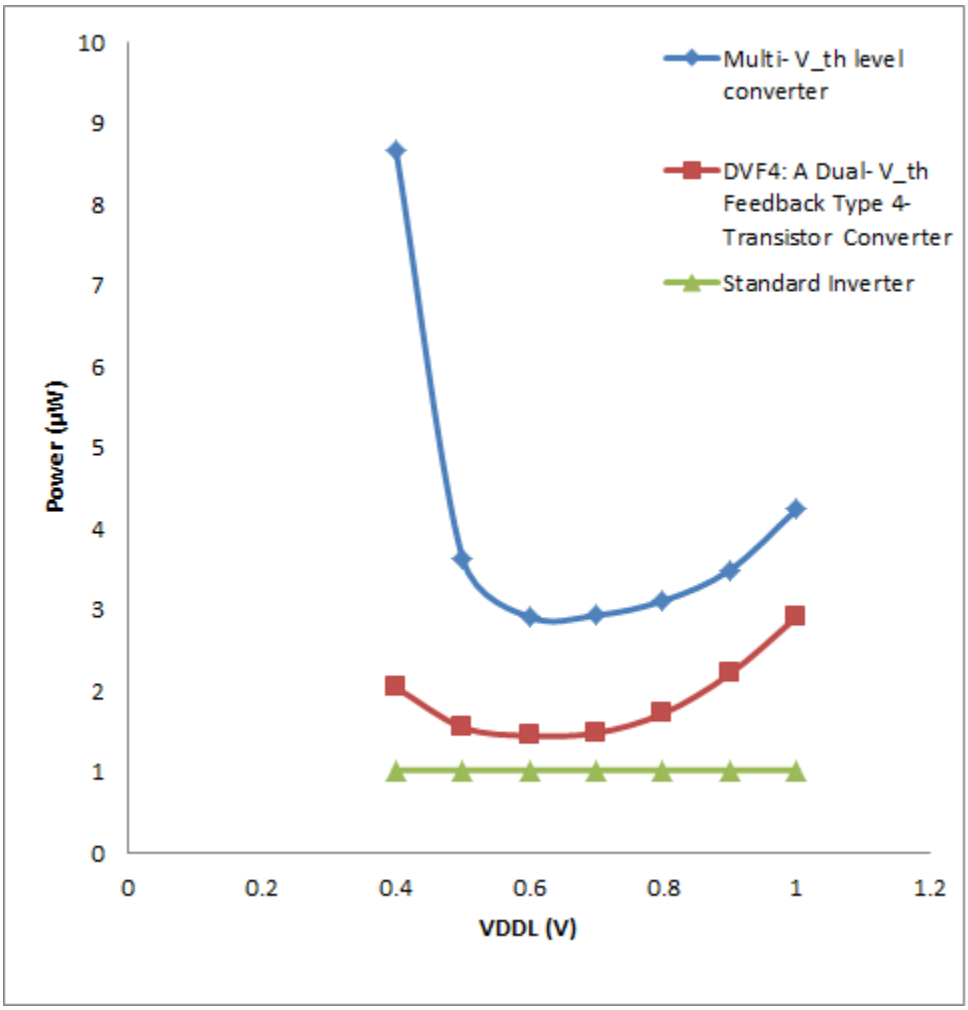

Figure 4.5: Comparison of power consumption of level converters using cascaded inverters.

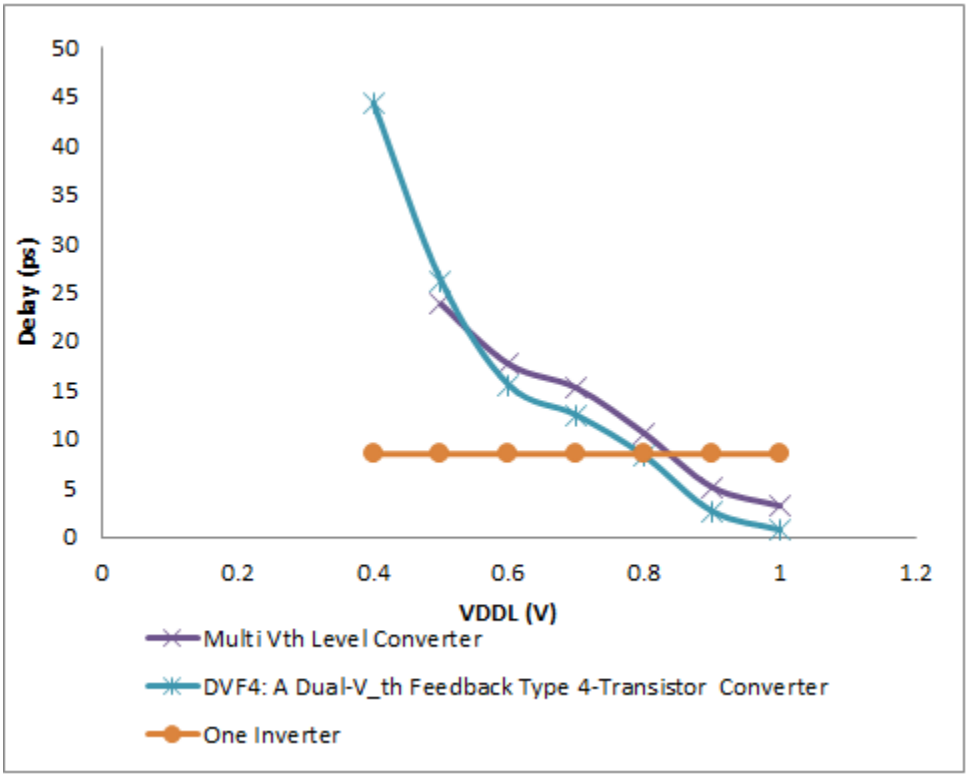

Figure 4.6: Delay comparison of level converters using cascaded inverters.

4.4 Comparison of number transistors in level converters discussed

In this section the numbers of transistors used in the level converters are compared to get an area overhead. We calculated the area of each level converter by getting the product of width and the length of transistor and adding the number of transistors and the approximate area of the buffered capacitance connected at the outputs of the level converters. The area of the level converters and capacitance area is calculated as described in[24]. Table 4.4 shows the results of the number of transistors and the area of the level converters, calculated as mentioned. From Table 4.4, we can see that as the number of transistors are reduced the area of the transistors are also reduced. As indicated, contention mitigated level converter has 8 transistors the area is increased.

Table 4.4: comparison of number transistors in level converters

Level Converter	Number of transistors	Area overhead μm^2
Standard	6	0.521
Pass Transistor	6	0.521
Conventional TypeII	6	0.521
Contention Mitigated	8	0.530
cascaded Inverter	4	0.5143
Multi-V_{th}	4	0.5143
DVF4	4	0.5124

4.5 A Slack-Based Algorithm for Dual Voltage Assignment Using Level Converters

An algorithm is described to assign lower supply voltage without any constraints imposed on the circuit topology. This method is called *Enhanced Clustered Voltage Scaling* (ECVS) [46]. This algorithm removes the condition that requires only high voltage gates feeding the low voltage gates and allows the low voltage gate to feed the high voltage gate with an asynchronous level converter (ALC) [24] in between to shift the logic level from low to high. This allows more gates to be assigned a lower voltage and higher energy savings are expected. However, the level shifters added at low-voltage gate to high-voltage gate junctions contribute to additional energy consumption, which needs to be taken into account while calculating the final energy savings. The terms "level shifters" and "level converters" are used interchangeably. An additional delay penalty is also associated with these level converters. Thus, fast and low power level converters are important in mitigating these penalties.

In both CVS and ECVS algorithms, described in [12, 47], we start with all gates at high voltage and then assign the lower power supply to gates by traversing the circuit from the primary outputs to the primary inputs in a levelized order. However, since ECVS performs this assignment simply by visiting gates one at a time in a reverse levelized manner, it still

Table 4.5: Optimal lower supply voltage (V_L) and energy saving using Algorithms 2 and 4 [4] for ISCAS'85 benchmark circuits using DVF4: A dual-V_{th} feedback type 4-transistor level converter. $V_H = 1.0$V.

Circuit	Algorithm 2, see [4] V_L V	Total gates	Algorithm 4 ([4]) Gates in low voltage	Number of level shifters	Energy calculated by Spice $E_{singleVDD}$ fJ	E_{Dual} with proposed Level converters fJ	$E_{savg.-obs.}$ %	$E_{savg.-obs.}$ Dual-VDD Algorithm 3 see [4] %
C432	0.80	154	73	44	161.3	145.4	9.85	3.66
C499	0.91	493	247	101	463	396.9	20.1	7.8
C880	0.58	360	203	78	277.6	106.1	61.77	58.29
C1355	0.92	469	101	119	455.2	421.2	7.4	4.86
C1908	0.77	584	380	138	496.5	352.1	29.08	23.81
C3540	0.61	1270	881	232	1843	1437	22.02	12.23
C6288	0.73	2407	1183	98	1932	1855	3.98	3.26

assigns supply voltages in a fundamentally constrained manner [24]. Noting this drawback, we do not use levelization in our algorithm for voltage assignment. Our algorithm is related to the existing ECVS approach in that it allows the use of asynchronous level converters.

The simulation setup is described as follows. For each benchmark circuit, Algorithm 2, as specified in Allani [4], is used to find the gate slacks and the optimum voltage. Energy savings of benchmark circuits using Dual-VDD without using level converters, is found using the Algorithm 3 as described in Chapter 5 in [4]. The motive is to have more energy savings when using the level converters. Now, allowing level converters we find the energy savings of benchmark circuits by using Algorithm 4, as described in [4, 5]. These benchmark circuits are synthesized using a small set of 90nm predictive technology [2] standard cells consisting of an inverter, INV, a two-input NAND gate, NAND2, a three-input NAND gate, NAND3, and a two-input NOR gate NOR2. Each circuit is simulated with a logic simulator with randomly generated input vectors to determine the circuit's average activity.

Table 4.5 shows the results comparing the energy savings for various benchmark circuits when level converters are used in dual-VDD design against the savings when the DVF4 level converter is used. From Table 4.5, we can find that by allowing the level converter overhead,

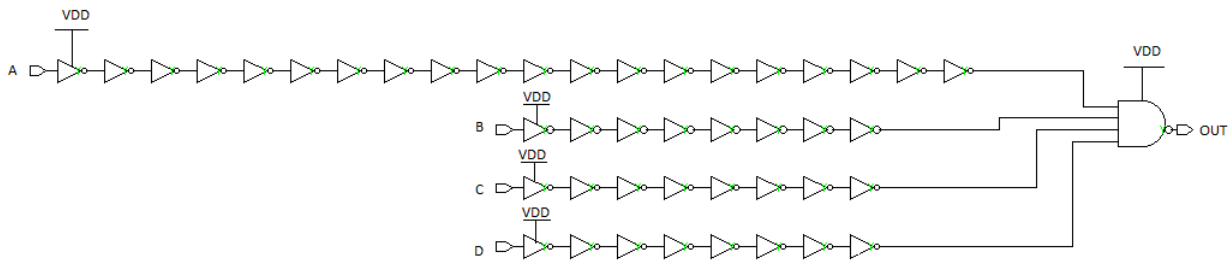

Figure 4.7: A single VDD inverter tree.

the energy savings we obtained is comparatively greater than the energy savings obtained using Dual-VDD design, where level converters were not used.

4.6 Inverter Tree Combination Setup

In order to determine whether the level converter can be used to reduce the power consumption in the case of Dual-VDD design and still maintain the critical delay of the circuit, we utilize the inverter tree circuit. We can determine how many gates can be assigned $VDDL$ and find the optimum low voltage (V_L) at which the critical path delay can be maintained and still save power consumption. We then compare our DVF4 level converter with the Multi-v_{th} level converter. In order to determine the critical delay, an inverter tree is first simulated with VDD. This inverter tree is shown in Figure 4.7.

The Inverter tree circuit is supplied with VDD. The path from input A to OUT determines the critical path. The power consumption with VDD as the supply is found. Our objective is to power some of the gates in non-critical paths with $VDDL$, without exceeding the critical path delay, and thus reduce the power consumption of the inverter tree. Now, for the simulation purpose, the three shorter chains are supplied with $VDDL$ and then we use DVF4 level converter to shift the level to proper high logic '1'. The number of $VDDL$ gates to be used is determined by the original critical delay. The gates connected to the output of a level converter are supplied with VDD. The output NAND gate is always supplied with VDD. The optimum voltage $VDDL$ supplied for the inverter tree is found

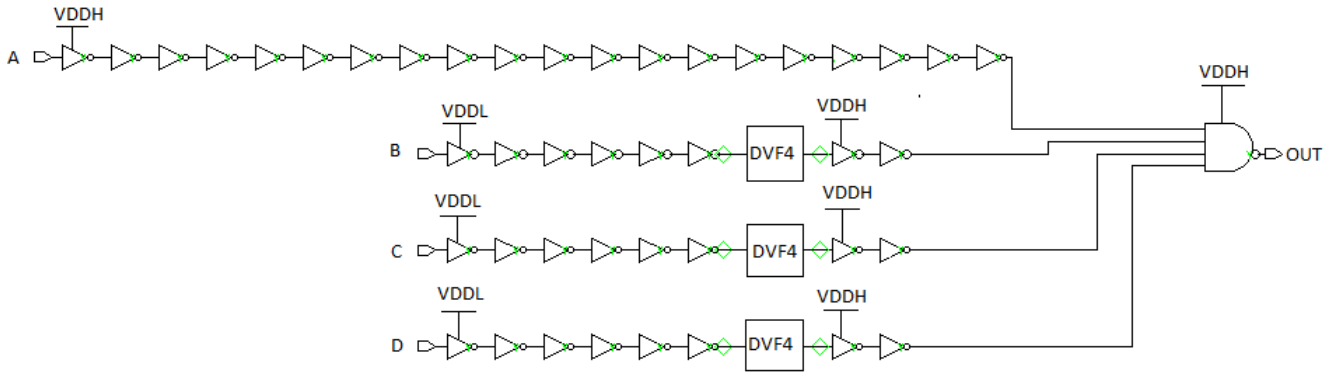

Figure 4.8: Inverter tree with DVF4 level converter.

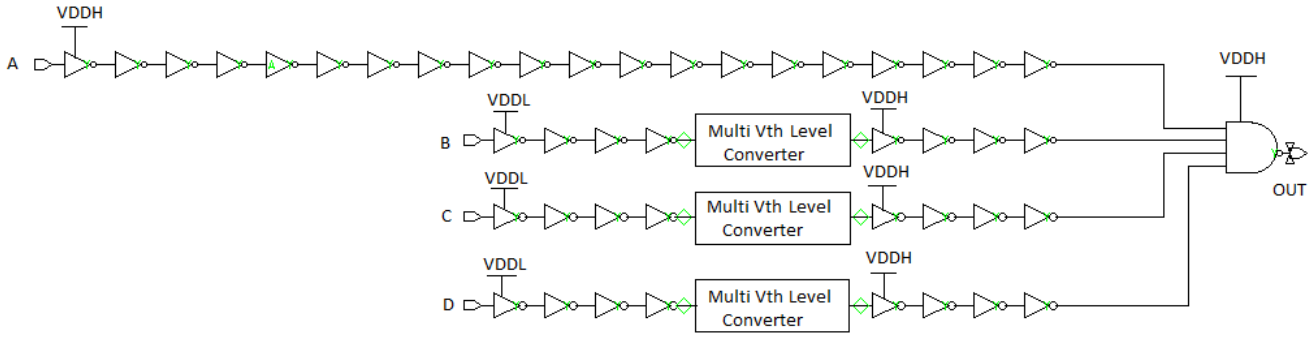

Figure 4.9: Inverter tree with multi-V_{th} level converter.

from algorithm 2[4]. The inverter tree is simulated for 100 cycles of toggling inputs with 100 vectors with critical delay as the period for each input vector. The simulations are done using 32nm predictive technology model [2]. The inverter tree simulation model using the DVF4 level converter is shown in Figure 4.8.

As shown in the Figure 4.8, each shorter path has six $VDDL$ gates and two gates supplied by $VDDH$. The optimum voltage $VDDL$ and the number of $VDDL$ gates must not allow the shorter path delays to exceed the critical delay of the long path and yet allow the maximum energy saving. The simulation is repeated with the Multi-v_{th} level converter and results are compared with the power savings obtained with the DVF4 level converter. The simulation setup remains the same in the two cases. Figure 4.9 shows the simulation model with multi-V_{th} level converter. To maintain the critical delay, the shorter chains are supplied with $VDDL$ and there are four $VDDL$ gates connected to multi- V_{th} level converter,

Table 4.6: Inverter chain example comparison of multi-V_{th} *previous best* level converter (LC) and DVF4: A dual-V_{th} feedback type 4-transistor level converter (LC) (proposed in this work), $VDDH = 1.0$V.

Single voltage $VDD = 1.0$V		Dual-voltage, $VDD = 1.0$V							
		With proposed LC				With previous best LC			
Power μW	Delay ps	$VDDL$ V_L	Power μW	Delay ps	% Power reduction	$VDDL$ V_L	Power μW	Delay ps	% Power reduction
4.53	132.1	0.7	2.13	132.1	51.8	0.8	3.59	132.1	22.39

with four gates supplied with VDD. The outputs of the inverter-chain are connected a nand gate which is supplied by VDD. The results are given in Table 4.6. We can see from the Table 4.6 that the power reduction with respect to the DVF4 level converter is 51.8%, and with the multi- V_{th} level converter the power savings are only 22.39%, we can also see that there are more $VDDL$ gates used when simulated with the DVF4 level converter which causes the power reduction. We are constrained with number of $VDDL$ gates because we have to maintain the critical delay.

4.7 Conclusion

From the Tables 4.1, 4.2, 4.3, 4.4, 4.5 and 4.6 we find that the Dual-V_{th} feedback-based level converter (LC) proposed in this work performs better both in terms of power consumption and delay when compared with the multi-V_{th} LC that is the best available in the existing state of the art.

Chapter 5

Conclusion

In this work a level converter based on a Dual-V_{th} feedback-based level converter was discussed. The existing level converters, ranging from conventional level converters to the recently published level converters, were analyzed. DVF4 level converter was compared to the multi-V_{th} level converter (best existing level converter) using various simulation setups and the results were obtained for different voltage supplies for multi-VDD systems. The circuits were optimized and simulated at 32nm CMOS technology. DVF4 level converter offers us a significant savings on power consumption of up to 76% and delay savings up to 52%. This level converter could be used and can produce lower power consumption in spite of the overhead, based on the data obtained from the simulations as discussed in this work.

"We cannot solve a problem with the same thinking we used when we created them"

- Albert Einstein.

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