Total Power Minimization in Glitch-Free CMOS Circuits Considering Process Variation

Abstract

Compared to subthreshold leakage, dynamic power is normally much less sensitive to the process variation due to its approximately linear relation to the process parameters. However, the average dynamic power of a circuit optimized by a deterministic path balancing approach increases because the filtered glitches randomly start reappearing under the influence of process variation. Combining several existing techniques, we propose a new statistical mixed integer linear programming (MILP) formulation, which uses path balancing and dual-threshold techniques to statistically minimize the total power in glitch-free circuits considering process variation.

1. Introduction

With the continuous increase of the density and performance of integrated circuits due to the scaling down of the CMOS technology, reducing power dissipation becomes a serious problem that every circuit designer has to face. At the same time, the increase in variability of several key process parameters can significantly affect the design and optimization of low power circuits in the nanometer regime [1].

Due to the exponential relation of leakage current with some process parameters, such as the effective gate length, oxide thickness and doping concentration, process variations can cause a significant increase in the leakage current. To minimize the effect of process variation, some techniques [2-4] statistically optimize the leakage power and circuit performance by dual-V_{th} assignment. Leakage current and delay are treated as random variables. A dynamic programming approach for leakage optimization by dual-V_{th} assignment has been proposed [2] using two pruning criteria that stochastically identify pareto-optimal solutions and prune the sub-optimal ones. Another approach [4] solves the statistical leakage minimization problem using a theoretically rigorous formulation for dual-V_{th} assignment and gate sizing.

Glitches as unnecessary signal transitions account for 20%-70% of the dynamic switching power [5]. To eliminate glitches, a designer can adopt techniques of hazard filtering [6, 8-11] and path balancing [7, 9, 12]. Compared to leakage power, dynamic power is normally much less sensitive to the process variation because of its approximately linear dependency on the process parameters. However, any deterministic path balancing technique used for eliminating glitches becomes less effective under process variation, since the perfect hazard filtering conditions can be easily corrupted even with a small variation in some process parameters. Hu and Agrawal [13-14] proposed a technique to eliminate glitches under process variation. However, performance has to be sacrificed to obtain a process-variation-resistant circuit, and the process variation on leakage power is not considered.

Our work is motivated by the above research. To minimize the leakage power, we use an MILP model to determine the optimal assignment of V_{th} while controlling any sacrifice in performance. To eliminate the glitch power, additional MILP constraints determine the positions and values of the delay elements to be inserted to balance path delays. Statistical delay and leakage models are further adopted to reduce the total power in glitch-free circuits considering process variation.

2. Background

Lu and Agrawal [17] propose a statistical MILP formulation to minimize the impact of process variation on the subthreshold leakage. In this section, we further discuss the impact of process variation on dynamic power in detail.

Dynamic power comprises two parts, logic switching power and glitch power, which can be expressed by the following equation:

$$P_{dyn} = \frac{1}{2} C_L V^2 \cdot A \cdot F$$
$$= \text{Logic switching power} + \text{Glitch power} \quad (1)$$

where A is switching activity and F is the circuit operating frequency.

Logic switching power is directly proportional to the loading capacitances, C_L, which linearly depends upon gate sizes, gate width and gate length. Local (intra-die) process variation causes gate sizes to vary randomly and hence does not affect logic switching power too much. Global (inter-die) process variation changes gate sizes in the same tendency and does vary the logic switching power. However, it does not affect the solution of our MILP formulation, since gate delays and gate sizes in the MILP constraints either increase or decrease with the same percentage when global process variation is considered, and T_{max} (maximum circuit performance) is assumed to change accordingly.

The impact of process variation on glitch power is different and more complicated. Glitches are generated if the glitch filtering condition (2) [7] is not satisfied for cell i. Since inertial gate delays d_i vary with process variations,

inequality (2) may change from being satisfied to being violated or vice versa.

$$d_i \geq T_i - t_i \quad (2)$$

We consider the impact of global process variation and local process variation on glitch power separately.

- **Impact of global process variation on glitches**

For every gate *i*, its timing window T_i - t_i is actually determined by the two timing paths, the fastest path (*FPath*) and the slowest path (*SPath*) from primary inputs to gate *i*. T_i is the cumulative inertial gate delays along that slowest path, and t_i is the cumulative inertial gate delays along that fastest path, which is shown in equation (3).

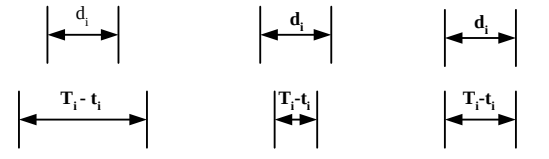
$$T_i - t_i = \sum_{m \in SPath} d_m - \sum_{n \in FPath} d_n \quad (3)$$

Assuming there is $r \cdot 100\%$ (r: 0~1) of global variation applied to the circuit, glitch filtering conditions for gate *i* keep unchanged since both timing window, $T_i - t_i$, and gate delay vary $r \cdot 100\%$. Therefore, the technique of glitch elimination by path balancing is resistant to the global process variation.

- **Impact of local process variation on glitches**

Now, let's consider the impact of local process variation on glitch elimination by path balancing. When local variation is applied to a circuit, T_i and t_i are the sum of gate delays, which vary randomly, along the slowest and the fastest paths from primary inputs to cell *i*'s inputs, so, T_i - t_i is not very sensitive to the process variations, while d_i does change with the process variation.

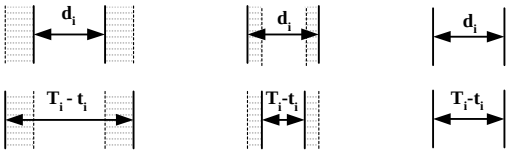
As shown in Figure 1, there are three possible glitch filtering conditions. Both Figures 1(b) and 1(c) are glitch free while Figure 1(a) has a glitch. In an un-optimized (with-glitch) circuit, Figures 1(a) or 1(b) is the much more common condition for one gate, although Figure 1(c) is still possible but with the least possibility. On the contrary, in a glitch-free optimized circuit, Figure 1(c) is applied to lots of gates because Figure 1(a) is always forced to become Figure 1(c) by path balancing for glitch elimination.



(a) Glitch Not Free (b) Glitch Free (c) Glitch Free

Figure 1. Three possible glitch filtering conditions.

With local process variation, Figures 2(a) and 2(b) show that the original condition is not so easily corrupted if only the variation of the timing window or the gate delay falls into the shaded areas, while Figure 2(c) is extremely sensitive to the local process variation, since a slight increase of the timing window or decrease of the gate delay can simply let an original glitch-free gate generate glitches at its output.



(a) Glitch Not Free (b) Glitch Free (c) Glitch Free

Figure 2. Three possible glitch filtering conditions under local process variation.

This explains why the dynamic power of an un-optimized (with-glitch) circuit is much more resistant to local process variation than that of a glitch-free circuit optimized by path balancing. The glitch-free condition shown in Figure 1(c) cannot be really satisfied even with a quite small process variation.

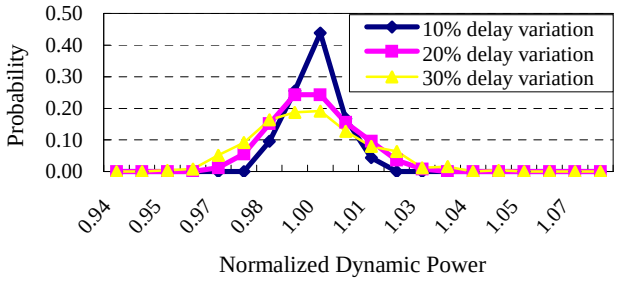


Figure 3. Normalized dynamic power distribution of un-optimized (with -glitch) C432 under local delay variation

Figure 3 demonstrates the resistance of un-optimized circuits to the local process variation. We apply 10%, 20% and 30% local delay variations, which are caused by the variation in gate-length-independent $V_{th,}$ to the un-optimized (with-glitch) circuit C432. The largest percentage of the mean value deviated from the nominal value is 0.22% and the maximum spread (3*S.D./mean) is only 4.5%.

The sensitivity of glitch-free circuits optimized by path balancing to the local process variation is illustrated by Figure 4. It shows that both the mean free circuits optimized by path balancing to the local process value and standard deviation of dynamic power distribution increase significantly with the increase of the local process variation. When 30% local variation is applied to the optimized glitch-free C432, its average dynamic power increase 32% and almost equals to the normalized dynamic power (1.34) of un-optimized C432. In Figure 4, some samples of optimized C432's dynamic power are even larger than 1.34. It should be mentioned that every sample in Figure 4 is larger than the nominal value, 1, which is the expected minimum-normalized-dynamic-power of optimized glitch-free C432 achieved by path balancing. Process variation causes some glitches to be

generated in this glitch-free circuit and hence increases the dynamic power.

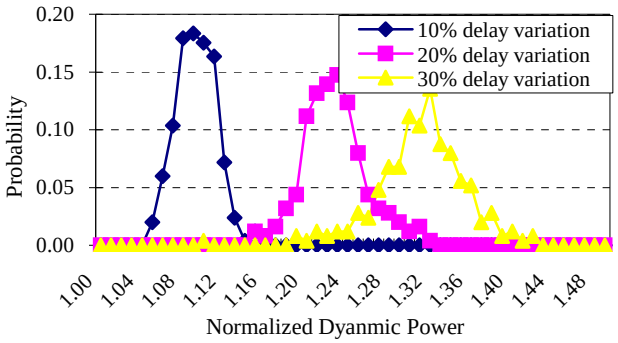


Figure 4. Normalized dynamic power distribution of optimized (glitch-free) C432 under local delay variation.

It is remarkable that the advantage of glitch elimination by path balancing is totally lost due to the local process variation. The deterministic approach of path balancing is not effective for power optimization with process variation. In the following section, we combine the MILP formulations introduced in [15-17], and thus a new statistical MILP formulation is proposed to optimize total power under process variation and to fully utilize the advantage of path balancing.

The deterministic MILP [15-16] using path balancing and dual-V_{th} assignment to reduce the total power consumption is first adopted as a prerequisite for later modification to consider process variation.

3. Statistical MILP for Total Power Optimization with Process Variation

In the statistical MILP formulation, we treat all gate delays and timing window variables as random variables with normal distribution whose standard deviation is σ_r.

3.1 Variables

- **Integer variables:**

In our cell library, each standard cell has two possible threshold voltages and three alternative sizes (1X, 2X and 4X). Therefore, this MILP has six integer variables since each device has 6 alternative choices.

$X1L[i]$, $X2L[i]$, $X4L[i]$, $X1H[i]$, $X2H[i]$, $X4H[i]$

- **Continuous Variables:**

$\delta[i]$ - relaxed variable for the glitch filtering constraint of cell i. It will be discussed in Section 3.3.

$Size[i]$ - size of cell i.

$I_{leak}[i]$ - nominal value of leakage of cell i.

$u\_D[i]$ - mean of inertial gate delay of cell i.

$s\_D[i]$ - standard deviation of inertial gate delay.

$u\_\Delta d[i,j]$-mean of $\Delta d[i,j]$ (the delay of the inserted delay element).

$s\_\Delta d[i,j]$ - standard deviation of $\Delta d[i,j]$.

$u\_T[i]$ - mean of $T[i]$.

$s\_T[i]$ - standard deviation of $T[i]$.

$u\_t[i]$ - mean of $t[i]$.

$s\_t[i]$ - standard deviation of $t[i]$.

3.2 Constants

T_{max} - the maximum expected circuit performance.

σ_r - standard deviation of the process parameter variations.

$S_{X2}[i]$ - gate size of cell i with 2X driving strength.

W_1, W_2 ,W_3 - weight factors.

$I_{X2L}[i]$, $I_{X2H}[i]$ - nominal values of the subthrehold leakage of cell i with 2X driving strength.

$D_{X1L}[i]$, $D_{X2L}[i]$, $D_{X4L}[i]$, $D_{X1H}[i]$, $D_{X2H}[i]$, $D_{X4H}[i]$ - nominal values of the inertial gate delay of cell i at all six corners.

3.3 Constraints

- **Basic constraints**

Let LP solver choose one and only one optimal version for cell i.

$$X1L[i]+X2L[i]+X4L[i]+X1H[i]+X2H[i]+X4H[i]=1 \quad (4)$$

Nominal value of the subthreshold leakage of cell i:

$$u\_I_{leak}[i]=(0.5\cdot X1L[i]+X2L[i]+2\cdot X4L[i])\cdot I_{X2L}[i]+(0.5\cdot X1H[i]+X2H[i]+2\cdot X4H[i])\cdot I_{X2H}[i] \quad (5)$$

Mean and standard deviation of the gate delay of cell i:

$$u\_D[i]=D_{X1L}[i]\cdot X1L[i]+D_{X2L}[i]\cdot X2L[i]+D_{X4L}[i]\cdot X4L[i]+D_{X2L}[i]\cdot X1H[i]+D_{X2L}[i]\cdot X2H[i]+D_{X4L}[i]\cdot X4H[i] \quad (6)$$

$$s\_D[i]=\sigma_r\cdot u\_D[i] \quad (7)$$

The size of cell i:

$$Size[i]=\left\{\begin{matrix}0.5\cdot(X1L[i]+X1H[i])+(X2L[i]+X2H[i])+\\2\cdot(X4L[i]+X4H[i])\end{matrix}\right\}\cdot S_{X2}[i] \quad (8)$$

- **For glitch elimination**

Instead of using inequality (2), in the statistical method, we adopt the following glitch filtering constraint:

$$u\_D[i]-3\times s\_D[i]\geq(u\_T[i]+3\times s\_T[i])-(u\_t[i]-3\times s\_t[i]) \quad (9)$$

This constraint can leave certain margin for process variation in advance as shown in Figure 2(b) instead of Figure 2(c). However, normally the above worst case constraint is too tight to make CPLEX LP solver find a feasible solution. So, we add a relaxed variable ***δ*[i]** to each glitch filtering constraint (9).

$$\delta[i]+(u\_D[i]-3\times s\_D[i])\geq(u\_T[i]+3\times s\_T[i])-(u\_t[i]-3\times s\_t[i]) \quad (10)$$

In the objective function, by minimizing $\Sigma\delta[i]$, CPLEX LP solver will try to find one optimal solution to make as large number of constraints (10) satisfied as possible with a zero $\delta[i]$, which means the glitches of corresponding cells can be truly eliminated even in the worst case condition of process variation. Those constraints only being satisfied with the help of a positive $\delta[i]$ quite likely fail to filter glitches.

- **For maximal performance**

To keep the maximal performance, at every primary output k, let,

$$u\_T[k]+3\times s\_T[k]\leq T_{\max}. \quad (11)$$

3.4 Objective function

The objective function minimizes the impact of process variation on the total power consumption.

Min {the impact of process variation on the total power consumption}

= Min {mean and standard deviation of leakage power + mean and standard deviation of dynamic power}

=

$$Min\left\{W_1\cdot C_1\sum_i I_{leak}[i]+W_2\cdot\left(C_2\sum_i size[i]+C_3\sum_i\sum_j\Delta d[i,j]\right)+W_3\cdot\sum_i\delta[i]\right\} \quad (12)$$

C_1, C_2 and C_3 are fitting parameters to let three terms ($C_1\Sigma I_{leak}[i]$, $C_2\Sigma size[i]$ and $C_3\Sigma\Sigma\Delta d[i,j]$) have the same units (uW).

When we talk about process variation, its impact on the mean and standard deviation of the power consumption should both be considered. For leakage, a smaller mean value automatically means a narrower spread of leakage power distribution since more gates are assigned high V_{th}. Min($C_1\Sigma I_{leak}[i]$) should be enough to minimize the impact of process variation on the total subthreshold leakage. For the dynamic power, standard deviation of the dynamic power distribution is determined by $\Sigma\delta[i]$, and ($C_2\Sigma size[i]+C_3\Sigma\Sigma\Delta d[i,j]$) affects the average dynamic power. Therefore we should minimize ($C_2\Sigma size[i]+C_3\Sigma\Sigma\Delta d[i,j]$) and $\Sigma\delta[i]$ simultaneously.

The objective function (12) is composed of three parts (three single objectives), including, to minimize the average leakage power, to minimize the average dynamic power and to minimize the standard deviation of the dynamic power. It is actually a multi-objective function and each single objective conflicts with others, for instance, to minimize $\Sigma\delta[i]$ results in the increase of $\Sigma\Sigma\Delta d[i,j]$, and to optimize $\Sigma I_{leak}[i]$ leads to a larger $\Sigma size[i]$, *etc*. It is not easy to get one optimum value for every single objective. What we can do instinctively is to carefully select weight factors, W_1, W_2 and W_3 to make a tradeoff among these three objectives.

It should be noticed that the solution provided by a deterministic MILP [15-16] gives us a rough image of which one is the dominant component between leakage and dynamic power. We also get their exact optimal values (power consumption) for the optimized circuit. Based on that information, we can choose weight factors and add some constraints of the largest allowable minimal leakage or dynamic power in the statistical MILP formulation empirically.

The choice of minimizing the impact of process variation on the leakage or reducing the effect of process variation on the dynamic power is determined by which one is the dominant one between the leakage and the dynamic power, and the circuit applications as well. In a circuit optimized by the deterministic MILP,

- Case 1 - if the optimal leakage is much less than the optimal dynamic power and its large spread due to process variation (for example, 5X difference under 30% global process variation) still can be ignored, we need put much more emphasis on dynamic power resistance to process variation;
- Case 2 - if the optimal leakage is comparable to the optimal dynamic power, and most of the time the circuit in the standby mode, for example, circuits of cell phones, the impact of process variation on the optimal leakage should be minimized with priority definitely since leakage is much more sensitive to the process variation;
- Case 3 - if the optimal leakage is comparable to the optimal dynamic power, and most of the time the circuit is in the active mode, for example, circuits of portable GPS or portable game machines, *etc*., both the mean and standard deviation of the dynamic power distribution should be optimized in the first place.

3.5 Minimizing impact of process variation on leakage

In case 1 and case 3, dynamic power is the dominant component of the total power consumption. Its standard deviation is determined by the number of glitch filtering constraints (10) whose $\delta[i]$ are positive values. So, in the MILP objective function (13), we first let *W3* be infinitely large to put the highest priority on minimizing $\Sigma\delta$[i].

$$Min\left\{W1\cdot\sum_i I_{leak}[i]+W2\cdot\left(\sum_i size[i]+\sum_i\sum_j\Delta d[i,j]\right)+\underset{W3->\infty}{W3}\sum_i\delta[i]\right\} \quad (13)$$

Although MILP tries to minimize $\Sigma\delta[i]$, $\delta[i]$ for some gate may still be positive since the constraint (9) is too tight to be satisfied without the help of a positive $\delta[i]$. Every positive $\delta[i]$ possibly results in the glitch generation at gate i's output. From Figure 4, we can also see that the average dynamic power linearly increase with the process variation approximately. This increase is contributed by the glitch power, which generates under process variation condition. To counteract the increase in the average dynamic power due to those glitches, or to let the really average dynamic power in process variation condition still be close to that one achieved by the deterministic MILP formulation, we have to sacrifice some leakage power to get a smaller logic switching power in advance. This can be achieved by letting *W1* and *W2* both equal to 1 in the MILP objective function (14) and adding a new constraint (15) to the statistical MILP formation.

$$Min\left\{C_1\sum_i I_{leak}[i]+\left(C_2\sum_i size[i]+C_3\sum_i\sum_j \Delta d[i,j]\right)+\underset{W->\infty}{W3}\sum_i \delta[i]\right\} \quad (14)$$

$$C_2\sum_i size[i]+C_3\sum_i\sum_j \Delta d[i,j] < P_{dyn\_opt}/\rho \quad (\rho>1) \quad (15)$$

P_{dyn_opt} is the optimal dynamic power obtained by the deterministic MILP [15-16] and ρ is a constant determined by the process variation. By letting ρ larger than 1, the statistical MILP formulation can give an optimal circuit which has less dynamic power.

3.6 Minimizing impact of process variation on leakage

In case 2, leakage almost equals to or is even larger than the dynamic power. Since leakage is so sensitive to the process variation that we cannot minimize the effect of process variation on the dynamic power by sacrificing leakage any more. The technique of using path balancing to eliminate glitches has to be discarded since the increase in the average dynamic power under process variation may be close to or even larger than the glitch power eliminated by path balancing. To let the leakage of optimized circuits resistant to the process variation, we can still use the MILP proposed in [17] except every gate has six possible choices instead of two choices.

4. Results

In C432 optimized by the deterministic MILP formulation in [15-16], the optimized total power comprises 59.3uW dynamic power and 5.54μW leakage power. With 15% local process variation, its average dynamic power increase 13.53% and with 5.34% standard deviation. To reduce the impact of process variation on its dynamic power, the objective function (14) and constraint (15) (let P_{dyn_opt}=59.3μW and ρ=1.10) are adopted in the statistical MILP formulation. The two curves in Figure 5 show that the average dynamic power only increases 3.63% instead of 13.53%, and standard deviation is also reduced to 2.82% from 5.13% when 15% local process variation is applied to the optimized glitch-free C432, although at a cost of 94% average leakage power increase (from 1.0 to 1.94) and a little bit wider spread of leakage power distribution, which is shown in Figure 6.

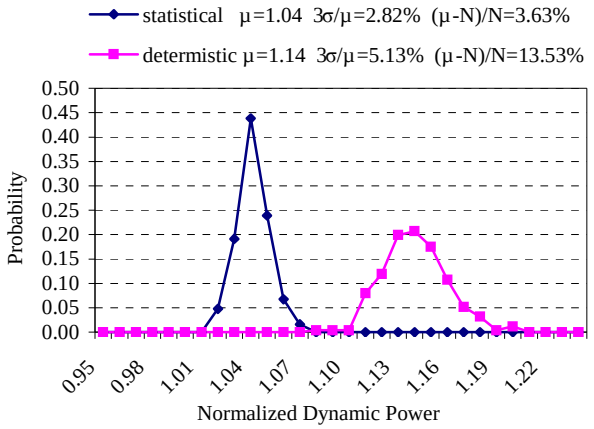


Figure5. Comparison of the impacts of 15% local process variation on the **dynamic power** in C432 which is optimized by the statistical MILP with the emphasis on the resistance of dynamic power to process variation, or by the deterministic MILP [15-16]. (N=1, is the expected normalized minimum dynamic power in the optimized glitch-free C432).

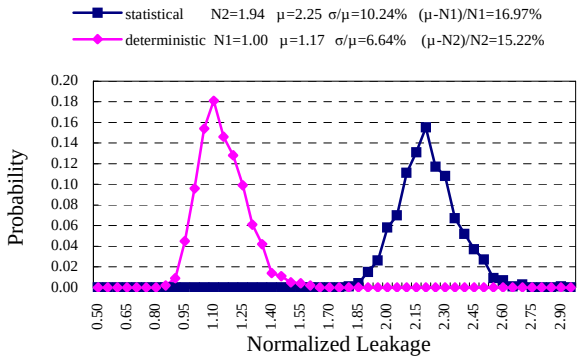


Figure 6. Comparison of the impacts of 15% local L_{eff} process variation on the **leakage power** in C432 which are optimized by the statistical MILP with the emphasis on the resistance of dynamic power to process variation, or the deterministic MILP [15-16]. (N1 and N2 are the normalized nominal leakage power in the optimized glitch-free C432).

5. Summary

In this paper, the impact of process variation on dynamic power is analyzed, and a statistical MILP formulation is presented to minimize the total (dynamic and leakage) power in glitch-free circuits considering process variation. The impact of process variation on dynamic power can be minimized by giving up some leakage if the dynamic power is still the dominant power component under process variation. Figure 7 gives the flowchart of how to

make a decision as to which one, leakage or dynamic power, should be optimized with process variation.

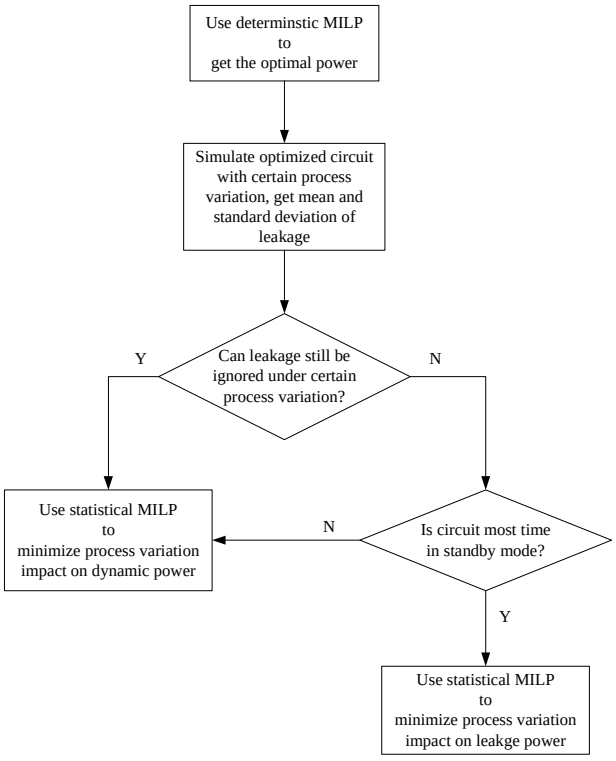


Figure 7. An algorithm to determine whether leakage or dynamic power should be optimized with process variation.

6. References

[1] M. Mani, A. Devgan, and M. Orshansky, "An Efficient Algorithm for Statistical Minimization of Total Power Under Timing Yield Constraints," in *Proc. Design Automation Conference*, 2005, pp. 309-314.

[2] A. Davoodi and A. Srivastava, "Probabilistic Dual-V_{th} Optimization Under Variability," *Proc. ISLPED*, 2005, pp. 143-147.

[3] A. Srivastava, D. Sylvester, D. Blaauw, "Statistical Optimization of Leakage Power Considering Process Variations Using Dual-V_{th} and Sizing," *Proc. DAC*, 2004, pp. 773-778.

[4] M. Mani, A. Devgan and M. Orshansky, "An Efficient Algorithm for Statistical Minimization of Total Power Under Timing Yield Constraints," *Proc. DAC*, 2005, pp. 309-314.

[5] A. P. Chandrakasan and R. W. Brodersen, *Low Power Digital CMOS Design*. Boston: Springer, 1995.

[6] V. D. Agrawal, "Low Power Design by Hazard Filtering," in *Proc. 10th International Conf. VLSI Design*, 1997, pp. 193-197.

[7] V. D. Agrawal, M. L. Bushnell, G. Parthasarathy, and R. Ramadoss, "Digital Circuit Design for Minimum Transient Energy and a Linear Programming Method," in *Proc. 12th International Conf. VLSI Design*, 1999, pp. 434-439.

[8] E. Jacobs and M. Berkelaar, "Using Gate Sizing to Reduce Glitch Power," in *Proc. PRORISC/IEEE Workshop on Circuits, Systems and Signal Processing*, 1996, pp. 183-188.

[9] S. Kim, J. Kim, and S. Y. Hwang, "New Path Balancing Algorithm for Glitch Power Reduction," *IEE Proc. of Circuits, Devices and Systems*, vol. 148, no. 3, pp. 151-156, 2001.

[10] C. V. Schimpfle, A. Wroblewski, and J. A. Nossek, "Transistor Sizing for Switching Activity Reduction in Digital Circuits," in *Proc. European Conference on Theory and Design*, 1999.

[11] A. Wroblewski, C. V. Schimpfle, and J. A. Nossek, "Automated Transistor Sizing Algorithm for Minimizing Spurious Switching Activities in CMOS Circuits," in *Proc. IEEE International Symposium on Circuits and Systems*, 2000, pp. 291-294.

[12] T. Raja, V. D. Agrawal, and M. L. Bushnell, "Minimum Dynamic Power CMOS Circuit Design by a Reduced Constraint Set Linear Program," in *Proc. 16th International Conf. VLSI Design*, 2003, pp. 527-532.

[13] F. Hu and V. D. Agrawal, "Input-Specific Dynamic Power Optimization for VLSI Circuits," in *Proc. of the International Symposium on Low Power Electronics and Design*, 2006, pp. 232-237.

[14] F. Hu, "Process-Variation-Resistant Dynamic Power Optimization for VLSI Circuits," PhD Thesis, Auburn, Alabama: Auburn University, May 2006.

[15] Y. Lu and V. D. Agrawal, "CMOS Leakage and Glitch Power Minimization for Power-Performance Tradeoff," *Journal of Low Power Electronics*, vol. 2, no. 3, pp. 378-387, Dec. 2006.

[16] Y. Lu and V. D. Agrawal, "Leakage and Dynamic Glitch Power Minimization Using Integer Linear Programming for Vth Assignment and Path Balancing," in *Proc. of the International Workshop on Power and Timing Modeling, Optimization and Simulation*, 2005, pp. 217–226.

[17] Y. Lu and V. D. Agrawal, "Statistical Leakage and Timing Optimization for Submicron Process Variation," in *Proc. 20th International Conf. VLSI Design*, 2007, pp. 439-444.