2009 22nd International Conference on VLSI Design

# Soft Error Rates with Inertial and Logical Masking*

Fan Wang
Juniper Networks, Inc.
Sunnyvale, CA 94089, USA
*fanw@juniper.net*

Vishwani D. Agrawal
Auburn University, Dept. of ECE
Auburn, AL 36849, USA
*vagrawal@eng.auburn.edu*

## Abstract

*We analyze the neutron induced soft error rate (SER). An induced error pulse is modeled by two parameters, probability of occurrence and probability density function of the pulse width. We calculate failures in time (FIT) rates for ISCAS85 benchmark circuits. A comparison with measured SER for SRAMs shows better relevance of our work over other published work. Our CPU times are reasonable; benchmark circuit C1908 with 880 gates requires only 1.14 seconds. Further, we study the influence of circuit topology on SER. We find that for some circuits with many levels of logic there exists a critical single event transient (SET) width. For smaller induced pulse width the SER depends not on the size of the circuit but only on the gates near the output, and only those need to be protected. For an inverter chain in TMSC035 technology, the critical width is between 25ps and 50ps. For a shallow circuit, e.g., a ripple-carry adder, the critical SET width may not exist.*

## 1 Introduction

Continuous downscaling of CMOS technologies has resulted in clock frequencies in the multiple gigahertz range, supply voltage below one volt and load capacitances of circuit nodes dropping to femtofarads. As a result, soft error rates in logic and processor circuits are increasing. In addition, if other circuit noises such as interconnect coupling and ground bounce are also considered soft errors, the logic FIT (*failure in time*, 1 FIT = 1 failure in $10^9$ hours) rate is expected to increase faster and become comparable to the FIT rate of memories [9]. The SER due to high-energy neutrons in SRAM cells, latches, and logic circuits for feature sizes from 600nm to 50nm have been reported [25]. According to that study, the SER of logic circuits is expected to increase nine orders of magnitude from 1992 to 2011, becoming comparable to the failure rate of unprotected on-chip memories.

Well-known noise sources include noisy power supply, lightning, electrostatic discharge (ESD), ground bounce, and interconnect coupling capacitances. With advances in the design and manufacturing technology, such non-environmental conditions may not remain the dominant influence on the sub-micron semiconductor reliability. Errors caused by cosmic rays and alpha particles will become the prevalent reliability issue in electronic systems. A detailed discussion on the source of alpha particles and neutrons and their effects on electronics can be found in a recent tutorial paper [30].

In Section 2, we summarize the previous work on soft error rate estimation and in Section 3, we will review a novel environment dependent soft error model, which is based on both error occurrence rate represented as a probability, and the single event transient (SET) pulse density represented as a probability density function [28, 29, 31]. We favor this model because it includes both inertial and logic masking effects inherent in digital circuits. In Section 4, we compare analysis results with relevant published work. We discuss various key factors that may influence logic SER. Some of those factors are barely considered in existing logic SER estimation work. In Section 5, we study the influence of circuit topology on soft error rate.

## 2 Previous Work

Soft-error studies have traditionally been experimental where one uses an accelerated life environment for a VLSI device [12]. Typically, a neutron beam accelerator may be used. An alternative is a real life environment where a tester evaluates the failure rate for hundreds of chips at nominal conditions. Though field testing is very expensive and takes up to a year to obtain reliable results, it is important to validate the accelerated testing assumptions. The long delay in getting the SER results is often unacceptable for a contemporary chip market. Alternative is either a costly test of more chips with bigger tester or deviation from the nominal conditions to more sensitive ones [35]. For example, the test facilities in the Jungfraujoch lab in Switzerland located at 11,000 feet can accelerate ground-level test times by a factor of 11. In this lab, *iRoC Technologies* obtained a statistically significant number of soft errors on several different devices over a period of 4 to 6 months [16].

The JEDEC (*Joint Electron Device Engineering Council*) standard includes JESD89, JESD89-A [10] and JESD89-2. In JESD89 [10], the standard specifications cover soft errors due to alpha particles and atmospheric neutrons. These standards specify that the SER data obtained from alpha accelerated SER tests should be extrapolated to an alpha flux of 0.001 particles/hr-cm$^2$. For example, the neutron accelerated SER (*ASER*) test results have been extrapolated to the typical neutron flux observed at New York City. For energy in the range of 10–10000 MeV, the neutron flux is $3.9\times10^{-3}$ N/cm$^2$-s and when the energy range

*This research is supported in part by the National Science Foundation Grant CNS-0708962.

1063-9667/09 $25.00 © 2009 IEEE
DOI 10.1109/VLSI.Design.2009.77



IEEE computer society

is from 1 to 10 MeV, the neutron flux is $4.0\times10^{-3}$ N/cm$^2$-s [8, 10]. Primarily, the procedures apply to memory devices like DRAMs and SRAMs, but with some adjustments can be used for logic devices [10].

The existing computer programs to model the single event effects (*SEE*) on electronics include SEMM, developed by IBM [26]; CRIME, supported by U.S. Air Force and Office of Naval Research grant [4] and CREME96 from Naval Research Laboratory [27].

Unlike memories, soft errors in logic circuits may be filtered out by the circuit itself and may not effect the circuit performance. This is known as logic masking, electrical masking or temporal masking [18]. Also, the complex topology of a logic circuit is different from memory's regular structure.

Asadi *et al.* [2] present a soft error rate estimation technique based on error probability propagation. Rejimon and Bhanja [24] gave a single event fault model based on probabilistic Bayesian networks, which captures spatial dependencies. These approaches do not take the circuit electrical masking factor and the characteristic of transient pulses like pulse widths into account. An improvement was provided by Zhao *et al.* [33], who proposed a constraint-aware robustness insertion methodology to protect the sequential elements in digital circuits against various noise effects. However, the authors did not include the environmental factors like the error frequency. Besides, their propagation method required tabulating all the pulse width and height data for each logic gate. It would thus take enormous memory for large logic circuits. Other notable logic circuit SER estimation work includes SEAT-LA [21], SERA [32] and an algorithm by Rao *et al.* [23].

Mohanram and Touba [17] gave a cost effective approach to selectively protect high susceptibility nodes in logic circuits. A recent paper [15] proposed symbolic approaches using binary decision diagrams, algebraic decision diagrams and a probabilistic model for sequential SER analysis. Rewriting, with optimization for area and power consumption, can also be used for reducing the soft error rate [1].

## 3 Environment-Based Model

Different from memories, in a logic circuit, a single event effect exists as a single event transient (SET) pulse. An SET has its unique characteristics like polarity, waveform, amplitude and duration, and these characteristics depend on particle impact location, particle energy, device technology, device supply voltage and output load. A single event upset does not occur unless the SET can survive the circuit masking effects and is captured by a clock edge of some sequential element [16].

Environmental neutrons come from cascaded interactions when galactic cosmic rays traverse through earth's atmosphere. These neutrons reach the ground with finite probabilities [19]. The intensity of cosmic-ray induced neutrons flux in the atmosphere varies with altitude, location in the geomagnetic field, and solar magnetic activity. The flux rate data is available from the reported measurement records over decades [14]. Not every particle hit on the sensitive silicon area can induce an error. An SEU occurs with certain probability for each high-energy particle hit. Such probability can be obtained from existing computer programs, for example, IBM's SEMM (Soft Error Monte-Carlo Modeling) program [26].

We consider all energy components in the proposed soft error model. We average the error probability over different energies and assign each circuit node with a unique error occurrence probability.

The particle energy distribution at any specific geographic locations for any specific technology can be obtained from experimentally measured results. For example, the cosmic particle strikes were simulated using a heavy ion beam at the Twin Tandem Van de Graaff accelerator of the Brookhaven National Laboratory. Those results suggest that in the natural environment of space the probability distribution of high-energy particles falls rapidly with increasing energy. For $0.5\mu$ and $0.35\mu$ CMOS technology processes at the ground level, the largest population has an linear energy transfer (LET) of $20 MeV\text{-}cm^2/mg$ or less and the particles with LET greater than $30 MeV\text{-}cm^2/mg$ are exceedingly rare [7]. LET determines the ionization energy and hence the charge collection as the particle traverses through the material of a switching device.

The transient current pulse created by a striking particle with given LET has been represented by a double exponential expression [13]:

$$\begin{cases} I(t) = \frac{Q_{coll}}{\tau_\alpha - \tau_\beta}(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}) & \text{(a)} \\ Q_{coll} = 10.8 \times L \times LET & \text{(b)} \end{cases} \quad (1)$$

where $Q_{coll}$ is the collected charge in the sensitive region, $\tau_\alpha$ is the collection time constant, which is a process-dependent property of the junction, and $\tau_\beta$ is the ion-track establishment time constant, which is relatively independent of the technology. In bulk silicon, the typical charge collection depth ($L$) is $2\mu$. For every 1 $MeV\text{-}cm^2/mg$, and an ionizing particle deposits about $10.8fC$ (femtocoulomb) charge along each micron on its track. Typical values are approximately $1.64 \times 10^{-10}sec$ for $\tau_\alpha$ and $5 \times 10^{-11}sec$ for $\tau_\beta$ from measurements [3, 33].

By charging and discharging the circuit node capacitance, the single event transient current pulse is converted into a transient voltage pulse in Figure 1. Figure 2 gives a neutron-induced soft error model for logic circuits. Because the probability per hit is related to the neutron flux which is location dependent, we can easily get the circuit SER in units of *FIT* for different locations if the corresponding neutron flux data is available.

In summary, this probabilistic soft error model is based on two considerations: (1) the SEU occurrence rate, represented as probability and (2) once an SEU occurs, it exists in the logic circuit as SETs with a random pulse width characterized by a probability density function [28, 31].

## 4 Simulation Results

We compare new simulation results with the relevant published work and discuss various key factors

**Table 1. SEU error rate (SER) analysis of ISCAS85 benchmark circuits.**

| Circuit | # PI | # PO | # Gate | Our approach [28, 31] CPU s | Our approach [28, 31] SER (FIT) | Rao et al. [23] CPU s | Rao et al. [23] SER (FIT) | Rajaraman et al. [21] CPU min. | Rajaraman et al. [21] Error Prob. |
|---|---|---|---|---|---|---|---|---|---|
| c432 | 36 | 7 | 160 | 0.04 | $1.18\times10^3$ | <0.01 | $1.75\times10^{-5}$ | 108 | 0.0725 |
| c499 | 41 | 32 | 202 | 0.14 | $1.41\times10^3$ | 0.01 | $6.26\times10^{-5}$ | 216 | 0.0041 |
| c880 | 60 | 26 | 383 | 0.08 | $3.86\times10^3$ | 0.01 | $6.07\times10^{-5}$ | 102 | 0.0188 |
| c1908 | 33 | 25 | 880 | 1.14 | $1.63\times10^4$ | 0.01 | $7.50\times10^{-5}$ | 1073 | 0.0011 |
| Computing platform | | | | Sun Fire 280 R | | Pentium 2.4GHz | | Sun Fire v210 | |
| Circuit technology | | | | TSMC035 | | Std. 0.13$\mu$m | | 70nm BPTM* | |
| Altitude | | | | Ground | | Ground | | N/A | |

**Table 2. Comparison with measured data.**

| (Measured Data) (Altitude Unknown) Devices | SER (FIT/Mbit) | (Estimated Logic Circuit SER) (Ground Level) Our Work (FIT) | Rao et al. [23] (FIT) |
|---|---|---|---|
| 0.13$\mu$m SRAMs [6] | 10,000 to 100,000 | 1,000 to 20,000 | $1\times10^{-5}$ to $8\times10^{-5}$ |
| SRAMs, 0.25$\mu$m and below [11] | 10,000 to 100,000 | | |
| 1 GBit memory in 0.25$\mu$m [20] | 4,200 | | |

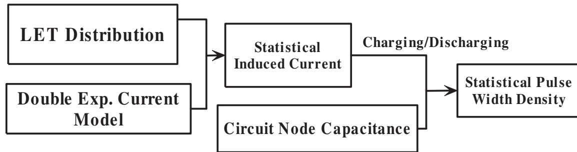


**Figure 1. Transforming statistical neutron energy spectrum to SET width statistics.**

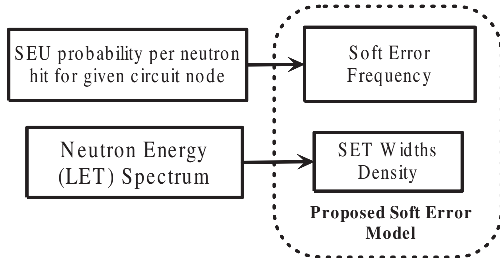


**Figure 2. Proposed probabilistic neutron induced soft error model for logic.**

that may influence logic SER.

For a detailed algorithm to propagate soft errors through elementary logic gates and the algorithm to calculate circuit SER, one may refer to recent publications [28, 31]. We simulated ISCAS85 benchmark circuits by a simulator developed in C programming language. We assume that all circuits are working at the ground level and the probability of SEU per particle hit is $10^{-4}$. We have neglected the polarity of SETs and the temporal masking factor. At ground level we use the neutron energy statistics obtained from [7] assuming the SET width density per circuit node follows a *normal* distribution with mean $\mu = 150$ and standard deviation $\sigma = 50$. These assumptions are justified for relatively small values of particle flux and small chip area. From [34], the total neutron flux at sea level is $56.5m^{-2}s^{-1}$. For a CMOS circuit in TSMC035 technology, we assume the sensitive region to be $10\mu m^2$ for each circuit node. For a circuit with $n$ primary outputs and $m$ nodes, the circuit SER is $\Sigma_{i=0}^{n}(\Sigma_{j=0}^{m} SER_{i_caused_by_j})$ which is different from [31], in which we calculated the SER per gate per output $(\frac{1}{n}\Sigma_{i=0}^{n}(\frac{1}{m}\Sigma_{j=0}^{m} SER_{i_caused_by_j}))$. The unit for SER is FIT.

In Table 1, we compare these results for several benchmark circuits with available results; not all benchmark circuit SER results have been published. Our results have several orders of magnitude difference from the results of Rao et al [23] and the cause of this huge discrepancy will be discussed in the following section. The term BPTM marked with asterisk (*) stands for Berkeley Predictive Technology Model. The run times of our approach appear acceptable. For example, for C1908 with 880 gates, the simulation run time is only 1.14 second.

Field test data for logic circuits is largely unavailable but the actual neutron experiments on a test chip in the future will help validate our analysis. However, the measured SER data for memories, both SRAM and DRAM, is available. Table 2 shows our results, estimated logic SER from Rao et al. [23], and the reported SRAM SER measurement data [6, 11, 20]. Clearly, our results show better relevancy with the measured SRAM SER. In Table 3, we compare the proposed approach with previous relevant works on logic soft error rate estimation [2, 21, 23, 24, 32]. We observe that none of the existing logic SER estimation work has considered the re-convergent fanout, which may have a significant influence on the analysis. We will further discuss these factors in the next section.

From the specification or experimental setup comparison presented in Table 3 we find that to accurately calculate logic SER, factors that influence logic SER estimation should be comprehensively considered. However, no analysis has considered all of them. Consider the following:

(1) The physics of the SEU phenomena seems involved. For example, the analysis of the funneling and the angle of incidence are not considered. We take the energy of neutrons to be the main source that induces the SEU. In reality, it is the physics of interaction be-

**Table 3. Comparison of SEU error rate (SER) estimation methods.**

| Authors and Reference | Factors considered | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | LET Spectrum | Re-conv. Fanout | Sensitive Regions | SEU prob. | Vectors Applied | Location Altitude | Circuit Tech. | SET Degradation |
| Our work | yes | no | yes | yes | no | yes | yes | yes |
| Rao et al. [23] | yes | no | no | no | yes | yes | yes | yes |
| Rajaraman et al. [21] | no | no | no | no | yes | no | no | yes |
| Asadi-Tahoori [2] | no | no | no | yes | no | no | no | no |
| Zhang-Shanbhag [32] | yes | no | yes | yes | yes | yes | yes | yes |
| Rejimon-Bhanja [24] | no | no | no | yes | yes | no | no | no |

tween neutrons and silicon that produces the SEU. Simpler modeling and assumptions may influence the SER estimation accuracy.

(2) The sensitive region of a transistor is defined as the channel region of an off nMOS transistor or the drain region of an off pMOS transistor. For a CMOS circuit, the "on" or "off" status of transistors is determined from inputs. We statically assume that each circuit node's sensitive region is $10\mu m^2$. This may bias the SER result. Although we have considered the sensitive node areas, the strikes on pMOS or nMOS nodes also influence the polarity of the SET. Thus, the dynamic state of the circuit is important.

(3) Compared to the earth's surface, the size of the sensitive region of a single transistor or a circuit board is trivially small and continues to reduce with the technology trend. At the surface of the earth we take the probability of a particle strike to a sensitive node simply by taking the ratio of the number of particle strikes per $\mu m^2$-s to strikes per $m^2$-s. Because 1 m$^2$ equals $10^{12}$ $\mu$m$^2$, most probably there will be no strike on the sensitive regions though such low probability events cannot be neglected. Once the SEU occurs, the SER may easily be several orders of magnitude higher compared to the case of no strike at all. For example, 1 SEU in 6 months (4320 hours) would be measured as 231,480 FIT. On the other hand, a 0 SEU in those 6 months will measure as 0 FIT.

(4) For logic circuits fan-out details should be considered. Our analysis only considers the worst case error rate for re-convergent fan-outs. For example, if a re-convergent fanout has two paths, and one passes through more gates than the other, our program only takes the path that has fewer gates because it is likely to give a higher SER. Timing and logic simulation of all paths would be needed for better accuracy [5]. Two situations can arise as shown in Figure 3:

(a) When SET goes through a high fan-out node, the large load capacitance can eliminate the SET through node inertia.

(b) Or if the SET is not canceled by the fan-out node, it goes through multiple fan-out paths. If all paths have equal length, the SET might cancel itself at a re-converging point depending on path inversions. However, in general, one SET on the affected node can cause several propagating SETs to further increase the SER of the circuit.

Path delays may also influence logic SER.

(5) It is highly recommended to have more field tests for logic circuits. Also, we suggest that the SER results from field tests for the same circuit, even in the same working environment, may be widely different at different times. Still, with field test data, the logic circuit SER results can be validated. A comparison with measurement may be the only way to determine which factors can be really neglected and which assumptions and approximations are justified.

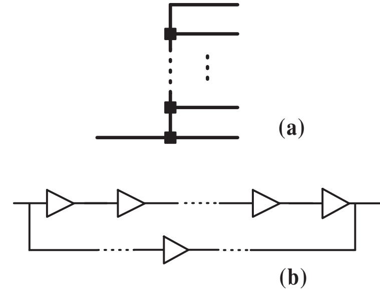


**Figure 3. Circuit fanout stem and reconvergence of paths with different lengths.**

(6) None of the SER estimation approaches consider process variation effects, which may also be a factor in the vulnerability to transient errors. It is reported that, intra-die process variation of threshold voltage may result in SER variation of 41% in a small circuit [22].

## 5 Circuit Topology and SER

The circuit topology is an important factor that influences the logic SER. Deep and shallow circuits, having many or few levels, respectively, may have quite different masking effects on SER. Besides, the operating environment, technology, node capacitances and supply voltage are the other factors that should be considered. Once these factors and their weights are taken into account, we will have information to decide whether and how SEU protection methods should be applied. A good analysis will give circuit engineers opportunities to choose the most economic protection technique instead of the costly traditional methods like triple modular redundancy (TMR).

We analyzed examples of the two types of circuits mentioned above, an inverter chain as a deep circuit and a ripple carry adder as a shallow circuit. To apply the SER estimation method of our recent paper [28, 31], we assumed the working environment is the ground-level. The simulation results are shown in Figure 4. Figures 4 a(1) and b(1) show the circuit schematics. In the inverter chain each gate has

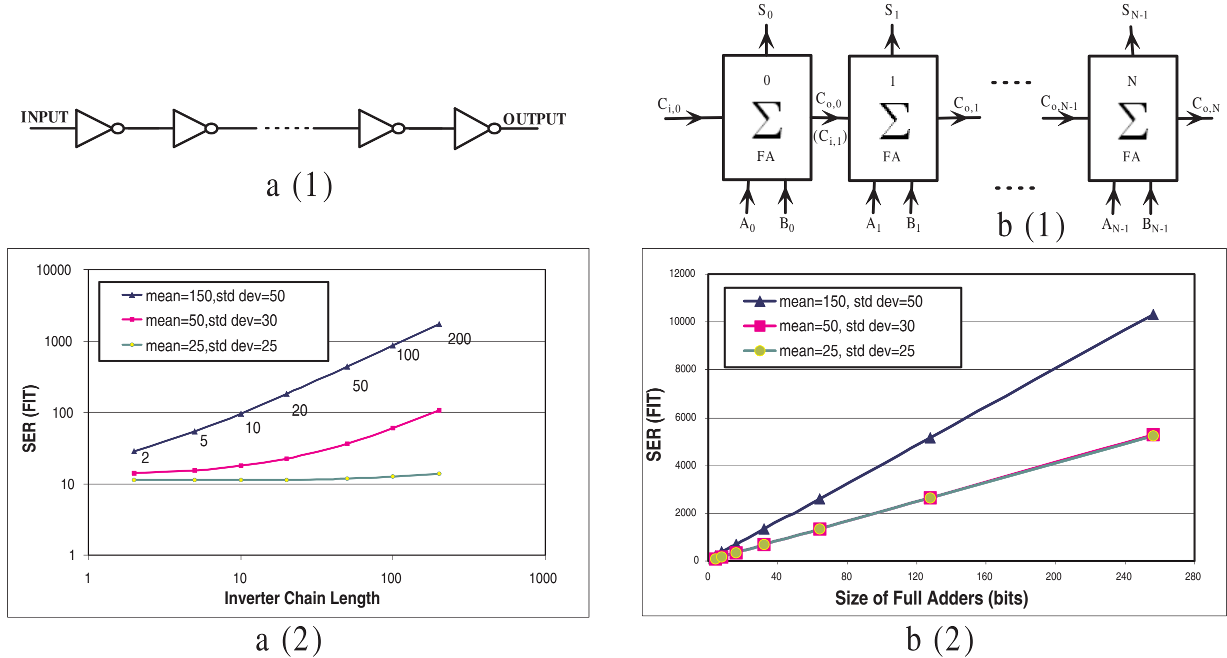


**Figure 4. SER for circuits with different topologies: an inverter chain structure, a(1), and its SER simulation, a(2); a ripple-carry adder, b(1), and its SER simulation, b(2).**

only one input and one output. Thus, there can be only electrical masking and no logic masking. The ripple carry adder has a parallel topology. With the exception of the rippling carry signal, all other inputs ($A_n$ and $B_n$) propagate through the same number of gates to arrive at output ($Sum_n$). Figure 4 a(2) shows the estimation results for different lengths of inverter chains, with three different induced SET width distributions. For the two wider pulse widths (in picoseconds) whose normal distribution mean and standard deviation are (150, 50) and (50, 30), respectively, the SER increases almost linearly with the chain length. In the absence of logic masking, longer the chain, larger is the probability the circuit can be affected by the radiation source. For these two cases the pulse widths are large enough compared to the inertial delay thus survive the electrical masking. When the neutron flux density (mean, standard deviation) is (25, 25), the circuit SER remains fixed even with the increasing chain length. This is because the majority of induced SET pulse widths are small enough so the electrical masking is able to filter out these pulses. We can, therefore, determine a critical pulse width for the inverter chain as being somewhere between 25ps and 50ps. Majority of pulses of smaller widths are filtered out and the SER depends only on a few gates near the output of the chain. Only the gates near the primary output need to be protected against upset.

In Figure 4 b(2) the simulation results for ripple-carry adders are presented. For SET pulse width distributions (mean, standard deviation) of (50, 30) and (25, 25), the two SER curves are almost identical. Even with these SET pulse widths, the SER always increases with the increasing circuit size. This is caused by the parallel topology of the RC adder. Increasing number of gates will increase the cosmic ray hit probability thus causing the circuit SER to increase linearly with the circuit size. For ripple-carry adder, there is no critical SET pulse width below which the transients would be localized.

## 6 Conclusion

We have estimated the logic circuit SER based on an environment-dependent soft error model characterized by error occurrence rate and SET pulse width density. Results show better relevancy over other published work. Field test or accelerated test data on logic devices would be needed to further validate the accuracy of the our analysis. Our soft error rate estimation method requires logic signal probabilities. For any given set of input vectors or signal statistics, these may be obtained either from logic simulation or from static analysis. From our discussion, the logic SER may be highly sensitive to factors like sensitive region calibration, process variation and circuit characterization, making soft error estimation for logic circuits a complex problem. The influence of circuit topology on logic circuits is studied. We proposed a critical SET width such that for smaller pulse widths the SER does not increase with the increasing circuit size. However, for a shallow and wide circuit like a ripple-carry adder, the critical pulse width does not exist. More comprehensive studies should provide better insights for soft error protection schemes in the future.

## References

[1] S. Almukhaizim, Y. Makris, Y. S. Yang, and A. Veneris, "Seamless Integration of SER in

Rewiring-Based Design Space Exploration," in *Proc. International Test Conference*, 2006, pp. 1–9.

[2] G. Asadi and M. B. Tahoori, "An Accurate SER Estimation Method Based on Propagation Probability," *Proc. Design Automation and Test in Europe Conf*, pp. 306–307, 2005.

[3] V. Carreno, G. Choi, and R. K. Iyer, "Analog-Digital Simulation of Transient-Induced Logic Errors and Upset Susceptibility of an Advanced Control System," in *NASA Technical Memo 4241*, 1990.

[4] D. L. Chenette, J. Chen, E. Clayton, T. G. Guzik, J. P. Wefel, M. Garcia-Munoz, C. Lopate, K. R. Pyle, K. P. Ray, E. G. Mullen, and D. A. Hardy, "The CRRES/SPACERAD Heavy Ion Model of the Environment (CHIME) for Cosmic Ray and Solar Particle Effects on Electronic and Biological Systems in Space," *IEEE Trans. on Nuclear Science*, vol. 41, no. 6, pp. 2332–2339, 1994.

[5] A. Dharchoudhury, S. M. Kang, H. Cha, and J. H. Patel, "Fast Timing Simulation of Transient Faults in Digital Circuits," in *Proc. IEEE/ACM International Conference on Computer-Aided Design*, 1994, pp. 719–722.

[6] Graham, "Soft errors a problem as SRAM geometries shrink," http://www.ebnews.com/story/OEG20020128S0079, ebn, 28 Jan 2002.

[7] K. J. Hass and J. W. Ambles, "Single Event Transients in Deep Submicron CMOS," in *Proc. 42nd Midwest Symposium on Circuits and Systems*, 1999.

[8] T. Heijmen and A. Nieuwland, "Soft-Error-Rate Testing of Deep-Submicron Integrated Circuits," in *Proc. Eleventh IEEE European Test Symposium*, 2006, pp. 247–252.

[9] B. Ingols and A. Rambaud, "iRoC Releases Robust SPARC Test Report," *http://www.us.design-reuse.com/news/news65.html*, 2002.

[10] JEDEC, "Measurements and Reporting of Alpha Particles and Terrestrial Comic Ray-Induced Soft Errors in Semiconductor Devices," *JESD89, August*, 2001.

[11] W. Leung, F.-C. Hsu, and M. E. Jones, "The ideal soc memory: 1t-sramtm," in *Proc. 13th Annual IEEE International ASIC/SOC Conference*, 2000, pp. 32–36.

[12] T. C. May, D. L. Crook, D. W. Gralian, R. A. Reininger, and R. C. Smith, "Soft Error Testing," in *Proc. International Test Conference*, 1980, pp. 137–150.

[13] G. C. Messenger, "Collection of Charge on Junction Nodes from Ion Tracks," *IEEE Trans. on Nuclear Science*, vol. 29, no. 6, pp. 2024–2031, 1982.

[14] G. C. Messenger and M. Ash, *Single Event Phenomena*. Chapman & Hall, 1997.

[15] N. Miskov-Zivanov and D. Marculescu, "Circuit Relaiability Analysis Using Symbolic Techniques," *IEEE Trans. on CAD*, vol. 25, no. 12, pp. 2638–2649, Dec. 2006.

[16] S. S. Mitra, N. Kee, and S. Kim, "Robust System Design with Built-In Soft-Error Resilience," *IEEE Design & Test Computers*, vol. 38, no. 2, pp. 43–52, 2005.

[17] K. Mohanram and N. A. Touba, "Cost-Effective Approach for Reducing Soft Error Failure Rate in Logic Circuits," in *Proc. International Test Conference*, 2003, pp. 893–901.

[18] H. T. Nguyen and Y. Yagil, "A Systematic Approach to SER Estimation and Solutions," in *Proc. 41st Annual IEEE International Reliability Physics Symposium*, 2003, pp. 60–70.

[19] E. Normand, "Single-Event Effects in Avionics," *IEEE Transactions on Nuclear Science*, vol. 43, no. 2, pp. 461–474, 1996.

[20] OnlineResource, "Soft Errors in Electronic Memory - A White Paper," Technical report, Tezzaron Semiconductor, 2004.

[21] R. Rajaraman, J. S. Kim, N. Vijaykrishnan, Y. Xie, and M. J. Irwin, "SEAT-LA: A Soft Error Analysis Tool for Combinational Logic," in *Proc. 19th International Conference VLSI Design*, 2006, pp. 499–502.

[22] K. Ramakrishnan, R. Rajaraman, S. Suresh, N. Vijaykrishnan, Y. Xie, and M. J. Irwin, "Variation Impact on SER of Combinational Circuits," in *Proc. 8th International Symposium on Quality Electronic Design*, 2007, pp. 911–916.

[23] R. R. Rao, K. Chopra, D. Blaauw, and D. Sylvester, "An Efficient Static Algorithm for Computing the Soft Error Rates of Combinational Circuits," in *Proc. Conference on Design, Automation and Test in Europe*, 2006, pp. 164–169.

[24] T. Rejimon and S. Bhanja, "An Accurate Probabilistic Model for Error Detection," in *Proc. 18th International Conference on VLSI Design*, 2005, pp. 717–722.

[25] P. Shivakumar, M. Kistler, S. W. Keckler, D. Burger, and L. Alvisi, "Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic," in *Proc. International Conference on Dependable Systems and Networks*, 2002, pp. 389–398.

[26] G. R. Srinivasan, "Modelling the Cosmic Ray-Induced Soft-Error Rate in Integrated Circuits: An Overview," *Microelectronics Reliability*, vol. 37, no. 4, pp. 691–691, 1997.

[27] A. J. Tylka, J. H. Adams Jr, P. R. Boberg, B. Brownstein, W. F. Dietrich, E. O. Flueckiger, E. L. Petersen, M. A. Shea, D. F. Smart, and E. C. Smith, "CREME96: A Revision of the Cosmic Ray Effects on Micro-Electronics Code," *IEEE Transactions on Nuclear Science*, vol. 44, no. 6, p. 2150, 1997.

[28] F. Wang, "Soft Error Rate Determination for Nanometer CMOS VLSI Circuits," Master's thesis, Auburn University, Dept. of ECE, May 2008.

[29] F. Wang and V. D. Agrawal, "Probabilistic Soft Error Rate Estimation from Statistical SEU Parameters," in *Proc. 17th IEEE North Atlantic Test Workshop*, May 2008, pp. 86–92.

[30] F. Wang and V. D. Agrawal, "Single Event Upset: An Embedded Tutorial," in *Proc. 21th International Conference on VLSI Design*, 2008, pp. 429–434.

[31] F. Wang and V. D. Agrawal, "Soft Error Rate Determination for Nanometer CMOS VLSI Logic," in *Proc. 40th Southeastern Symposium on System Theory*, Mar. 2008, pp. 324–328.

[32] M. Zhang and N. R. Shanbhag, "A Soft Error Rate Analysis (SERA) Methodology," in *Proc. IEEE/ACM International Conference on Computer-Aided Design*, 2004, pp. 111–118.

[33] C. Zhao and S. Dey, "Evaluating and Improving Transient Error Tolerance of CMOS Digital VLSI Circuits," in *Proc. International Test Conference*, 2006, pp. 1–10.

[34] J. F. Ziegler, "Terrestrial Cosmic Rays," *IBM Journal of Research and Development*, vol. 40, no. 1, pp. 19–39, 1996.

[35] J. F. Ziegler and H. P. Muhfeld, "Accelerated testing for cosmic soft-error rate," *IBM Journal of Research and Development*, vol. 40, no. 1, pp. 51–63, 1996.