Graphical I_{DDQ} Signatures Reduce Defect Level and Yield Loss

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***Abstract*—We propose a new I_{DDQ} testing signature, the graphical I_{DDQ} signature. We discovered that noise, in the entire set of current measurements for a chip, is a vastly superior feature for classifying chips as good or bad, compared to present methods. The measured I_{DDQ} current as a function of vectors is defined here as the signature. We examine the shape of the waveform defined by the total set of the I_{DDQ} measurements, to extract the number of bands that all of the current measurements cluster into, the width and separation of the bands and current glitches or noise among all I_{DDQ} measurements. We examined the I_{DDQ} signatures of all SEMATECH experiment chips that were classified as good or bad by a combination of functional, delay, and scan voltage tests. A single I_{DDQ} threshold, whether absolute or differential, cannot separate good/bad chips reliably. Good chip signatures contain discrete levels (or bands) of varying widths and separations. A faulty chip almost always displays noise and glitches in the band structure. The graphical I_{DDQ} classifier shows very high accuracy for SEMATECH test data with a test escape rate of 5.97%, compared with 7.5% for the single threshold method, 7.6% for current differences and 7.5% for the ΔI_{DDQ} method. The graphical I_{DDQ} method had a 1.2% test overkill, compared with 2.3% for the single threshold method, 6.1% for current differences and 7.0% for ΔI_{DDQ}.**

***Index Terms*—I_{DDQ} testing, current noise, current signatures, data mining, pattern recognition.**

I. Introduction

THE I_{DDQ} testing [1] finds defects not detectable by voltage tests when the average current caused by a defect is significantly higher than the average quiescent current of good *integrated circuits* (ICs). The variation of quiescent current over a test set, chips, wafers, and fabrication processes must be small, and must not affect the classification. This assumption no longer holds for *deep submicrometer* (DSM) technologies. With the minimum feature size shrinking to less than 70 nm, the subthreshold current increases and the range of all sorts of leakage currents in good devices becomes wider, which makes the differentiation between defective and defect-free devices much harder. Concern has been expressed whether I_{DDQ} testing will remain useful [2]. For DSM devices with high background current, single threshold I_{DDQ} methods result either in unacceptably high levels of *yield loss* (declaring a good chip to be bad) or *test escapes* (declaring a bad chip to be good). Methods were proposed to address the higher leakage current and process variation problems [3]–[7], but improved methods are still needed. Sachdev [8] discusses options for DSM I_{DDQ} testing, including ΔI_{DDQ}, reverse body bias, and power-supply resistive drop methods.

We introduce a graphical model as a current signature. Here, the absolute value of I_{DDQ} current measurement is no longer used for the chip pass/fail decision. Instead, the appearance of noise in recognizable patterns in the measured data over the entire set of test vectors is the distinguishing factor. This view of I_{DDQ} measurements reflects more physical information for discriminating good and faulty devices than the *mean* (μ), *variance* (σ^2), or other comparisons. The self-contained method is not affected by wafer and production process variations. We studied the graphical method on SEMATECH data [9], because it was readily available and had an unusually large number of I_{DDQ} measurements (most other data sets have only 5 or 10). Although the data is old, it illustrates the value of the graphical method very well. Experiments on all SEMATECH data show significant improvement in yield loss (overkill) and defect level (test escapes). This may allow I_{DDQ} testing to substantially reduce the usage of other testing methods. Section II describes prior work. Section III describes the *devices-under-test* (DUTs). Section IV presents the experiment, analyzes physical phenomena, and discusses results. Comparisons appear in Section V, a training set experiment appears in Section VI and statistical significance is analyzed in Section VII. Section VIII is an analysis of testing feature correlation. Section IX is an analysis of the test economics of graphical I_{DDQ} testing and Section X concludes this paper.

II. Prior Work

I_{DDQ} testing was first proposed by Levi [10]. Malaiya and Su [11] and Acken [12] proposed a single pass/fail current threshold. By the mid 1980's, the I_{DDQ} test was proven to detect physical defects (gate oxide shorts, floating transistor gates, stuck-open transistors and bridging, some delay, leakage, and weak transistor faults). Most of these are due to resistive shorts between transistor terminals. In the early 1990's, I_{DDQ} test was used commercially (ViewLogic, Duet, Synopsys, LSI, Lucent, IBM) as a cost-effective test method (no overhead, few test vectors), and for reliability screening [13]. Books on I_{DDQ} testing [1], [14]–[17] exist.

1) Current Signatures: Previously, it was assumed that the variation of the I_{DDQ} current measurement (*energy consumption ratio*) is limited over two different test vectors for a good

Manuscript received June 18, 2004.

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Digital Object Identifier 10.1109/TVLSI.2007.904128

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chip [18]–[20]. Gattiker and Maly [3], [21] observed I_{DDQ} measurements clustering into bands. They developed *current signatures*, with all current measurements sorted by value and found that a significant break (a *current step* or an *activation path*) in the measured current in various vectors indicated an active defect. These steps were often due to activating a different current path through a bridging fault or gate-oxide transistor short. There were two defect kinds: *active* and *passive*. Gattiker *et al.* measured current for the first vector and rejected die if subsequent vector currents differed by more than a threshold.

2) ΔI_{DDQ} Testing: Thibeault [7], [22] took differences in I_{DDQ} measurements between a vector and the next one and plotted them in a histogram to differentiate good and bad chips. ΔI_{DDQ} testing transformed a Gaussian distribution with a mean μ and a variance σ^2 representing the fault-free I_{DDQ} distribution into a distribution with zero mean and a variance $2\sigma^2$. Miller [23] detected active defects [3] for up to 10 mA leakage with ΔI_{DDQ} testing on 100 SRAMs and 197 Pentium microprocessors. The main advantage of ΔI_{DDQ} testing is that the test conditions remain almost identical for both measurements. Small I_{DDQ} anomalies due to active defects are detected, but passive defects are missed. Kruseman *et al.* [24] compared the max-min method of Gattiker *et al.* with Thibeault's method [7] and concluded that neither was more sensitive than the other. They discovered that ΔI_{DDQ} as a function of sorted test patterns was more sensitive than a single ratio-based testing approach.

3) Current Ratios: Maxwell *et al.* [6] used a *current ratio* method with a statistical regression model to dynamically recalibrate the minimum and maximum acceptable leakage current thresholds according to wafer and process variations: $\mathrm{Max\,Threshold} = \mathrm{Slope} \times \mathrm{Min} + \mathrm{Intercept}$. Slope was the slope of the line from the origin to the point representing a DUT on a graph of maximum current against minimum current. Intercept accounted for nonsubthreshold leakage currents. Min was measured from a predetermined minimum current vector.

4) Clustering: A second assumption is that the absolute value of the I_{DDQ} current measurement should be less than a threshold. In current clustering [25]–[28], multiple I_{DDQ} thresholds are used for multiple defect distributions in a single chip. Henry and Soo [4] computed an I_{DDQ} mean μ and standard deviation σ for every vector, and rejected devices when any one I_{DDQ} measurement exceeded $\mu + 4\sigma$ for the corresponding vector.

5) DUT and State Dependence: Li and McCluskey [5] summed up the total variances of I_{DDQ} current to check an I_{DDQ} curve with respect to the standard signature for all vectors. A DUT failed when the sum exceeded $\mu + 4\sigma$. Since other nondefect phenomena might cause fluctuations in current measurements, e.g., *DUT-dependency*, this method had more yield loss than others. Henry and Soo [4] and Li and McCluskey [5] took the *state dependence* into account, but they leveled out the *DUT dependence*. State dependence means that the I_{DDQ} current in a given logic gate depends on the gate input logic states. DUT dependence means that the I_{DDQ} current measured for a die depends on its position on the wafer. Kruseman *et al.* [24] asserted that the DUT dependence will dominate in DSM technologies and showed that $\sigma_{\mathrm{DUT}} = 0.3\sigma_{\mathrm{state}}$, which is a real limitation of the ΔI_{DDQ} method.

6) Miscellaneous Methods: Thibeault [29] took the fast Fourier transform (FFT) of I_{DDQ} measurements and the dc component and the first harmonic were compared with those of good chips to eliminate variation between chips and between wafers and to improve resolution. Chess [30] calculated the mean (μ) I_{DDQ} current for each DUT by measuring the I_{DDQ} current using statistically sufficient test patterns and then determined upper and lower thresholds. Variyam [28] used the difference of the predicted and the measured I_{DDQ} to detect defects. Okuda [31] used the average of the I_{DDQ} current measurements through multiple strobe points as the pass/fail threshold. Lu *et al.* [32] estimated the current σ for DUTs. Then, they either tested the DUT I_{DDQ} current using different test vectors or they tested two chips under the same test vector and compared the difference with 6σ.

III. Test Chip Description and Classification

SEMATECH data is used here [9]. The DUT power supply is 3.3 V. It has 116 000 equivalent (two-input NAND) gates and its two clock domains are 40 MHz and 50 MHz. Five test steps were taken, i.e., wafer level, T0 package level, T1 packaged burn-in level (6 h), T72 packaged burn-in level (78 h), and T144 packaged burn-in level (150 h).[1] In each step, four kinds of tests were applied to each device: stuck-at tests (8023 patterns with 99.79% stuck-fault coverage); functional tests (532 K cycles with 52% stuck-fault coverage); delay tests (15 232 patterns with 91% transition fault coverage); and SEMATECH I_{DDQ} tests (195 patterns with >96% pseudo-stuck-at fault coverage) [33].[2] The SEMATECH experiment used 5 μA as the I_{DDQ} pass/fail limit, which may not be good for production testing. In total, 18 466 devices were tested at wafer test. A subset of them went through the other four test steps. Additional characterization tests were added to package-level tests. Test results were recorded for each test step as well as the kinds of tests failed. Since none of these four tests has complete fault coverage, bad devices may pass all four tests. The single pass/fail current threshold of the I_{DDQ} test means that a device failing only the I_{DDQ} test is not necessarily defective, either. We treat the subset of devices that went through several stages of burn-in and did not fail as good. Here, tested devices are categorized as follows.

1) *Reliable good devices* passing all four tests in all five test steps or passing all available test steps when not all steps are used. Devices that fail wafer probe test, but pass packaged test and burn-in, are good, because the error was due to poor wafer probe registration [34].
2) *Bad devices* failing tests other than the I_{DDQ} test, or having extremely high I_{DDQ} current, > 8 μA, which causes the chip to eventually overheat and fail.
3) I_{DDQ} only fails, which failed only on the I_{DDQ} test with < 8 μA I_{DDQ} current.

The statistical analysis is based on this classification.

[1]Nigh of IBM has explained that there is a discrepancy in this data, so that T72 is really 78 h and T144 is really 150 h.

[2]The *pseudo-stuck-at* fault model for a logic gate includes all hard stuck-at faults and all internal transistor shorts.

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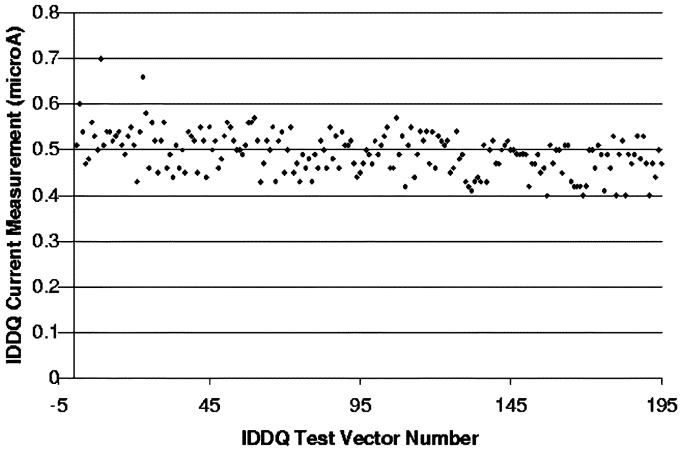

Fig. 1. Good chip with single-band profile.

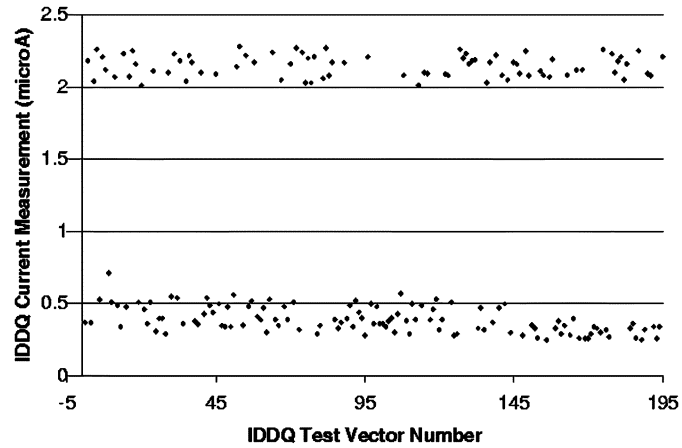

Fig. 2. Good chip with two-band profile.

IV. New I_{DDQ} Classification Features

We introduce a new graphical model for chip classification for current testing [35]–[38]. Instead of using the absolute value of I_{DDQ} current measurement to pass/fail a chip, the graphical appearance of the measurement over the entire set of test vectors is used. This reflects more physical information for discriminating between good and defective devices than μ, σ^2, or other thresholds. The self-contained method will not be affected by the wafer and production process variations. This method differs from the *current signatures* or *current differences* of Gattiker and Maly [3], because it is the noise in the bands of I_{DDQ} measurements that we use to classify chips as good or bad, whereas they classify based on a difference between two consecutive sorted I_{DDQ} measurements. When this difference exceeds a threshold, indicating another activation path due to an active defect, they reject the chip. In our new method, instead, it is the number of bands in the signature, their separations, their widths, the presence of current glitches, and the activity within the bands that is used to classify chips as good or bad. Results will show that ours is a more effective classifier, because it indicates variability in the chip based on the noise-like behavior of the current measurement data.

Previously, it was assumed that the variation range of the I_{DDQ} current measurement is limited for a good chip and that the absolute value of the I_{DDQ} current measurement should be less than a threshold. For the first assumption, we plot each I_{DDQ} current versus test vector number for all 195 vectors and call this the *band diagram*. Sample I_{DDQ} profiles for several chips are shown in Figs. 1–6. Figs. 1 and 2 are two kinds of good devices. There are 5674 good devices out of 18 466 devices having the form of Fig. 2. Fig. 3 is a bad device. Any comparison of the μ's or σ's will fail the good chip of Fig. 2 when the band separation is wide enough so that it exceeds the 4σ threshold, and it will pass the faulty chip of Fig. 3 because the spike does not exceed the 4σ threshold. Another 5684 devices have only one band as in Fig. 1. This also shows that there is no such thing as a current standard for each vector as the second assumption requires.

We plot the I_{DDQ} profile by points or by a line. Fig. 1 is typical of the profile for a good device with a single band, i.e., a high frequency random waveform. Fig. 2 shows the two-band I_{DDQ} profile for a good device. The profiles of single-band faulty devices of Figs. 3 and 4 only differ from good devices due to either continuous or spiked noise. Figs. 5 and 6 are faulty two-band devices. These four devices are typical of the majority of defective devices. In Fig. 3, obvious glitches are observed, while in Figs. 4 and 6, the waveform has high-frequency random signals. However, it differs from the defect-free ones, as the amplitude

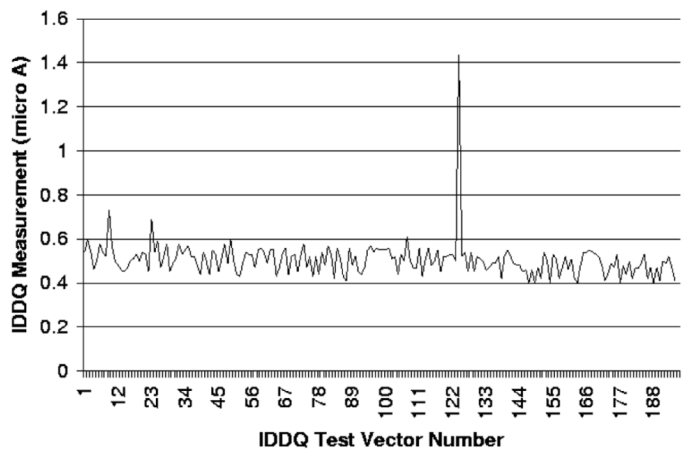

Fig. 3. Faulty chip with noisy single-band profile.

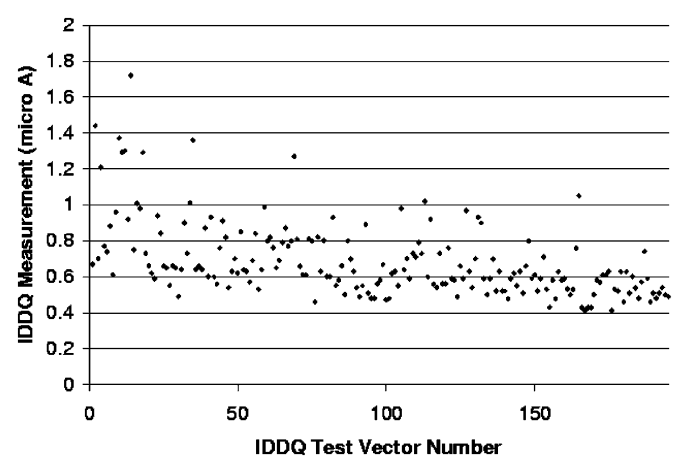

Fig. 4. Faulty chip with smeared single-band profile.

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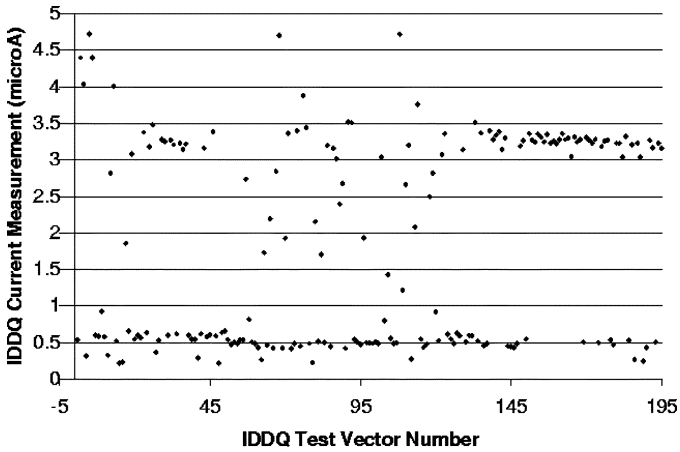

Fig. 5. Faulty chip with smeared two-band profile.

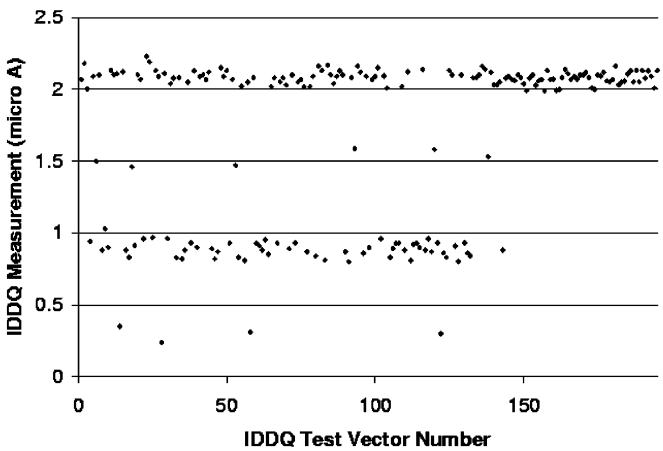

Fig. 6. Faulty chip with smeared two-band profile.

changes obviously in some places. These irregular glitches can either be featured as different bands, or as glitches. The amplitude changes can be described by the number of bands, as in Fig. 6, or by the unclear band, as in Fig. 4. The differentiation between good and bad can only be made by the presence of noise in the band structure.

We propose the use of the following four new features of all I_{DDQ} current measurements for classification purposes:

1) number of bands that all of the current measurements cluster into;
2) width and separation of bands;
3) glitch detection among all I_{DDQ} measurements;
4) lack of activity in the bands.

Even good devices often had non-Gaussian I_{DDQ} measurement distributions that clustered into well-defined bands as in Fig. 2. These devices may have one or more high resistance shorts. Some vectors sensitize these shorts to current flow, by causing opposite potentials across them. Good chips might have multiple band current signatures, if a few high resistance shorts are present. Two or three bands in the good SEMATECH chips indicate one or two switching paths, possibly due to some bridging path(s) with a lower defect resistance. This phenomenon may worsen in DSM technologies. These chips

TABLE I
BAND STATISTICS IN SEMATECH DATA

# Bands	Good devices	Bad devices	Unknown devices
1	5,684	1,592	351
2	5,674	2,429	546
3	487	1,144	104
4	12	367	31
>4	1	44	0
Any	11,858	5,576	1,032

were classified as good by IBM because their anomalies were not detectable by prior I_{DDQ} test methods.

Table I shows statistics for all of the SEMATECH data based on the classification standard of SEMATECH and IBM [9]. We chose 450 μA as the limit here to catch passive I_{DDQ} defects and because data analysis showed that any limit between 8 and 1 μA gave nearly the same result of lowest defect level. In addition to this criterion, if we relax the pass/fail current threshold to 450 μA, we also found the following.

1) If the device band diagram looks like Fig. 5, with unclear bands, then even if the number of bands is less than 5, the device is bad with more than 99% certainty. These devices may have one or more resistive shorts of high resistance. Some vectors sensitize these shorts to current flow, by causing opposite potentials across the resistive short. The bands become unclear because different vectors sensitize different paths, which lead to various logic gates switching late in the clock period. This makes the bands smear and merge with each other.
2) If the band width is greater than 4 μA, then with >96% probability, the device is defective. The explanation of the band smearing (Case 1) applies here.
3) If multiple bands, such as in Fig. 2, part more than 5.0 μA, then it is >98% likely that the device is defective. This means that the shorts had lower resistance, so the difference in the current between a vector that sensitizes a resistive short and one that does not increases.
4) If just a few points are far apart from the majority band, say 3σ away from μ of the band, as in Fig. 3, then the device is >99% likely to be defective. The physical explanation of Case 3 may apply.
5) If the number of bands exceeds 4, (Fig. 6 has only four bands) then the device is 99% likely to be defective. The band differentiation algorithm in Fig. 7 determines the bands and the band width is the difference between the maximum and minimum measurements put in this band by the algorithm. In this case, there are more than just three resistive shorting paths in the chip, so more bands appear, indicating a defective device.

We now describe our new graphical I_{DDQ} test result classifier, which rejects chips based on the following features:

1) when there are *unclear bands* existing in the band diagram; this means that more than one group of data cluster, but the edges are not clear and obvious;
2) when the band width is greater than 3.5 μA or if the bands part by more than 5.1 μA;
3) when the number of bands exceeds 4;
4) when just a few obvious glitches are observed;

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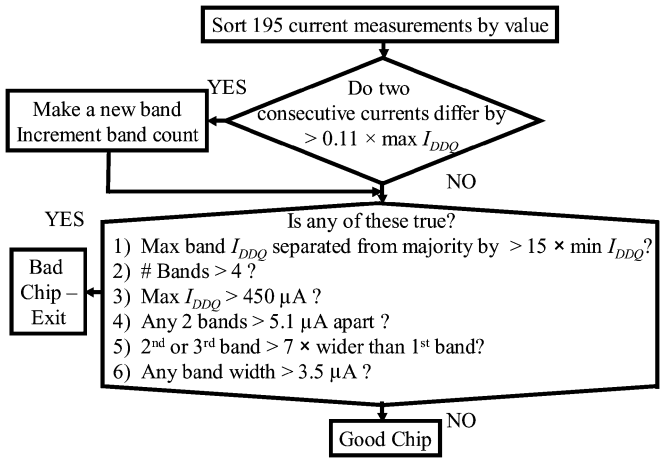

Fig. 7. Band differentiation algorithm.

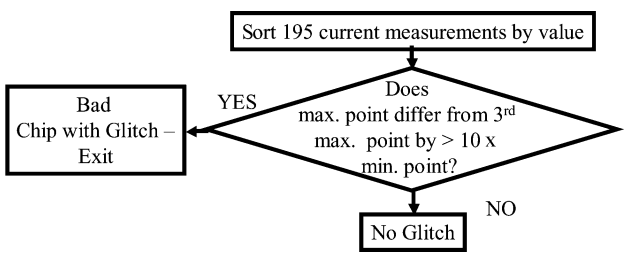

Fig. 8. Glitch detection algorithm.

5) when the second or third band is more than 2 times wider than the first (bottom) band.

The exact number of I_{DDQ} current measurements and the classifier parameters differ among designs because the I_{DDQ} current relates to the manufacturing technologies and the logic gate count of the DUT.

We now summarize the method as follows.

1) Analyze a representative sample of chips during current and voltage characterization, and calculate (with various tests) the number of bands, the band extents, the band separation, and the current glitch criteria for good chips to get a classification standard.
2) During manufacturing test, for each chip run the *band differentiation* (see Fig. 7) and *glitch detection* (see Fig. 8) algorithms and classify it as good or bad.

Based on these criteria and voltage tests, our method classified DUTs into the following six categories in Table II.

1) *Good Pass*: Those DUTs that passed all SEMATECH tests and also passed our evaluation.
2) *Good Fail*: Those DUTs that passed all SEMATECH tests but failed our evaluation.
3) *Bad Pass*: Those DUTs that failed some SEMATECH tests other than the I_{DDQ} test but passed our test.
4) *Bad Fail*: Those DUTs that failed some SEMATECH tests other than the I_{DDQ} test but also failed our test.
5) *Unknown Pass*: Those DUTs that only failed the SEMATECH I_{DDQ} test but passed our test.
6) *Unknown Fail*: Those DUTs that only failed the SEMATECH I_{DDQ} test and failed our test as well.

TABLE II
SEMATECH STATISTICS, TEST ESCAPES, AND YIELD LOSS

Category	Number	% Yield loss	% Test escapes	% Other
Total Reliable Functional Devices	11,858			
Total # of Unreliable Devices	5,576			
Unknown Devices	1,032			
Good Pass	11,719			98.83
Bad Pass	333		5.97	
Unknown Pass	153		14.83	
Good Fail	139	1.17		
Bad Fail	5,243			94.03
Unknown Fail	879			85.17

For multiple power domains, a mix of logic and memories and different mixtures of library cells (high leakage versus low leakage) in the DUT, we will segregate the V_{SS} bus used for I_{DDQ} measurements so that each domain has its own V_{SS} bus for I_{DDQ} test. Also, our classifier must be reparameterized when the fabrication process changes. We show in Section IX how the larger number of I_{DDQ} measurements required by our method is offset by a reduction in voltage tests.

V. RESULTS

No paper has given the total I_{DDQ} test statistics about the SEMATECH data except for the single threshold criterion. So we calculate results from Thibeault's ΔI_{DDQ} method [7] and from Gattiker *et al.*'s current difference method [3] for that data. Table III compares the various I_{DDQ} methods on the SEMATECH data, using three different I_{DDQ} thresholds. I_{DDQ} methods compared include the single-threshold, current difference, and two kinds of ΔI_{DDQ} methods. The first ΔI_{DDQ} method uses 4 μA as the pass fail threshold for the current difference of two consecutive vectors, instead of 4σ, because 4 μA gave a much better overkill rate. We also calculate the ΔI_{DDQ} method for 4σ, for comparison purposes, where σ is 0.35 μA, as given by Thibeault [7].

We tried these I_{DDQ} methods with three different ultimate thresholds, 8, 25, and 450 μA in Table III. Because the ultimate thresholds vary, the universe of chips changes. For the 8 μA column of the table, it is {11 824 good chips, 6520 bad chips, and 122 unknown chips}, for the 25 μA column, it is {11 843 good chips, 6137 bad chips, and 486 unknown chips} and for the 450 μA column it is the same as in Table I. The parameters for this experiment were a *noise ratio* of 0.11, a band separation limit of 5.1 μA, a limit of 4 bands, a single point glitch limit of 15 times the minimum I_{DDQ} value, a maximum band width of 3.5 μA, a band width variation limit of 7 times between bands, and a limit of 2 times the (maximum I_{DDQ} − third minimum I_{DDQ}/minimum I_{DDQ}). The noise ratio is the ratio of the ΔI_{DDQ} current to the maximum I_{DDQ} current. The threshold for the single I_{DDQ} threshold testing method is determined in a somewhat *ad hoc* way. Therefore, we want to see the robustness of these methods over different choices. Table III shows that the graphical I_{DDQ} testing method always achieves the best test coverage and second lowest overkill rate, just slightly higher than the ΔI_{DDQ}(4 μA) method. There are two reasons why, when the threshold decreases, the graphical I_{DDQ} test quality improves:

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TABLE III
COMPARISON OF TEST ESCAPE AND OVERKILL IN SEMATECH DATA

Method	Threshold $= 8\ \mu A$		Threshold $= 25\ \mu A$		Threshold $= 450\ \mu A$	
	Escape	Overkill	Escape	Overkill	Escape	Overkill
Single-Threshold	6.4%	1.60%	6.8%	2.2%	7.50%	2.3%
Current Difference	7.2%	5.90%	7.0%	6.0%	7.60%	6.1%
ΔI_{DDQ} (4 μA)	9.1%	0.74%	8.5%	0.9%	8.50%	1.0%
ΔI_{DDQ} (1.4 μA, $\sigma = 0.35\ \mu A$)	7.1%	6.70%	6.9%	6.9%	7.50%	7.0%
Graphical I_{DDQ}	5.0%	0.90%	5.4%	1.0%	5.97%	1.2%

TABLE IV
TEST VECTOR SET TRUNCATION RESULTS

Vector set (number of vectors)	# Devices		
	Good out of 11,858	Bad out of 5,576	I_{DDQ} only passing out of 1,032
# 1 (125)	11,711	5,229	167
# 1 + # 2 (135)	11,715	5,240	165
# 1 + # 3 (185)	11,715	5,235	154
# 1 + # 2 + # 3 (195)	11,719	5,243	153
Random (50)	11,657	5,152	222
Random (100)	11,726	5,168	176
Random (140)	11,735	5,209	172

TABLE V
0.8-μm CHIPS ESCAPING THE GRAPHICAL I_{DDQ} TEST AND PROBING ERROR STATISTICS

Kinds of failing tests	Count/ total of kind	Probe errors/ total
Stuck-at Only	10 / 10	8 / 8
Delay Fault Only	83 / 85	253 / 255
Functional Only	18 / 19	69 / 70
Functional and Delay Only	9 / 10	41 / 41
Stuck-at and Delay Only	49 / 53	1 / 1
Stuck-at and Single Threshold I_{DDQ}	0 / 48	0 / 0
Functional and Single Threshold I_{DDQ}	6 / 72	0 / 1
Functional and Stuck-at Only	48 / 49	29 / 29
Single Threshold I_{DDQ} and Delay	5 / 85	1 / 1
Other 3 Failed But Not Functional Test	3 / 1,234	0 / 0
Other 3 Failed But Not Delay Test	0 / 159	0 / 2
Other 3 Failed But Not I_{DDQ} Test	53 / 58	32 / 32
Other 3 Failed But Not Stuck-at Test	0 / 18	0 / 0
All Fail	1 / 3,040	0 / 0
Short Power Fail	10 / 17	0 / 0
Unknown Type (RR)	38 / 118	0 / 0
I_{DDQ}-only Fails	0 / 501	N/A
Total	333 / 5,075	434 / 440

some defective chips that escaped the test when using 450 μA now are declared defective by the lower threshold, so the test escape rate drops; also, some good chips that were overkilled by the 450 μA threshold standard now are declared good by the new classification standard, hence, the overkill rate drops as well. The ultimate I_{DDQ} threshold affects the overkill rate and must be set by accurate failure effect analysis down to the physical defect. We must minimize the overlap of the I_{DDQ}-pass set with the voltage test-fail set. Measurement errors are accounted for by the band width parameters.

A. I_{DDQ} Test Vector Selection

Since our goal is to use I_{DDQ} testing to reduce the use of other test methods, we analyze the effect of vector selection on I_{DDQ} defect detection. All four test methods, functional, delay, stuck-at fault, and single threshold I_{DDQ} test, clearly provide incomplete fault-coverage on the SEMATECH data. The I_{DDQ} fault models are: stuck-at, pseudo-stuck-at, bridging, and special faults. The bridging fault model is better than all others in detecting I_{DDQ} defects. No single model achieves complete fault coverage, so one should choose tests for all sorts of faults. The I_{DDQ} test vectors consist of the following:

1) 125 vectors created by IBM's I_{DDQ} test generator, which targets pseudo-stuck-at-faults (95.7% fault coverage) (set # 1);
2) ten vectors that applied simple, regular patterns into the scan chains (set # 2);
3) first 60 vectors of the stuck-fault tests (set # 3).

We experimented on a truncated set of test vectors (see Table IV, where explanations for the numbers of chips in the title row can be found in Table II). The ten vectors (set # 2) that applied simple, regular scan chain patterns are more effective than the 60 stuck-at faults (the longer set # 3) in catching defects, given the number of vectors added. We concluded that sets # 1 and # 2 are sufficient for testing. Randomly selecting test vectors does not work well here because of the information loss due to omitted vectors, but results show that increasing the number of randomly selected vectors improves test quality. The experiment shows that a better selection of current measurement vectors leads to lower defect level and low overkill rate.

B. Test Escapes

Table V, second column, gives the test escape distribution from the graphical I_{DDQ} test. The 434 chips in Table V, third column, failed various tests specified in column 1 at the wafer test stage but passed all tests applied at the package and burn-in test stages (note, however, that only a chosen subset of tests may have been applied). In column 3 of Table V, the denominators are the total number of chips in each category, while the numerators are the chips that were recovered by the graphical I_{DDQ} test. These chips should be defined as *probing errors*, which means that they are actually good chips, but were claimed by wafer tests to be defective. Some other chips have a similar phenomenon, but are real defective chips that self-healed. The difference is that healers also fail package stage tests.

Since the classification algorithm can still be improved, we also rechecked misjudged bad chips visually using Microsoft Excel. We found another 105 chips that can be visually classified as bad using the criteria given here, even though the previous algorithm classified them as good. Some bands are irregular even though they do not exceed the bandwidth or band separation limits. By irregular, we mean that the band was not flat, it had uneven density or the bandwidth changed along the band. Fig. 9 shows a typical bad chip with a sloped band, while Fig. 10 shows a chip with variable bandwidth. All of these chips were rejected

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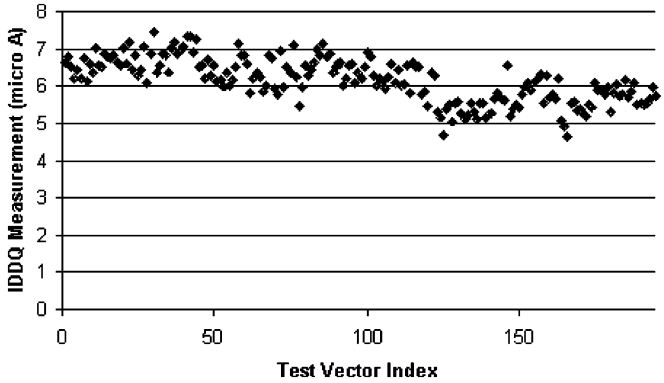

Fig. 9. Bad 0.8-μm chip with sloped current band.

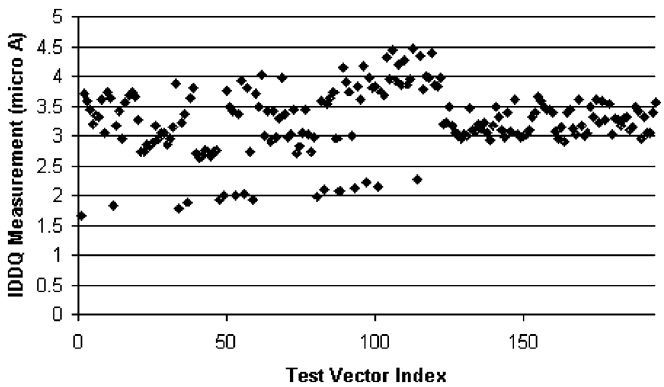

Fig. 10. Bad 0.8-μm chip with variable band width.

TABLE VI
COMPARISON OF EFFICIENCIES OF TEST METHODS

Kind of test method	% Defective chips detected	
I_{DDQ} threshold	8 μA	450 μA
IBM Functional Test	52.6%	65.0%
IBM Stuck-at Test	71.3%	83.4%
IBM Delay Test	70.3%	82.2%
IBM I_{DDQ} Test	93.6%	93.5%
Graphical I_{DDQ} Test	96.5%	95.9%
IBM (All Tests)	75.8%	88.6%

by sight classification. This additional classification would reduce the test escape percentage of the graphical test algorithm to 4.1%.

The efficiencies of all test methods and that of the graphical I_{DDQ} method are given in Table VI. In this table, we sight classified another 105 chips as defective in the graphical I_{DDQ} experiment for the 450 μA threshold, using the criteria of this classifier. This boosted the percentage of defective chips detected from 94.03% to 95.9%. For the experiment with a threshold of 8 μA, 99 chips were sight classified as defective, which brought the defective chip detection rate up to 96.5%. Obviously, the graphical method identifies more defective chips than other methods and has lower overkill because of the 434 chips that first were declared bad due to wafer probing errors but later turned out to be good.

VI. TRAINING SET SELECTION

To test the classifier quality, we experimented with training using samples, thus examining the effect of the sample size on the classifier quality. We adjusted the *noise ratio* of the classifier. Table VII shows results for training sets with 200, 400, and 800 samples. We also tried the classifiers on a verification vector set of the same size as the training set. The names of the sets have two numbers, e.g., 5000_200. Here the first number gives the position of the start chip of the training set in the SEMATECH data set. The second number gives the training set size. Hence, 5000_200 means the training set starts from the 5000th chip of the data set and has 200 samples.

TABLE VII
RESULTS OF TRAINING SETS

200 sample set	Escape rate		Overkill rate	
Training Set 0_200	3 /	63	0 /	125
Verification Set 5000_200	0 /	73	3 /	117
Entire Set	337 /	5,576	121 /	11,858
Training Set 5000_200	0 /	73	3 /	117
Verification Set 10000_200	9 /	61	4 /	131
Entire Set	337 /	5,576	121 /	11,858
Training Set 10000_200	9 /	61	4 /	131
Verification Set 15000_200	2 /	42	1 /	147
Entire Set	337 /	5,576	121 /	11,858
400 sample set	Escape rate		Overkill rate	
Training Set 0_400	4 /	132	1 /	249
Verification Set 5000_400	3 /	152	3 /	233
Entire Set	334 /	5,576	115 /	11,858
Training Set 5000_400	3 /	152	3 /	233
Verification Set 10000_400	20 /	124	5 /	259
Entire Set	336 /	5,576	116 /	11,858
800 sample set	Escape rate		Overkill rate	
Training Set 0_800	5 /	268	6 /	499
Verification Set 5000_800	6 /	263	6 /	499
Entire Set	337 /	5,576	121 /	11,858

The criterion for choosing the parameters of the classifier using the training set is to find the combination of the parameter set with the minimum test escape rate and the minimum overkill rate. From the table, the training set size does not affect the quality of the classifier much. But, the starting chip number is important to the classifier quality. Training set 0_200 gives a better classifier than training set 10000_200. There may be differences in the randomness of the two training sets.

VII. STATISTICAL SIGNIFICANCE OF DATA

To overcome the randomness problem, we need a statistically significant size for the training set. The classifier is a mixed *parametric-nonparametric* pattern recognizer [39]. It is nonparametric because we do not have density functions of the I_{DDQ} measurement band that can be characterized by a set of parameters to feature the classifier. It is parametric because some parameters, such as the bandwidth, the band separation, the noise level, etc., can be characterized by density functions. The discriminant features of the classifier are parameters, while the parameters that specify the density functions of the parameter set of the classifier are not parameterizable. Therefore, the estimation of the classifier is more complex than a simple parametric classifier or a nonparametric classifier. The classifier parameters must be estimated from available samples, so errors come from the classifier design errors, the sample errors, and measurement errors.

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We have two subsets of samples available: the defective chips (for the minimum test escape rate) and the defect-free chips (for the minimum overkill rate). To determine the sample size, we use the defective chips and assume that each is statistically independent of the others. Following Agrawal [40], [41], we use the following notation.

- N_p is the total number (population) of defective chips for which coverage is to be determined.
- C is the unknown but true fault coverage of the given test, $0 \leq C \leq 1$. This is the quantity being estimated.
- CN_p is the actual (but unknown) number of defective chips detectable by the given test.
- N_s is the number of randomly sampled chips from the set of N_p defective chips. $N_s \ll N_p$.
- c is the sample coverage, a random variable, $0 \leq c \leq 1$.
- x is the value of c determined from sampling, $0 \leq x \leq 1$.
- xN_s is the number of sampled defective chips detected by the given test. This is a known quantity.

The number of ways in which we can pick N_s chips from a population of N_p defective chips is

$$\text{Ways of obtaining sample of size } N_s = \binom{N_p}{N_s} = \frac{N_p!}{N_s!(N_p - N_s)!}. \quad (1)$$

The number of ways in which a sample with coverage x is possible is the product of the ways of sampling the detectable and undetectable fault subpopulations

$$\text{Ways of obtaining sample coverage } x = \binom{CN_p}{xN_s}\binom{(1-C)N_p}{(1-x)N_s}. \quad (2)$$

The probability of a fault sample giving a value x for c is obtained by dividing (2) by (1)

$$p(x) = \text{Prob}(\text{sample coverage}, c = x) = \frac{\binom{CN_p}{xN_s}\binom{(1-C)N_p}{(1-x)N_s}}{\binom{N_p}{N_s}}. \quad (3)$$

This is the hypergeometric probability density function of a discrete-valued random variable [42]. The random variable c can only take discrete values, $0, 1/N_s, 2/N_s, \ldots, 1$. When N_s is large, c can be treated as continuous and (3) is conveniently approximated by a *Gaussian probability density function* with mean C and variance σ^2[40]

$$p(x) = \text{Prob}(x \leq c \leq x + dx) = \frac{1}{\sigma\sqrt{2\pi}} e^{-((x-C)^2/2\sigma^2)}. \quad (4)$$

The variance of c is given by [40]

$$\sigma^2 = \frac{C(1-C)}{N_s}\left(1 - \frac{N_s}{N_p}\right). \quad (5)$$

The 3σ confidence range of the *normal* distribution gives the fault coverage. So for the 63 defective sample chips, the entire set of 18 466 chips and a fault coverage of 95.9%, the sample accuracy is $\pm 7.4\%$. For the 268 defective sample chips, the sample accuracy is $\pm 3.6\%$. To achieve $\pm 1\%$ accuracy, one needs 2910 samples. We care only about the representativeness of the sample and not the fault coverage estimate accuracy. So, the classifier parameterized from the sample set of size 268 is good. A sample set size of 63 defective chips is also good, but not statistically significant.

TABLE VIII
CHOICE OF THE FEATURE SET

Parameter name	# of parameters
Maximum I_{DDQ} Value	1
Number of Bands	1
Mean of Each Band	First 6 Bands
Standard Deviation of Each Band	First 6 Bands
Number of Points in Each Band	10
Separation of Each Band	First 5 Bands
Width of Each Band	First 6 Bands

VIII. Correlation Analysis of Graphical I_{DDQ} Testing Feature Set

Feature relevance analysis should be done to improve the classifier efficiency. The Pearson or product-moment *correlation* measures the degree of linear relationship between two variables, X and Y. The correlation coefficient sign $(+, -)$ defines the direction of the relationship and the absolute value measures the strength of the relationship. Correlation coefficients are represented as a *correlation matrix*. $\text{Var}[\,]$ denotes variance and $\text{Cov}[X, Y]$ is the covariance of X and Y having mean μx and μy, respectively. The correlation coefficient $\rho_{X,Y}$ of X and Y is

$$\text{Var}[X] = E[(X - \mu x)^2] \quad (6)$$

$$\text{Cov}[X, Y] = E[(X - \mu x)(Y - \mu y)] \quad (7)$$

$$\rho_{X,Y} = \frac{\text{Cov}[X, Y]}{\sqrt{\text{Var}[X]\text{Var}[Y]}}. \quad (8)$$

If two variables are strongly correlated, only one of them should be chosen in a classifier or the model will be *overfitted*. It is possible for two variables to be related (correlated), but not have one variable cause another (no *causation*). In this case, choosing only one of the two for the classifier is inappropriate because it is difficult for the classifier to achieve optimal quality, since the related variables cannot be set separately able to satisfy optimality.

A. Choice of Feature Set

The features utilized in graphical I_{DDQ} testing are: the number of bands, the bandwidth, the band separation, and the extreme points (noise). Here, we choose the 35 feature parameters in Table VIII.

We consider *efficient rank*. If a matrix is huge, but the eigenvalues differ greatly, then only those rows with relatively significant eigenvalues count. If a 5×5 matrix has the following eigenvalues:

$$\text{diag}[X] = [0.4436 \quad 0.0056 \quad 0.0007 \quad 0.0001 \quad 0.0000] \quad (9)$$

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TABLE IX
TEST TIME ESTIMATION FOR 0.8-μm CHIPS

Time	Conventional way	New way #1	New way #2	New way #3
Stuck-at Test	$8023 \times 1000 \times 400\ ns$	0	$8023 \times 1000 \times 400\ ns$	0
Setup Time	$100\ ms$	0	$100\ ms$	0
Delay Fault Test	$15232 \times 1000 \times 200\ ns$	$15232 \times 1000 \times 200\ ns$	$15232 \times 1000 \times 200\ ns$	0
Setup Time	$500\ ms$	$500\ ms$	$500\ ms$	0
Functional Test	$530000 \times 35\ ns$	$530000 \times 35\ ns$	0	0
Setup Time	$100\ ms$	$100\ ms$	0	0
I_{DDQ} Time	$20 \times 10\ ms$	$135 \times 10\ ms$	$135 \times 10\ ms$	$135 \times 10\ ms$
Setup Time	$100\ ms$	$100\ ms$	$100\ ms$	$100\ ms$
Wafer + Package	$\times 2$	$(Delay + Func.) \times 2 + GI$	$(Stuck + Delay) \times 2 + GI$	$\times 1$
Total	$14.55\ s$	$8.78\ s$	$15.16\ s$	$1.45\ s$

TABLE X
TEST ECONOMICS FOR 0.8-μm CHIPS

	Conventional way of testing	New way # 1	New way # 3
# Measurements	$8023(stuck) + 53K\ (functional)$ $+ 15232\ (delay) + 20\ (I_{DDQ})$	$135(I_{DDQ}) + 15232\ (delay)$ $+53K\ (functional)$	$135\ (I_{DDQ})$
Test Time	$14.55\ s$	$8.78\ s$	$1.45\ s$
Production Test Cost	$5\ cents/s \times 14.55\ s = \$0.728$	$5\ cents/s \times 8.78\ s = \$0.439$	$5\ cents/s \times 2.9\ s = \$0.145$
% Cost Savings	0%	40.0%	80.1%
% Defective Chips	97.6%	99.0%	95.9%
Pattern Generation	Difficult	Simpler	Much simpler
Chip Classification	Complex	Complex	Complex

then the efficient rank of this matrix is 1, since the second largest eigenvalue is less than a tenth of the largest one. The effect of the columns (rows) with smaller eigenvalues is negligible.

B. Feature Correlation Analysis of all SEMATECH Chips

The entire SEMATECH data set is analyzed first. By calculating the efficient rank of the 35×35 feature matrix from Table VIII, only the following 13 features are efficient:

1) maximum I_{DDQ} current;
2) μ's of the first, second, third, and fourth bands;
3) σ's of the widths of the first and second bands;
4) numbers of points in the first and second bands;
5) band separation of the first two bands;
6) widths of the first, second, and third bands.

The correlation coefficient matrix of these 13 features from the entire SEMATECH data was computed. Some features such as μ or σ of the bandwidth strongly correlate with the band width (0.4850, 0.9751). The maximum I_{DDQ} value strongly correlates with the μ of the first band (0.4741), the σ of the width of the second band (-0.5786), and the number of points in the second band (0.7691) since a majority of chips have only one or two bands. But, one cannot eliminate these features, which give information about noise. For example, the spread of a band may be caused by measurement noise, but measurement noise is not necessarily the cause of the band width, as there may be defect-induced noise.

C. Feature Correlation Analysis of SEMATECH Good Chips

From the efficient rank of the 35×35 feature matrix in Table VIII of the good chip data set, only the following 10 features are efficient:

1) maximum I_{DDQ} current;
2) number of bands;
3) μ's of the first, second, and third bands;
4) σ's of the widths of the first and second bands;
5) number of points in the first band;
6) band separation of the first two bands;
7) width of the first band.

The correlation coefficient matrix of these 10 features from the good chip SEMATECH data was computed. The strong correlations among those features in the last subsection are caused by noise, since the largest correlation is -0.2012 in the good data set. So, the choice of feature set for graphical I_{DDQ} testing is sound, but a parametric classifier would not be proper for graphical I_{DDQ} testing, because of the strong correlations among some features. Hence, linear discriminator, quadratic discriminator, and logistic regression analysis should not be used here. The classifier discussed here is a decision tree method. It is a hybrid parametric and nonparametric one, which reduces the influence of strongly correlated features.

IX. TEST ECONOMICS

To achieve better test economics, we propose several new ways to utilize the graphical I_{DDQ} testing method. Conventional testing uses scan-chain stuck-at fault, functional, delay, and single threshold I_{DDQ} tests with only 10-20 I_{DDQ} measurements. In the SEMATECH case in Table IX, the number of chips that failed only stuck-at voltage tests is only 10 out of 18 466, so we consider eliminating these time-consuming voltage tests. In New way # 1, we discard the scan chain stuck-at fault test and use the graphical I_{DDQ} test with 135 I_{DDQ} test patterns instead of the single threshold I_{DDQ} test. In New way # 2, the functional test is discarded to reduce test time and cost. The delay test cannot be removed, since the number of delay faults that escape the graphical I_{DDQ} test is relatively large. In New way # 3, all voltage tests are discarded and only the graphical I_{DDQ} test is used. Table X gives the estimation of the total test time required for each way. New way # 1 uses less test time than the Conventional way, New way # 2 uses more test time and New way # 3 uses only one tenth of the test time of the Conventional way. In

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New way # 1, with less test time, we found 1.4% more defective chips than the Conventional way. So, the Conventional way has a defect level of $2.4\% \times 5576 \times 1\,000\,000 \div 18\,466 = 7247$ defective chips per million, but New way # 1 has a defect level of $1.0\% \times 5576 \times 1\,000\,000 \div 18\,466 = 3020$ defective chips per million. New way # 3 has a high defect level, but it only uses one-tenth of the conventional test time and test pattern generation is much simpler.

The classifier for this method was augmented with sight classification of additional chips as defective. Sight classification boosted the defect coverage of New way # 3 from 94.1% to 95.9%, due to 105 additional chips classified as defective. Better I_{DDQ} test patterns would improve the graphical I_{DDQ} test quality even further [43].

X. Conclusion

We have proposed a new graphical I_{DDQ} current signature, where we plot all I_{DDQ} measurements as a waveform and accept or reject chips based on the noise in this waveform. This method can catch some defects that other I_{DDQ} tests cannot. This graphical I_{DDQ} test may substantially reduce the number of conventional voltage tests. This method has a slightly higher overkill rate of 1.2%, compared to the ΔI_{DDQ} method with an enlarged threshold of 4 μA. It is not clear whether these losses are really losses, since the tests are incomplete. On the other hand, this method can correct for a majority of the probing errors during wafer test to reduce the overkill rate.

We clearly defined the device classes and did extensive experiments on the IBM SEMATECH data. The results showed promising signs that I_{DDQ} testing can still survive through DSM technology because this method does not relate results of I_{DDQ} testing to absolute current measurements, but rather to the shape of the series of measurements. Statistical significance analysis is also provided. Lu *et al.* [32] calculated the leakage current caused by faults for DSM chips until year 2011 and found that the leakage current would still scale beyond the nondefective leakage current.

The graphical method computational complexity is $O(n \log n)$ for $n =$ number of current measurements, since the most computation-intensive part is sorting. The classifier can be implemented on an existing *automatic test equipment*.

This method gives clearer insight and more realistic criteria, hence it can catch more faults, i.e., it has a lower defect level. It also allows multiple bands to exist in I_{DDQ} measurements of good chips and since it does not depend on absolute values of current measurements, the faulty information introduced by erroneous probing is eliminated. Hence, the overkill rate is reduced at the same time as the defect level by this method.

Further research can be done on DSM technologies using test vectors generated from multiple fault models, and physical diagnosis needs to be done on those devices that caused yield loss. More features of defective devices need to be found for the I_{DDQ} test to replace other tests.

Acknowledgment

The authors would like to thank Dr. P. Nigh and the IBM Corporation for giving them access to the data from the SEMATECH experiment. Their generosity made this work possible.

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