Panel: INCREASING TEST COVERAGE IN A VLSI DESIGN COURSE

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VLSI Design is a popular course in the computer engineering (CE) curriculum at most universities. The course is usually so packed with the material on design that little or no time is left for testing. With the exception of a handful of universities, most others do not offer a separate course on test. Even if a course on test is offered, it can rarely be included in an undergraduate curriculum, which is already overloaded with "essential" courses. Thus, most CE students graduate with just a VLSI Design course.

The National Science Foundation (NSF) held a workshop in 1998 to discuss the future of research and education in test. Several panelists participated in that workshop. The present level of "test coverage" in the CE education was found to be inadequate. A possible remedy suggested was to enhance test in the VLSI Design course.

All panelists from academia have taught VLSI Design course and there is an almost 50-50 balance between the design and test-oriented professors. In addition, a VLSI design manager represents the industry on the panel. They will present their views on: (a) how much testing (1, 2, 3 or more lectures) should be included in a VLSI Design course, and (b) given the limited time in a one-semester course, what topics on test should be included. Audience participation will be sought in deciding what makes a "well-rounded" CE graduate. Panelists will outline:

- Their experience with VLSI Design course – number of lectures on test and topics included. The industry panelist will outline the required "basic" and the desirable "advanced" skills of a new graduate.
- Any proposed changes in the course based on the experience.

The panel will then debate the need for and the means of enhancing the "test coverage" of a VLSI Design Course.

PANELISTS

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