

Designing Variation-Tolerance in Mixed-Signal Components of a System-on-Chip

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Abstract—Nanoscale system-on-chip (SoC) devices offer potential for higher performance and reduced power consumption at lower cost. However yield and reliability of mixed-signal components in such devices become serious issues due to process variability. In this paper, we discuss a novel variation-tolerant technique for non-linearity errors in self-correctable mixed-signal components. We propose a completely digital method of test and correction of digital-to-analog and analog-to-digital converters (DAC/ADC) using a digital signal processor (DSP) assumed to be available on the SoC. The added hardware includes a first-order sigma-delta ADC for measurement and a low-resolution dithering DAC for correction of output. The DSP handles test pattern generation (TPG) and output response analysis (ORA) and a third-order polynomial fitting algorithm is employed to characterize the nonlinearity error. Simulation results demonstrate a reduction in non-linearity errors of converters from $\pm 1.5\text{LSB}$ down to $\pm 0.5\text{LSB}$. Our technique can also be applied to other mixed-signal devices with digital control.

I. INTRODUCTION

In recent decades, rapid advances in integrated circuit (IC) technology have led semiconductor industry into the manufacture of nanoscale (65nm and smaller feature) devices. As feature size on an IC chip shrinks, the performance improves and power consumption reduces. Consequently, we can integrate more components and build more capable SoCs at lower cost. However, scaling down SoCs to nanoscale also brings new problems. Along with the increasing difficulties in manufacturing and testing of nanoscale devices, parameter variations of individual devices during the fabrication process become a critical factor for die yield, system reliability and eventually manufacturing cost. As downscaling in CMOS technologies will continue at least to 22nm, one of the difficult challenges in the near-term will be to deal with fluctuations and statistical process variation affecting the sub-11 nm gate length MOSFET [1]. When the feature size of nanoscale devices approaches the physical limits, the device parameters become more difficult to control. This would limit further

feature size reduction, performance improvement and cost reduction.

Mixed-signal components are affected by such process variations and are more susceptible to parametric faults than digital circuits [2]. These faults may cause deviations of device parameters beyond specified tolerance limits and seriously degrade system performance. DAC and ADC are critical mixed-signal components, requiring higher resolution and better performance. They generally have increased fault rate and therefore lower yields due to parametric variations.

In this paper, we present a novel process variation-tolerant technique for post-fabrication fault detection, parameter characterization and at-speed output correction for non-linearity errors of on-chip DAC/ADCs in SoCs. Newly added components include a first-order 1-bit sigma-delta modulator, a digital filter, two digital polynomial evaluation units and a low-resolution dithering DAC plus some additional memory cells. DSP is used for test control, device characterization and parameters extraction. The DSP-based technique generally consists of two phases, initially testing and then correcting. During testing phase, non-linearity errors of series of consecutive ramp code are examined and converters are characterized by DSP. If these measured non-linearity errors are all within the specified range of correction, the converters will be considered correctable. During correcting phase, the evaluation units and dithering DAC are used to regenerate those non-linearity errors for output correction. The error in DAC is measured and corrected first and then that DAC is used to test and calibrate the ADC.

This technique can also be applied to other mixed-signal devices with digital control input. DSP would be used to generate test patterns, analyze responses, and assess parameter errors. That information will in turn be employed to control additional correction hardware to fix the erroneous outputs of the device under test. Such corrections and fixes will eliminate many parametric faults caused by process variations and make devices more variation-tolerant.

II. BIST ARCHITECTURE FOR MIXED-SIGNAL SOC

For digital circuits, built-in self-test (BIST) technique has been widely studied. The conventional digital BIST circuitry [6] consists of a test pattern generator (TPG), an output response analyzer (ORA), and possibly a digital signal processor (DSP) as BIST controller. Mixed-signal BIST architecture has a similar structure. DAC and ADC are commonly used as interfaces between digital and analog circuitry. Digital test patterns from TPG go through the DAC to analog functional circuit whose response then goes through the ADC to be converted back to digital response for the ORA. This is shown in Figure 1.

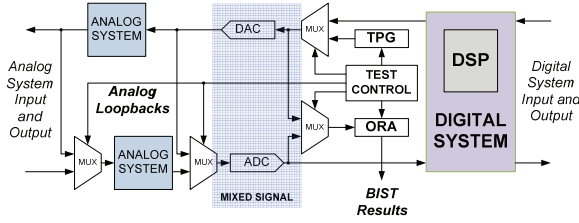


Figure 1 Typical mixed-signal BIST architecture [3].

Three loopbacks (two analog and one digital) are used for each part of the system to test analog circuitry, DAC/ADC, and TPG/ORA themselves, respectively. These loopbacks, activated through four MUXs, are disabled after BIST. DAC and ADC are essential for this mixed-signal BIST architecture. Parameters of the converters, such as linearity, converting speed and frequency response, will seriously affect performance of the mixed-signal system.

In the typical mixed-signal BIST architecture shown in Figure 1, DAC and ADC are both tested through one analog loopback with the other two loops disabled. Test patterns from TPG are converted by DAC to analog signals and then sampled by ADC as digital output for response analysis by ORA. ORA unit analyzes the output response to detect faults and determine BIST results for DAC/ADC. However, this method is incapable of fixing detected faults of DAC/ADC, especially the parametric faults. Otherwise, any minor parameter deviation of converters may make the whole mixed-signal system 'faulty' because of non-linearity errors.

III. VARIATION-TOLERANT DESIGN OF DAC AND ADC

DAC/ADC must be process variation-tolerant to reduce parametric faults. With the proposed BIST technique, non-linearity errors can be detected, characterized and fixed by additional correcting elements.

A. Main Ideas

Non-linearity errors are measured as differential non-linearity (DNL) and integral non-linearity (INL). Assuming digital code k and corresponding analog value v_k , we get

$$DNL_k = \frac{v_k - v_{k-1}}{LSB} - 1 \quad (1)$$

$$INL_k = \sum_{i=1}^k DNL_i = \frac{v_k - v_0}{LSB} - k$$

where least significant bit (LSB) is the minimal measurement value for DAC/ADC. INL errors are the differences between ideal outputs and real outputs of converters. Maximum INL determines the quality of converters. If any of INL is greater than ± 0.5 LSB, the converter is marked as faulty.

To eliminate such faults, one straightforward solution is to store all measured INL errors for every digital code during BIST and then add correction signals to converter outputs, removing all INL errors during the normal operation. However, no device is capable of exhaustively storing a large number of INL errors.

B. Third-order Polynomial Fitting Algorithm

A simplified polynomial fitting algorithm [7] has been proposed for characterizing DAC/ADC outputs. The third-order fitting algorithm can also be used for fitting INL errors, reducing the memory requirement by storing only four coefficients. General form of the third-order polynomial is

$$y = b_0 + b_1 \cdot x + b_2 \cdot x^2 + b_3 \cdot x^3 \quad (2)$$

where b_0 , b_1 , b_2 and b_3 are the coefficients. To calculate coefficients, the complete range of DAC/ADC output is divided into four equal-length sections, and sum of each section is defined as

$$S_i \Big|_{i=0,1,2,3} = \sum_{k=iN/4}^{(i+1)N/4} v_k \quad (3)$$

where N is the number of bits of DAC/ADC. Four syndromes are determined as linear combinations of the sums and the four coefficients are obtained from these syndromes,

$$\begin{aligned} B_0 &= S_3 + S_2 + S_1 + S_0 \\ B_1 &= S_3 + S_2 - S_1 - S_0 \\ B_2 &= S_3 - S_2 - S_1 + S_0 \\ B_3 &= S_3 - 3S_2 + 3S_1 - S_0 \end{aligned} \Rightarrow \begin{aligned} b_0 &= \frac{1}{n} \left(B_0 - \frac{4}{3} B_2 \right) \\ b_2 &= \frac{4}{Nn} \left(B_1 - \frac{4}{3} B_3 \right) \\ b_2 &= \frac{16}{n^3} B_2 \\ b_3 &= \frac{128}{3n^4} B_3 \end{aligned} \quad (4)$$

where n is the complete range of converter ($n=2^N$). The coefficients can also be used as measurement for the characteristics of the converter:

$$\begin{aligned} \text{offset} &\propto B_0 & \text{gain} &\propto B_1 \\ 2^{\text{nd}} \text{ harmonic} &\propto B_2 & 3^{\text{rd}} \text{ harmonic} &\propto B_3 \end{aligned} \quad (5)$$

With the fitting algorithm, no individual INL error needs to be stored, provided the four coefficients of third-order fitting polynomial are saved. The estimation value is sufficient for converter output correction because the objective of such a correction is to reduce INL error to within ± 0.5 LSB range.

C. Variation-Tolerant Design of DAC

In the testing phase, DAC is first tested and characterized by the DSP controller. As shown in Figure 2, a low-speed ADC (m-ADC) consisting of a first-order 1-bit sigma-delta modulator and digital filter (generally a low-pass filter, e.g., an integrator in this case) is used to measure on-chip DAC-under-test (DUT) outputs. The first-order sigma-delta modulator is used because it has high linearity and reliability given a large enough oversampling ratio (OSR) [5]. An analog loopback between DUT and m-ADC is established in this step to transmit DAC output signals.

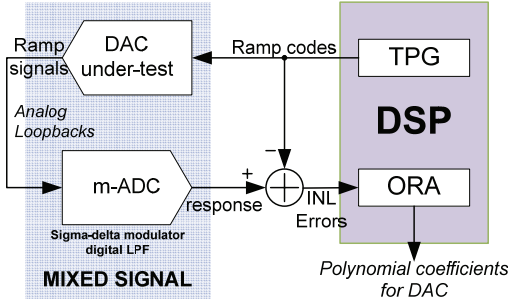


Figure 2 Test of on-chip DAC-under-test (DUT).

A series of consecutive ramp codes (k), ranging from the smallest to largest values, are generated by TPG for DAC test. The ideal outputs (v_k) of DAC are analog ramp signals. The actual outputs (v_k') of DAC are sampled by the sigma-delta modulator and transformed by the low-pass digital filter into digital codes (k'). The difference ($\Delta v_k = v_k - v_k'$) between ideal and actual outputs is the total INL error of both DUT and m-ADC. The difference values ($\Delta k = k - k'$) of TPG output code and m-ADC output code is in fact the digitized INL error of DUT and m-ADC. If effective number of bits (ENOB) of m-ADC is high enough, the INL error of m-ADC can be ignored and the difference value (Δk) will then be the digitalized INL error of DUT only.

After obtaining all digitized INL errors of DUT, DSP control unit will be able to calculate four polynomial coefficients using the third-order polynomial fitting algorithm. Four syndromes will also be used to determine characteristics of DUT and to mark DUT as faulty if any of them goes beyond the specified fitting range, which means the DUT is not correctable by the fitting polynomial.

These four characteristics data are stored in a polynomial evaluation unit (PE) by DSP and will be used to generate a digital correction value for each input code of DUT during the test of ADC as well as during the normal system operation. PE drives a low-cost low-resolution dithering DAC (d-DAC) to produce analog correction signals for DUT outputs, as shown in Figure 3. The supplied voltage of d-DAC (V_{REF}) is determined by the specified fault tolerance factor K , as shown below.

$$\left| V'_{REF} \right| = K \cdot V_{REF} \cdot 2^{-N} \quad (6)$$

where V_{REF} is the reference voltage of N -bit DAC. In ideal condition, the correction step effectively removes INL errors

from combined outputs of DUT and d-DAC. The final analog outputs could be considered ideal and on-chip DAC with given non-linearity range is variation-tolerant.

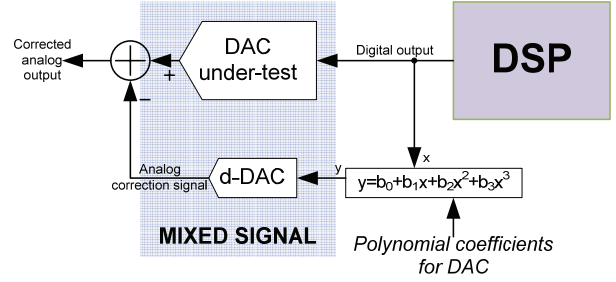


Figure 3 Output correction of on-chip DAC.

Considering that d-DAC may have non-linearity, the corrected outputs of DUT would not be ideal. Most of INL errors will be removed but some minor errors will still exist. The minimal resolution of d-DAC can be determined to ensure the INL errors below 0.5 LSB, as follows

$$\hat{N} > \log_2 \left(\frac{2^{2K}}{0.5} \right) = 2K + 1 \quad (7)$$

The minimal ENOB of m-ADC to detect tolerable faults can also be determined as

$$N' \geq N + \hat{N} - 2K \geq N + 1 \quad (8)$$

for N -bit DAC-under-test with variation-tolerance factor K .

Therefore, the minimum required OSR of the sigma-delta modulator in m-ADC can be calculated [4].

D. Variation-Tolerant Design of ADC

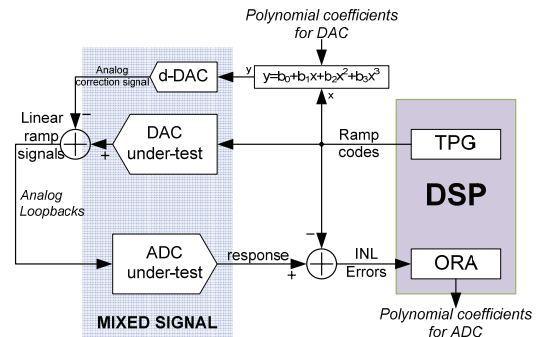


Figure 4 Test of on-chip ADC-under-test (AUT).

After correcting the on-chip DAC outputs by removing non-linearity errors by d-DAC, the final outputs of DAC can be considered very close to being ideal. This DAC can now be used to generate linear analog signals to test and diagnose the on-chip ADC, as shown in Figure 4.

In this second step of the test phase, an analog loopback is established between DAC output and the on-chip ADC-under-test (AUT). The loopback between DAC output and m-DAC used during DAC test is now disabled. TPG generates another series of consecutive ramp codes (k) which are in turn

