

V-Transform: An Enhanced Polynomial Coefficient Based DC Test for Non-Linear Analog Circuits

Suraj Sindia
Centre for Electronic
Design and Technology
Indian Institute of Science
Bangalore, India
Email: ssuraj@cedt.iisc.ernet.in

Virendra Singh
Supercomputer Education
and Research Centre
Indian Institute of Science
Bangalore, India
Email: viren@serc.iisc.ernet.in

Vishwani Agrawal
Department of Electrical
and Computer Engineering
Auburn University
Alabama, AL, USA
Email: vagrawal@eng.auburn.edu

Abstract—DC testing of parametric faults in non-linear analog circuits based on a new transformation, entitled, *V-Transform* acting on polynomial coefficient expansion of the circuit function is presented. *V-Transform* serves the dual purpose of monotonizing polynomial coefficients of circuit function expansion and increasing the sensitivity of these coefficients to circuit parameters. The sensitivity of *V-Transform* Coefficients (VTC) to circuit parameters is up to 3x-5x more than sensitivity of polynomial coefficients. As a case study, we consider a benchmark elliptic filter to validate our method. The technique is shown to uncover hitherto untestable parametric faults whose sizes are smaller than 10% of the nominal values.

I. INTRODUCTION

Non-linear circuit testing has been researched and different methods have been proposed for finding parametric faults [1], [2], [3], [4], [5], [6], [7], [8]. Prominent among them in the industry is the I_{DDQ} based testing where current from the supply rail is monitored and sizable deviation from its quiescent value is reported. However this requires augmentation of the CUT. For example, in the simplest case a regulator supplying power to any sizable circuit has to be augmented with a current sensing resistor and an ADC (for digital output) and then there is subsequent analysis to be performed on sensed current. Further I_{DDQ} is suitable only for catastrophic faults as the current drawn from the supply is distinguishable only when there is some “big enough” fault so as to change the current drawn from the supply from its quiescent value to a region where it is distinguishable. For example with resistor R_2 being open in Figure 1, the current drawn from supply can change by 50% of its quiescent value. Such faults can typically be found by monitoring I_{DDQ} using a current sensor. However parametric deviations say lesser than 10% from its nominal value cannot be observed using this scheme, specially so in the deep submicron era where the leakage currents can be comparable with defect induced current [9]. It is therefore interesting to develop a method to detect parametric faults while DC testing with lesser circuit augmentation.

To address the issue of parametric deviation, we would typically need more observables to have an idea about the parametric drift in circuit parameters. This would mean an increase in complexity of the sensing circuit. However, we would also want only little augmentation to tap any of the internal circuit nodes or currents. To overcome these seemingly contrasting requirements the method intended should have some way of “seeing through” the circuit with only the outputs and inputs at its disposal. References [10], [11] have accomplished this sort of a strategy for linear circuits in a different context as described next.

Savir and Guo describe a method [10] based on transfer function description of CUT. The transfer function, $H(s)$, of the CUT is expressed as in (1):

$$H(s) = \frac{\sum_{i=0}^M a_i s^i}{\sum_{i=0}^N b_i s^i} \quad (M < N) \quad (1)$$

Here, a_i and b_i are referred to as transfer function coefficients (TFCs). The CUT is subjected to frequency rich input signals and the output at these frequencies is observed. With these input-output pairs they estimate the TFCs of CUT. These coefficients are now compared with the ideal circuit TFCs, which are known a priori. The CUT is classified faulty if any of the estimated coefficients are beyond the tolerable range. This method necessarily needs the CUT to be linear, as transfer functions are possible only for LTI systems.

To extend the above idea to more general non-linear circuits we adopted a strategy in [12] where we expand the function of the circuit as a polynomial by the Taylor’s series expansion about the input voltage $v_{in} = 0$ as follows:

$$v_{out} = f(v_{in}) = f(0) + \frac{f'(0)}{1!} v_{in} + \frac{f''(0)}{2!} v_{in}^2 + \frac{f'''(0)}{3!} v_{in}^3 + \dots + \frac{f^{(n)}(0)}{n!} v_{in}^n + \dots \quad (2)$$

where $f(x)$ is a real function x . Ignoring the higher order terms in (2), we can expand v_{out} up to the n^{th} power of v_{in} , which gives us the approximation in (3):

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + \dots + a_n v_{in}^n \quad (3)$$

where $a_0, a_1, a_2, \dots, a_n$ are all real-valued functions of circuit parameters $p_k \forall k$. Further assume that normal parameter variations (normal drift) in a good circuit are within a fraction α of their nominal value, where $\alpha \ll 1$. This means that every parameter p_i is allowed to vary within the range $p_{k,nom}(1-\alpha) < p_k < p_{k,nom}(1+\alpha) \forall k$, where $p_{k,nom}$ is the nominal value of parameter p_k . Whenever one or more of the coefficient values slip outside its individual hyper-cube we get a different set of coefficients that reflects a detectable fault. Therefore, equation (4) describes a hypercube for all parameters that correspond to either good machine values or undetectable parameter faults [10], [2], [8]:

$$a_{i,\min} < a_i < a_{i,\max} \quad \forall a_i, 0 \leq i \leq n \quad (4)$$

This paper is organized as follows. Section II deals with the analysis of the nature of coefficients resulting from polynomial expansion of function $f(v_{in})$ and notions of detectable fault sizes of parameters. Section III outlines *V-Transform* and the resulting sensitivity improvement. In Section IV we describe the problem at hand and discuss the proposed solution with an example. In Section V we generalize the solution to an arbitrarily large circuit. Section VI presents the simulation results for some standard circuits. We conclude in section VII.

II. PRELIMINARIES

The coefficients $a_i \forall 0 \leq i \leq n$ are in general non-linear functions of circuit parameters $p_k \forall k$. The rationale in using these coefficients as metrics in classifying CUT as faulty or fault free is based on the premise of dependence of coefficients on circuit parameters.

A. Analysis of Polynomial Coefficients

Theorem 1. If coefficient a_i is a monotonic function of all parameters, then a_i takes its limit (maximum and minimum) values when at least one or more of the parameters are at the boundaries of their individual hypercube.

Lemma 1. If coefficient a_i is a non-monotonic function of one or more circuit parameters p_i , then a_i can take its limit values anywhere inside the hypercube enclosing the parameters.

By Theorem 1 and Lemma 1 it is clear that by exhaustively searching the space in the hypercube of each parameter we can get the maximum and minimum values of the polynomial coefficient. Typically this can be formulated as a non-linear optimization problem to find the maximum and minimum values of coefficient with constraints on parameters allowing only a normal drift.

Theorem 2. In polynomial expansion of Non-Linear Analog circuit there exists at least one coefficient that is a monotonic function of all the circuit parameters.

In conclusion, from Lemma 1 and Theorem 2, circuit parameter deviations have a bearing on coefficients and the monotonically varying coefficients can be used to detect parametric faults of the circuit parameters. We have proved theorems 1 and 2 in our previous paper [12].

B. Definitions

Definition 1: A minimum size detectable fault, MSDF ρ , of a parameter is defined as the minimum fractional deviation of the circuit parameter from its nominal value for it to be detectable with all other parameters held at their nominal values. The fractional deviation can be positive or negative and is named upside-MSDF (UMSDF) or downside-MSDF (DMSDF) accordingly.

Definition 2: A nearly minimum size detectable fault, or NMSDF ρ^* , of a parameter is defined as some fractional deviation of the circuit parameter from its nominal value, with all the other parameters being held at their nominal values, that is close to its MSDF with an infinitesimally small error, ϵ . Thus,

$$\epsilon = |\rho - \rho^*| \quad \epsilon \ll 1 \quad (5)$$

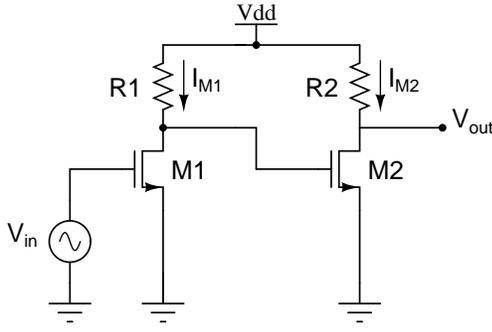


Fig. 1. Cascaded amplifier.

NMSDF also has notions of upside and downside as in case of MSDF. In (5), ϵ can be perceived as a coefficient of uncertainty about the MSDF of a parameter. If ψ is the set of all coefficient values spanned by the parameters while varying within their normal drifts, i.e.,

$$\psi = \{v_0, v_1, \dots, v_n \mid v_0 \in A_0, v_1 \in A_1, \dots, v_n \in A_n\} \\ \forall_k \quad p_{k, nom}(1 - \alpha) < p_k < p_{k, nom}(1 + \alpha)$$

then by definitions 1 and 2, ψ includes all possible values of coefficients that are not detectable. Any parametric fault inducing coefficient value outside the set ψ will result in a detectable fault.

III. V-TRANSFORM

Let us define V-Transform coefficients as follows: if $C_1, C_2 \dots C_n$ are polynomial coefficients of CUT then their V-Transform coefficients denoted by $V_{C_1}, V_{C_2} \dots V_{C_n}$ are given by

$$V_{C_i} = e^{\gamma C'_i} \quad \forall 0 \leq i \leq n \quad (6)$$

where C'_i are the modified polynomial coefficients defined indirectly as follows

$$\frac{dC'_i}{dp_j} = \left| \frac{dC_i}{dp_j} \right| \quad \forall 0 \leq i \leq n \quad (7)$$

The definition of C'_i as in (7) ensures that these modified polynomial coefficients are monotonic with the polynomial coefficients. Further, the V-Transform coefficients (VTC) are defined as exponential functions of these modified polynomial coefficients. γ is a sensitivity parameter which can be chosen according to the desired sensitivity. The gain in sensitivity of V-Transform coefficients to circuit parameters over the sensitivity of ordinary polynomial coefficients is given by

$$\frac{S_{p_i}^{V_{C_i}}}{S_{p_i}^{C_i}} = \frac{\left| \frac{dC'_i}{dp_i} \right| \gamma e^{\gamma C'_i} \cdot \frac{p_i}{e^{\gamma C'_i}}}{\frac{dC_i}{dp_i} \cdot \frac{p_i}{C_i}} = \gamma C_i \quad (8)$$

IV. PROBLEM AND APPROACH

We shall first illustrate with an example the calculation of limits of the polynomial coefficients for a simple circuit using MOS transistors. We shall follow this up with MSDF values for the circuit parameters.

Example 1. Two stage amplifier Consider the cascaded amplifier shown in Figure 1. The output voltage V_{out} in terms of input voltage results in a fourth degree polynomial equation as in (9).

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + a_4 v_{in}^4 \quad (9)$$

Where the constants a_0, a_1, a_2, a_3 are defined symbolically in (10) for M1 and M2 operating in saturation region. Nominal values of $V_{DD}=1.2V, V_T=400mV, \left(\frac{W}{L}\right)_1 = \frac{1}{2} \left(\frac{W}{L}\right)_2 = 20$, and $K = 100\mu A/V^2$ are substituted to get coefficients in terms of parameters R_1 and R_2 as stated in (11).

TABLE I
MSDF FOR CASCADED AMPLIFIER OF FIGURE 1 WITH $\alpha = 0.05$.

Circuit parameter	%upside MSDF	%downside MSDF
Resistor R_1	10.3	7.4
Resistor R_2	12.3	8.5

$$a_0 = V_{DD} - R_2 K \left(\frac{W}{L}\right)_2 \left\{ \begin{array}{l} (V_{DD} - V_T)^2 + \\ R_1^2 K^2 \left(\frac{W}{L}\right)_1^2 V_T^4 - \\ 2(V_{DD} - V_T) R_1 \left(\frac{W}{L}\right)_1 V_T^2 \end{array} \right\}$$

$$a_1 = R_2 K \left(\frac{W}{L}\right)_2 \left\{ \begin{array}{l} 4R_1^2 K^2 \left(\frac{W}{L}\right)_1^2 V_T^3 \\ + 2(V_{DD} - V_T) R_1 K \left(\frac{W}{L}\right)_1 V_T \end{array} \right\} \quad (10)$$

$$a_2 = R_2 K \left(\frac{W}{L}\right)_2 \left\{ \begin{array}{l} 2(V_{DD} - V_T) R_1 K \left(\frac{W}{L}\right)_1 \\ - 6R_1^2 K^2 \left(\frac{W}{L}\right)_1^2 V_T^2 \end{array} \right\}$$

$$a_3 = 4V_T K^3 \left(\frac{W}{L}\right)_1^2 \left(\frac{W}{L}\right)_2^2 R_1^2 R_2$$

$$a_4 = -K^3 \left(\frac{W}{L}\right)_1^2 \left(\frac{W}{L}\right)_2^2 R_1^2 R_2$$

$$a_0 = 1.2 - R_2 \left(\begin{array}{l} 2.56 \times 10^{-3} + 1.024 \times 10^{-7} R_1^2 \\ - 5.12 \times 10^{-4} R_1 \end{array} \right)$$

$$a_1 = 4.096 \times 10^{-9} R_1^2 R_2 + 5.12 \times 10^{-6} R_1 R_2$$

$$a_2 = 1.28 \times 10^{-5} R_1 R_2 - 1.536 \times 10^{-8} R_1^2 R_2 \quad (11)$$

$$a_3 = 2.56 \times 10^{-8} R_1^2 R_2$$

$$a_4 = 1.6 \times 10^{-8} R_1^2 R_2$$

To find the limit values of the coefficient a_0 we assume the parameters R_1 and R_2 deviate by a fraction x and y from their nominal values respectively. To maximize a_0 we have the objective function as given by (12) subject to constraints in (13). Note that here we have set out to find MSDF of R_1 . Similar approach can be used to find the MSDF of R_2 .

$$1.2 - R_{2, nom}(1 + y) \left\{ \begin{array}{l} 2.56 \times 10^{-3} + \\ 1.024 \times 10^{-7} R_{1, nom}^2 (1 + x)^2 \\ - 5.12 \times 10^{-4} R_{1, nom} (1 + x) \end{array} \right\} \quad (12)$$

$$4.096 \times 10^{-9} R_{1, nom}^2 (1 + x)^2 R_{2, nom} (1 + y) \\ + 5.12 \times 10^{-6} R_{1, nom} (1 + x) R_{2, nom} (1 + y) \\ = 4.096 \times 10^{-9} R_{1, nom}^2 (1 + \rho)^2 R_{2, nom} \\ + 5.12 \times 10^{-6} R_{1, nom} (1 + \rho) R_{2, nom} \quad (13)$$

$$1.28 \times 10^{-5} R_{1, nom} (1 + x) R_{2, nom} (1 + y) \\ - 1.536 \times 10^{-8} R_{1, nom}^2 (1 + x)^2 R_{2, nom} (1 + y) \\ = 1.28 \times 10^{-5} R_{1, nom} (1 + \rho) R_{2, nom} \\ - 1.536 \times 10^{-8} R_{1, nom}^2 (1 + \rho)^2 R_{2, nom} \quad (14)$$

$$2.56 \times 10^{-8} R_{1, nom}^2 (1 + x)^2 R_{2, nom} (1 + y) \\ = 2.56 \times 10^{-8} R_{1, nom}^2 (1 + \rho)^2 R_{2, nom} \quad (15)$$

$$1.6 \times 10^{-8} R_{1, nom}^2 (1 + x)^2 R_{2, nom} (1 + y) \\ = 1.6 \times 10^{-8} R_{1, nom}^2 (1 + \rho)^2 R_{2, nom} \quad (16)$$

$$-\alpha \leq x, y \leq \alpha \quad (17)$$

The extreme values for x and y on solving the set of equations in (12-17) we have $x = -\alpha$ and $y = -\alpha$, this gives us the MSDF value for R_1 , ρ in (18).

$$\rho = (1 - \alpha)^{1.5} - 1 \approx 1.5\alpha - 0.375\alpha^2 \quad (18)$$

Table I gives the MSDF for R_1 and R_2 based on above calculation.

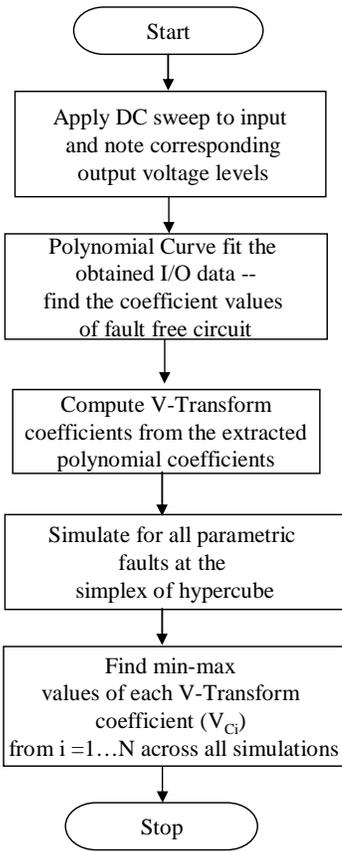


Fig. 2. Flow chart showing fault simulation process and bounding of coefficients.

V. GENERALIZATION

In general, calculation as above cannot be done for arbitrarily large circuits. Such circuits are handled by obtaining a nominal numeric polynomial expansion of the desired circuit. This is done by sweeping the input voltage across all possible values and noting the corresponding output voltages. Now, the output voltage is plotted against the input voltage. A polynomial is fit to this curve and the coefficients of this polynomial are taken to be the nominal coefficients of the desired polynomial. A V-Transform curve is now obtained based on the polynomial curve using the transformation in equation (9). The circuit is simulated for different drifts in the parameter values at equally spaced points from inside the hypercube enclosing each circuit parameter, spaced ϵ apart. Polynomials coefficients and hence V-Transform coefficients are obtained for each of these simulations. The maximum and minimum values of coefficient in this search are taken as the limit value on that coefficient. Once the limit values on all coefficients have been determined the CUT is subjected to DC sweep at the input. Its response to the DC sweep is curve fitted to a polynomial of order same as the fault free circuit. The V-Transform coefficients for CUT are now obtained. If there are any coefficients that lay outside the limit values of corresponding coefficients of the fault free circuit, we can conclude the CUT is faulty with a high probability that is inversely proportional to coefficient of uncertainty ϵ . The converse is also true. Flow chart in Figure 2 summarizes the process of numerically finding the V-T coefficients and finding the bounds on V-T coefficients. Flow chart in Figure 3 outlines the procedure to test CUT using the V-Transform coefficients. The bounds on coefficients of fault free circuit are found a priori as shown in flowchart of Figure 2.

VI. SIMULATION RESULTS

We subjected an elliptic filter shown in Figure 4 to V-Transform coefficient based test. The circuit parameter values are as in the benchmark circuit maintained by Stroud et al. [13]. Figure 5 shows the computed response and the estimated polynomial obtained by curve fitting:

$$v_{out} = 4.5341 - 3.498v_{in} - 2.5487v_{in}^2 + 2.1309v_{in}^3 - 0.50514v_{in}^4 + 0.039463v_{in}^5 \quad (19)$$

The combinations of parameter values leading to limits on the coefficients are as shown in Tables II and III. Some of the circuit parameters are not shown in the table because they do not appear in any of the coefficients and are kept at their nominal values. Further, results on pass/fail detectability of some injected faults is tabulated in Table IV.

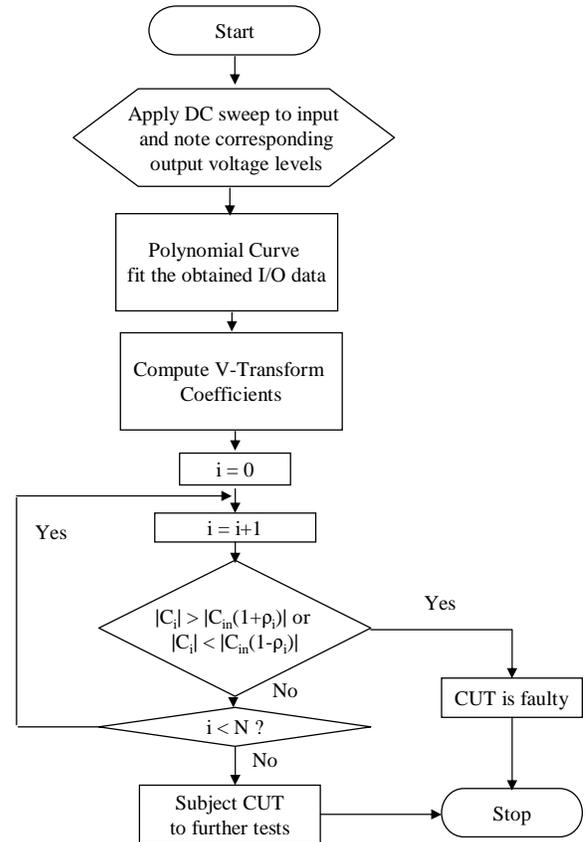


Fig. 3. Flow chart of test procedure for CUT.

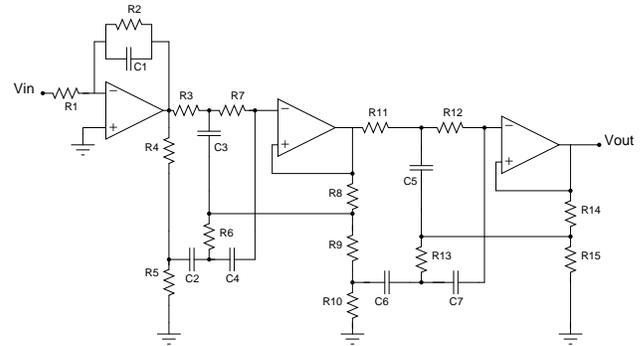


Fig. 4. Elliptic filter.

VII. CONCLUSION

A new approach for testing non-linear circuits based on polynomial expansion of the circuit was proposed. The approach was underpinned by V-Transform which renders the polynomial coefficients monotonic and increases the sensitivity of polynomial coefficients in transform domain (V-domain). The minimum size detectable faults of some of the parameters in circuits are as low as 5% which implies impressive fault coverage can be achieved with VTC as the metric. The method has been extended to sensitivity based fault diagnosis with probabilistic confidence levels in parameter drifts. The method of polynomial expansion at DC alone, as described here, may not detect certain types of faults, such as, parametric faults of a capacitor. To overcome this, in our ongoing work, we are generalizing this technique to multiple frequencies.

ACKNOWLEDGMENT

The authors would like to thank Prof. Vittala Rao, formerly with Dept. of mathematics, IISc for his comments and help in monotonicity arguments of V-Transform coefficients.

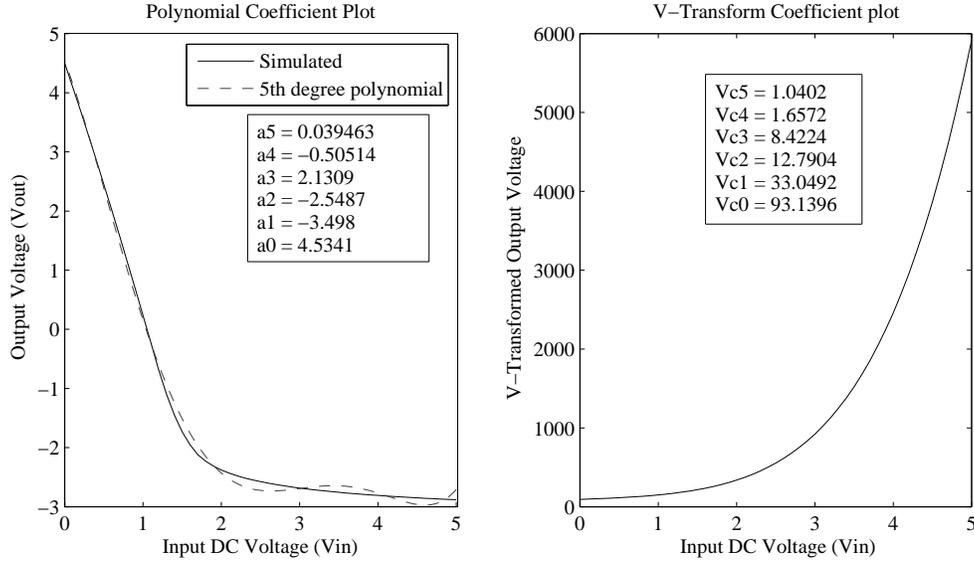


Fig. 5. DC response of elliptic filter with curve fitting polynomial and V-Transform plot

TABLE II
PARAMETER COMBINATIONS LEADING TO MAXIMUM VALUES OF
V-TRANSFORM COEFFICIENTS WITH $\alpha = 0.05$.

Circuit Parameter (Ω)	V_{c0}	V_{c1}	V_{c2}	V_{c3}	V_{c4}	V_{c5}
$R_1 = 19.6k$	18.6k	20.5k	20.5k	20.5k	18.6k	18.6k
$R_2 = 196k$	186k	205k	186k	186k	186k	205k
$R_3 = 147k$	139k	154k	154k	154k	139k	154k
$R_4 = 1k$	950	1010	1010	1010	1010	1010
$R_5 = 71.5$	70	80	80	70	80	70
$R_6 = 37.4k$	37.4k	37.4k	37.4k	37.4k	37.4k	37.4k
$R_7 = 154k$	161k	161k	146k	161k	146k	146k
$R_{11} = 110k$	115k	115k	104k	115k	104k	104k
$R_{12} = 110k$	104k	115k	104k	104k	104k	104k

TABLE III
PARAMETER COMBINATIONS LEADING TO MINIMUM VALUES OF
V-TRANSFORM COEFFICIENTS WITH $\alpha = 0.05$.

Circuit Parameter (Ω)	V_{c0}	V_{c1}	V_{c2}	V_{c3}	V_{c4}	V_{c5}
$R_1 = 19.6k$	20.5k	18.6k	18.6k	20.5k	20.5k	20.5k
$R_2 = 196k$	205k	186k	205k	205k	205k	186k
$R_3 = 147k$	150k	139k	139k	146k	154k	139k
$R_4 = 1k$	1010	950	950	950	950	950
$R_5 = 71.5$	80	70	70	80	70	80
$R_6 = 37.4k$	39.2k	39.2k	39.2k	39.2k	35.5k	39.2k
$R_7 = 154k$	146k	146k	161k	146k	161k	161k
$R_{11} = 110k$	104k	104k	115k	104k	115k	115k
$R_{12} = 110k$	115k	104k	115k	115k	115k	115k

REFERENCES

- [1] A. Abderrahman, E. Cerny, and B. Kaminska, "Optimization Based Multifrequency Test Generation for Analog Circuits," *Journal of Electronic Testing: Theory and Applications*, vol. 9, pp. 59–73, Mar 1996.
- [2] S. Chakravarty and P. J. Thadikaran, *Introduction to IDDQ Testing*. Kluwer Academic Publishers, 1997.
- [3] S. Cherubal and A. Chatterjee, "Test Generation Based Diagnosis of

TABLE IV
RESULTS FOR SOME INJECTED FAULTS.

Circuit Parameter	Out of bound polynomial coeff.	Fault detected?	Out of bound V-Transform coeff.	Fault detected?
R_1 down 15%	a_3, a_4	Yes	$V_{c0} - V_{c4}$	Yes
R_2 down 10%	a_2	Yes	V_{c2}, V_{c5}	Yes
R_3 up 5%	a_3	Yes	V_{c1}, V_{c2}, V_{c3}	Yes
R_4 down 15%	a_0	Yes	$V_{c0} - V_{c4}$	Yes
R_5 up 10%	a_4	Yes	V_{c0}, V_{c4}	Yes
R_7 up 5%	None	No	V_{c1}, V_{c2}	Yes
R_{11} up 5%	None	No	V_{c4}, V_{c5}	Yes
R_{12} down 5%	None	No	V_{c4}, V_{c5}	Yes

- Device Parameters for Analog Circuits," in *Proc. Design, Automation and Test in Europe Conf.*, pp. 596–602, 2001.
- [4] G. Devarayanadurg and M. Soma, "Analytical Fault Modeling and Static Test Generation for Analog ICs," in *Proc. Int. Conf. on Computer-Aided Design*, pp. 44–47, Nov. 1994.
- [5] S. L. Farchy, E. D. Gadzheva, L. H. Raykovska, and T. G. Kouyoumdjiev, "Nullator-Norator Approach to Analogue Circuit Diagnosis Using General-Purpose Analysis Programmes," *Int. Journal of Circuit Theory and Applications*, vol. 23, pp. 571–585, Dec. 1995.
- [6] R. K. Gulati and C. F. Hawkins, *IDDQ Testing of VLSI Circuits*. Kluwer Academic Publishers, 1993.
- [7] W. L. Lindermeir, H. E. Graeb, and K. J. Antreich, "Analog Testing by Characteristic Observation Inference," *IEEE Trans. Comp. Aided Design*, vol. 23, pp. 1353–1368, June 1999.
- [8] R. Rajsuman, *IDDQ Testing for CMOS VLSI*. Artech House, 1995.
- [9] J. Figueras, "Possibilities and Limitations of IDDQ Testing in Submicron CMOS," in *Proc. Innovative Systems in Silicon Conf.*, pp. 174–185, Oct. 1997.
- [10] Z. Guo and J. Savir, "Analog Circuit Test Using Transfer Function Coefficient Estimates," in *Proc. Int. Test Conf.*, pp. 1155–1163, Oct. 2003.
- [11] V. Panic, D. Milovanovic, P. Petkovic, and V. Litovski, "Fault Location in Passive Analog RC Circuits by measuring Impulse Response," in *Proc. 20th Int. Conf. on Microelectronics*, pp. 12–14, Sept. 1995.
- [12] S. Sindia, V. Singh, and V. D. Agrawal, "Polynomial Coefficient Based DC Testing of Non-Linear Analog Circuits," in *Proc. 19th ACM Great Lakes Symp. on VLSI*, May 2009.
- [13] R. Kondagunturi, E. Bradley, K. Maggard, and C. Stroud, "Benchmark Circuits for Analog and Mixed-Signal Testing," in *Proc. 20th Int. Conf. on Microelectronics*, pp. 217–220, Mar. 1999.