An Analog Bus for Low Power On-Chip Digital Communication

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Abstract

In this work, we are assessing a theoretical proposition of improving power consumption in complex VLSI circuits through a scheme of digital-analog-digital conversion of data. The proposed scheme replaces n-bit wide bus, running between cores, with a single line, by encoding the data(that was to be carried on the n-bit bus) into 2^n levels of voltage on a single wire. The bus power consumed by the proposed analog scheme compared to a typical digital scheme can significantly decrease. Bus encoding such as ours, may also be productively employed in test access mechanism for digital circuits. It can compress the amount of data to be communicated between the test head and the chip, and thereby reduce test time. We have carried out experiments that serve as proof-of-concept by evaluating power consumption of a case where an n- bit bus in a large digital circuit is replaced with a single wire using our proposed DAC/ADC bus encoding. SPICE simulation for an ideal case shows that, when replacing an 8-bit digital bus, the analog bus architecture can save up to 38.5% power.

Overview

- A significant fraction of power consumption in today's multi-core processors and system-on-chip can be attributed to power required to charge or discharge the capacitance of each line in the bus, running between two cores.
- The dynamic power consumed by a n-bit parallel bus, where, C = Capacitance of each line, f = frequency, V_{DD} = power supply voltage, α = activity factor, V_{swing} = Swing Voltage, is given by:

$$P_{parallel\ bus} = V_{DD}.f.\sum_{i=1}^{n} C_i . V_{swing,i}.\alpha_i$$

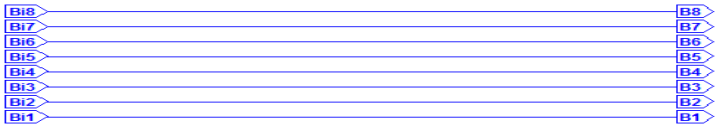

Fig. 1 8-bit Parallel Bus

- One of the prominent techniques to reduce power in a inter-core bus communication is by reducing the number of transitions and/or number of bus lines through bus encoding procedures.
- Alternate schemes for power reduction include low voltage and differential signaling, all of which try to limit the signal swing on the bit lines, thereby reduce power.

Proposed Idea

- The proposed scheme is to replace the n-bit wide bus running between cores with a single line, by encoding the data (that was to be carried on the n-bit bus) into **2^n** levels of voltage on a **single wire** as shown in Fig. 2.

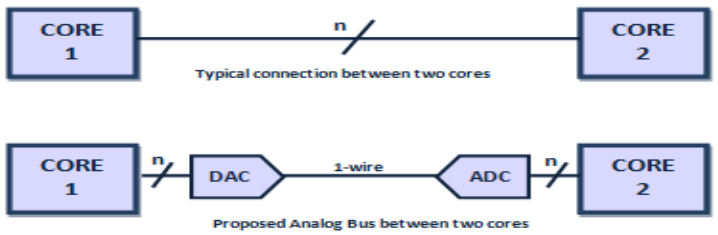

Fig. 2 Proposed strategy for bus elimination in multi-core processors

- Such a scheme offers the best of both the prominent low power inter-core communication schemes - bus encoding and differential/low-voltage signaling, as it offers the ultimate encoding of n lines to 1, and the average signal swing will be about $V_{DD}/2$.
- Dynamic Power consumed by a analog bus line replacing a parallel bus will be:

$$P_{analog\ bus} = V_{DD}.f.C.V_{swing}.\alpha$$

- The saving of power consumed in the proposed scheme to the typical scheme is noteworthy. For typical bus widths, such as n=32, this corresponds to more than two orders of reduction in the power dissipated on the bus.

Comparison with SERDES

SERializer/DE-Serializer is a widely used component in on-chip communication. Comparison between SERDES and our proposed technique is described below.

	Serialized Bus	Analog Bus
Bus Signal Type	Serial	Analog
Additional Element	Serializer and De-serializer	Analog to Digital Converter and Digital to Analog Converter
Average Voltage Swing	V_{DD}	V_{DD} /2
Required Time for a N-bit vector	n-clock cycle	1-clock cycle
Power Saving	No	Yes

Experiment Setup

In order to evaluate the power reduction with the proposed scheme:

- We replace the 8-bit lines with a single line and a combination of ideal DAC/ADC.
- Eventually both the parallel and proposed scheme drives the same digital circuit in each case, namely an adder.
- In our experiment, supply voltage is 1V, the wires have a capacitance of 1pF, fastest input signal is 50MHz and the ADC input clock is 100MHz.

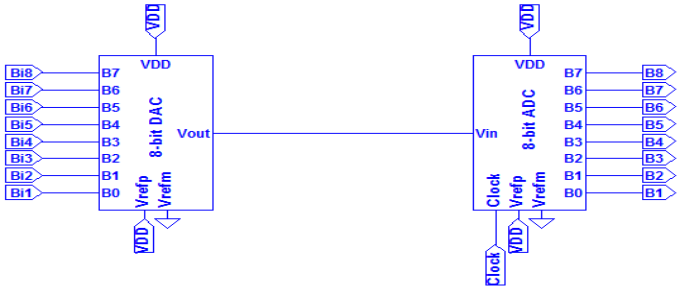

Fig. 3 8-bit bus replaced with Analog Bus Notice the single line between DAC and ADC

Discussion of Results

- Observing the results for power consumption, it is evident that when we replace the regular 8-bit bus line with a single wire using our proposed DAC/ADC bus encoding scheme, the system consumes less power.

Parallel Bus: Without Proposed Scheme	Analog Bus: With Proposed Scheme	Power Savings
16.578µW	10.195µW	38.5%

Table.1 Power Analysis for 8-bit Bus Line

- We have varied both the supply voltage and the noise voltage (in the analog line), for figuring out the noise margin for different sets of setup.
- From this analysis we found out that the level of noise tolerated by the circuit varied in proportion to the supply voltage.
- As we reduced V_{DD}, the noise margin also went down. This finding matches perfectly with our theoretical expectation.

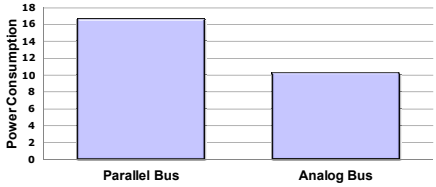

Fig. 4 Graph representation on comparison of Power Savings (in µW)

Risks and Challenges

- Since a single wire will be carrying a multitude of 2^n levels, ambient noise levels may limit successful communication between the cores.
- The power consumed by the high-resolution DACs and ADCs may limit the power savings of the scheme.

Future Work

- Evaluate power consumption for different ADC/DAC resolutions.
- Reduce Timing and Area overheads from added elements in between circuit.
- Design suitable compact and low power ADCs and DACs for the scheme.

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Thank you

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