A Linear Time Algorithm for Wire Sizing with Simultaneous Optimization of Interconnect Delay and Crosstalk Noise

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Abstract— In this paper, we propose a new methodology for wire sizing with simultaneous optimization of interconnect delay and crosstalk noise in deep submicron VLSI circuits. The wire sizing problem is modeled as an optimization problem formulated as a normal form game and solved using the Nash equilibrium. Game theory allows the optimization of multiple metrics with conflicting objectives. This property is exploited in modeling the wire sizing problem while simultaneously optimizing interconnect delay and crosstalk noise, which are conflicting in nature. The nets connecting the driving cell and the driven cell are divided into net segments. The net segments within a channel are modeled as players, the range of possible wire sizes forms the set of strategies and the payoff function is derived as the geometric mean of interconnect delay and crosstalk noise. The net segments are optimized from the ones closest to the driven cell towards the ones at the driving cell. The complete information about the coupling effects among the nets is extracted after the detailed routing phase. The resulting algorithm for wire sizing is linear in terms of the number of wire segments in the given circuit. Experimental results on several medium and large open core designs indicate that the proposed algorithm yields an average reduction of 21.48% in interconnect delay and 26.25% in crosstalk noise over and above the optimization from the Cadence place and route tools without any area overhead. The algorithm performs significantly better than simulated annealing and genetic search as established through experimental results. A mathematical proof of existence for Nash equilibrium solution for the proposed wire sizing formulation is provided.

I. INTRODUCTION

The optimization of delay and crosstalk noise is critical in deep submicron (DSM) designs and needs to be performed at different levels of the design flow. While the interconnect resistance impacts the delay, the coupling capacitance plays the most significant role in crosstalk noise [1], [2]. The high aspect ratio of wires result in more wire to wire capacitance among the neighboring wires in the same layer than the area capacitance between the upper and the lower wiring layers [2]. The noise due to cross-capacitance is the dominant component among the noise sources and is a major concern in deep submicron designs [3]. Modeling the noise of a circuit will need complete information about the nets (its neighboring nets, the length of overlap, spacing between the nets, etc) to analyze the coupling effects, and hence, is typically performed after the final routing of the design [4]. The common methods used to reduce DSM effects are driver sizing, buffer sizing, buffer insertion, wire sizing, wire spacing and net ordering. Among these, driver sizing, buffer sizing and buffer insertion are difficult to be applied at post route stage. In this work, we focus on interconnect delay and crosstalk noise optimization

using wire sizing at post-layout stage of the design.

A taxonomy of the various pioneering works found in the literature for the problem of wire sizing is shown in Figure 1. The earliest works on wire sizing can be found in [5]–[7] and they consider the interconnect wires by dividing each wire into smaller segments. In [8], the authors have provided closed form solutions to simultaneous buffer insertion/sizing and wire sizing using Elmore delay models. In [9] and [10], the coupling capacitance is considered during the wire sizing step. However, the interconnect positions and the routing congestion in the final layout are not considered. In [11], the problem of simultaneous wire sizing and wire spacing is investigated using Elmore delay models for optimizing interconnect delay without considering crosstalk. In [12], it is pointed out that Elmore delay models are inaccurate compared to transmission line models and a detailed transmission line model is developed for delay based on time domain analysis. The existing works on wire sizing do not consider the problem of simultaneous optimization of interconnect delay and crosstalk noise with accurate models.

In [13], Alpert et. al concluded that when minimizing interconnect delay using wire sizing, wire tapering is not cost-effective compared to uniform wire sizing. They also indicated that wire sizing is not widely utilized in current design flow due to the lack of complete design framework which is capable of performing wire size optimization. Following this, in our work, we have divided the nets into segments according to the channels, in order to perform uniform wire sizing for each net segment. We have identified that the best place to apply wire sizing in the design flow is at post-route stage (please refer to Section II) and hence, we develop a wire sizing framework to achieve multi-metric optimization in current design flow. The works on wire sizing reported in [5], [7], [8], [10] use analytical expressions and the works in [6], [9] use non-linear formulations while targeting for delay optimization. These models do not consider the routing congestion and the net positions, and hence, result in unconstrained wire sizes. The unconstrained wire sizes may lead to DRC violations and rerouting will be necessary to fix them. *Thus, there is a need to develop a new methodology which can be integrated in the current design flow for determining optimal wire sizes within the limits of DRC rules, and avoids the need for rerouting.*

In this work, we develop a complete design framework for simultaneous optimization of interconnect delay and crosstalk noise using wire sizing at post-route level which satisfies the above requirements. We use game theory as an optimization

tool to find the optimal wire sizes for interconnects. The interconnect wires are modeled as the players of the game trying to optimize their cost (payoff function) against other players. We later show that the resulting wire sizing formulation has linear time and space complexities. An overview of game theory can be found in [14].
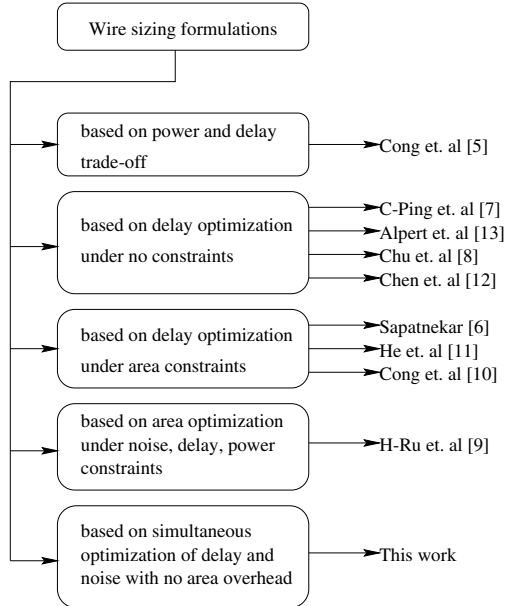

Fig. 1. Taxonomy of related works on wire sizing

II. MOTIVATION

The problem of wire sizing has been addressed by many researchers in the recent past. After the design is routed, the locations and orientations of the transistors and interconnect wires in the design are fixed. The application of optimization methods like buffer insertion, wire spacing, shielding, at post-route stage would result in area overhead and can lead to rerouting of the design. Rerouting of the design is time-consuming and costly to be performed repeatedly. Typically, when a design is routed, the channels have "unused" tracks which remain as white spaces and go through the fabrication process as wasted resource. Wire sizing can effectively make use of these "unused" tracks available through out the design, in optimizing the design parameters. If the wire sizing problem is modeled properly, it is possible to achieve optimization without the need for rerouting or additional area overhead. In this work, we show that wire sizing could be powerful and effective in making use of the unused routing resources to optimize design parameters at post-route stage.

Why Game Theory for Wire Sizing?

Game theory strongly supports the following four features: rationality, coalition formation, competition and equilibrium. Game theoretic reasoning takes into account what is best for a player with respect to every other player's objectives and

decisions. Thus, the goal is to find a solution that is the best for all the players in the game considering the various constraints and strategies. Each player's decision is based on the decision of every other player in the game and hence, it is possible to reach the equilibrium state corresponding to the global optima. As the wire size of a net increases, the interconnect delay decreases and the coupling capacitance increases (convex payoff function). The wire size of a net will affect the sizes of the neighboring nets, resulting in conflicting objectives. It is mentioned in [15] that for a game with players having convex interests, Nash equilibrium solution always exists and tends to achieve global optimal solutions. Also, it has been shown in [16] that *the complexity of determining the Nash equilibrium lies between P and NP depending on the problem formulation*. This suits the modeling of the problem using game theory with the possible wire sizes as strategies and the net segments as players who collectively work towards the global objective of optimizing the interconnect delay and crosstalk, modeled as the payoff function.

Traditionally, the wire sizing problem is modeled with crosstalk noise as the objective function, while maintaining interconnect delay as a constraint or vice versa. However, game theoretic formulation and Nash equilibrium solution allow the simultaneous optimization of multiple metrics with conflicting objectives. *Since, interconnect delay and crosstalk noise within a circuit are conflicting in nature, the proposed formulation is effective in terms of optimization*. Unlike other optimization techniques such as simulated annealing or genetic search, game theory exhibits the property of social equilibrium [17], which ensures that each element of the system is satisfied while the overall goals are reached. For example, other methods may not work towards optimizing each individual decision such as the individual wire sizes at each step while they are targeting the global objective. Thus, some wires may not be sized well. In game theory, the social equilibrium with respect to the individual decisions as well as the global objective are all considered together to ensure the fairness objective, in an inherent manner. The performance of the proposed algorithm is compared with that of simulated annealing and genetic search in order to illustrate the elegance of game theoretic solutions for problems with conflicting objectives. It is shown in Section V that the proposed approach yields better results than simulated annealing and genetic search under the assumptions of same models, setup, parameters and objective function for their implementation.

III. DELAY AND CROSSTALK MODELS

In this section, we discuss the interconnect delay and crosstalk models used in this work. Since the transmission line models are better in accuracy compared to the lumped models in modeling interconnect wires in deep submicron designs as pointed out in [12], [18], they are adapted in this work. The notations and terminology used in this paper are given in Table I. An analytical equation for the interconnect delay of a net is derived based on transmission line analysis in [12]. The propagation delay model reported in [12] is for a single

interconnect wire and hence, does not consider the coupling effects due to neighboring wires. This analytical model can be extended to incorporate coupling effects by replacing self capacitance C_i with total capacitance C_{tot_i}. In this work, we consider the coupling effects due to the immediate left and right neighbors for the reasons indicated in Section IV. Referring to the model developed in [12], the left and right mutual capacitances act in parallel with self capacitance. Hence, the total capacitance is given as $C_{tot_i} = C_i + C_{il} + C_{ir}$. Also, the propagation velocity is given as $V_i = 1/\sqrt{U_i C_{tot_i}}$.

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TABLE I

NOTATIONS AND TERMINOLOGY

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R	resistance of the interconnect line per unit length
C_i	self capacitance of interconnect line per unit length
U_i	inductance of interconnect line per unit length
R_d	resistance of driver gate or the driving net segment
W_i	width of the given interconnect line
C_{il}/C_{ir}	mutual capacitance per unit length of overlap between the net and its immediate left/right neighbor
C_l/C_r	self capacitance of left/right neighbor line per unit length
W_l/W_r	width of the left/right neighboring interconnect line
S_l/S_r	spacing between net and its immediate left/right neighbor
L	length of the given interconnect line
T	thickness of the given interconnect line
H	height of the given interconnect line from the dielectric
Z_L	load impedance of the given interconnect line
C_L	load capacitance of the given interconnect line
V_i	propagation velocity of the given interconnect line

The analytical expressions for the self capacitance and mutual capacitances have been derived in terms of its wire widths and spacings in [19] and [20] respectively. These equations are reproduced below in terms of our model parameters. The self capacitance C_i is given by the Equation 1 [19]. The mutual capacitance between the given net and its immediate left neighbor is given by Equation 2 [20]. The mutual capacitance between the given net and its immediate right neighbor can be obtained by replacing the values of width and spacing in Equation 2 with those of right neighbor.

$$C_i = \epsilon_r \left[10.166 \left(\frac{W_i}{H} \right) + 24.752 \left(\frac{T}{H} \right)^{0.222} \right] \ pF/m \quad (1)$$

$$C_{il} = \frac{55.6\epsilon_r}{ln \left[\pi^2 S_l^2 \left(\frac{1}{W_l + T} \right) \left(\frac{1}{W_i + T} \right) \right]} \ pF/m \quad (2)$$

The modified interconnect delay equation is given by Equation 3 (extended based on [12]).

$$D_i = \frac{L}{V_i} + \eta_i \left(R_d + \frac{\sqrt{U_i}}{W_i \sqrt{C_{tot_i}}} \right) C_L \quad (3)$$

where,

$$\eta_i = \frac{\ln 2 \left(e^{\theta_i} + 2\theta_i \left(e^{\theta_i} - 1 \right) \right)}{2}; \quad \theta_i = \frac{RL\sqrt{C_{tot_i}}}{2\sqrt{U_i}}$$

The crosstalk noise on a given net can be calculated using the superposition theorem by considering the coupling effects due its left and right neighbors separately. The crosstalk voltage due to the left neighbor can be defined as the voltage $V_l(t)$ induced across the load C_L of the net under consideration. It has been shown in [18] that the amplitude of crosstalk voltage at time t is given by Equation 4.

$$V_l(t) = \frac{1}{2} \left[\exp \left(-\frac{t}{\tau_1} \right) - \exp \left(-\frac{t}{\tau_2} \right) \right] \quad (4)$$

where, $\tau_1 = R(C_i + C_L)$ and $\tau_2 = R(2C_{il} + C_i + C_L)$. Using the theory of maxima and minima of differential calculus, it can be shown that the maximum value of the crosstalk voltage is given by Equation 5.

$$V_l^{max} = \frac{1}{2} \left[\exp \left[\left(\frac{N_{cl}-1}{2N_{cl}} \right) \ln \left(\frac{1+N_{cl}}{1-N_{cl}} \right) \right] \right]$$
$$- \frac{1}{2} \left[\exp \left[\left(-\frac{N_{cl}+1}{2N_{cl}} \right) \ln \left(\frac{1+N_{cl}}{1-N_{cl}} \right) \right] \right] \quad (5)$$

where, the capacitance coupling coefficient N_{cl} is given by $N_{cl} = C_{il}/(C_i + C_{il} + C_L)$. Similarly, the maximum crosstalk noise V_r^{max} induced across the load C_L of the net under consideration due to its right neighbor is given by Equation 6.

$$V_r^{max} = \frac{1}{2} \left[\exp \left[\left(\frac{N_{cr}-1}{2N_{cr}} \right) \ln \left(\frac{1+N_{cr}}{1-N_{cr}} \right) \right] \right]$$
$$- \frac{1}{2} \left[\exp \left[\left(-\frac{N_{cr}+1}{2N_{cr}} \right) \ln \left(\frac{1+N_{cr}}{1-N_{cr}} \right) \right] \right] \quad (6)$$

where, N_{cr} is obtained by replacing C_{il} with C_{ir} in N_{cl}. The total crosstalk noise on the given interconnect is calculated by applying the superposition theorem for voltages V_l^{max} and V_r^{max}, defined in Equations 5 and 6 respectively.

IV. PROPOSED METHODOLOGY

The problem of wire sizing can be defined as finding the optimal wire widths such that interconnect effects (delay and crosstalk noise in this work) are minimized. The parasitic resistance and capacitance of interconnect wires are highly dependent on the wire widths. The coupling capacitance is responsible for the majority of the deep submicron effects. Hence, it is important to extract the coupling capacitance of nets with high accuracy. The coupling capacitance of a net depends on its wire size, the length of overlap and spacing between adjacent nets. This information can be efficiently extracted at post-routing phase. In this work, we have modeled the problem of wire sizing such that it does not require rerouting and does not incur area overhead. The global grids of the router are used to partition the complete routing area into rectangular sections called channels. The channel boundaries are used in dividing the nets into net segments.

The following information is extracted from the routed design to calculate the parasitics: (i) the net segments of each net, (ii) the channel and the track numbers of the net segments, (iii)

the wire lengths and the starting positions of the net segments in a channel, and (iv) the net segment metal layer type and its orientation. The minimum wire size of a net segment is given by the minimum size requirements of the process technology. The maximum wire size for a net segment is determined from the track distance between its immediate adjacent nets and the minimum edge-to-edge spacing requirements. The range between minimum and maximum wire sizes for each net segment is divided into discrete set of values with equal step size. The discrete set of allowable wire sizes for a given net segment is modeled as its strategy set without violating the design rules.

Algorithm 1 Wire sizing algorithm for interconnect delay and crosstalk noise optimization

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Input: Placed and routed design
Output: Optimized wire sizes
  Algorithm:
  extract the net information
  organize the nets into channels and tracks
  identify terminal net segments
  for all layers **do**
    for all channels **do**
      initialize loads();
      initialize scores();
      determine strategies();
      mark the channel as un-played
    end for
  end for
  select a channel i with lowest score value
  while there exists an un-played channel **do**
    calculate mutual-capacitance();
    calculate wire-capacitance();
    calculate wire-resistance();
    for all net segments $j \in$ channel i **do**
      create a 3-player game with j, its left and right neighbors as players
      cost-matrix $\leftarrow$ payoff(three players, strategies)
      optimized-width $\leftarrow$ nash-solution(3 players, payoffs)
    end for
    update loads();
    update scores();
    mark the channel as played
    select the a new channel with lowest score value
  end while
  return: optimized widths of all net segments

A game is modeled for each individual channel. The channels located on different layers are considered separately as they consist of different net segments. For a given channel, its net segments are modeled as the players of the game. The coupling effects on a net segment depends on all the net segments adjacent to it, but decreases rapidly as the distance between them increases. As pointed out in [21], in the context of wire sizing, *it is sufficient to consider the coupling*

effects due to its immediate neighbors for two reasons: (i) The coupling effects of other neighboring nets are minimal when compared to the immediate neighbors due to their increased distance from the given net. (ii) The immediate neighbors act as shields to the given net from the other neighboring nets. Hence, in this work, we consider the coupling effects due to its immediate left and right neighbors for a given net segment.

The payoff function tries to capture the interaction between the neighboring net segments (modeled as the players of the game) in the channel. For each net segment, its delay D and maximum crosstalk noise N are calculated by using the Equations 3, 5, and 6. The delay and noise values obtained for a net segment are normalized with respect to the corresponding first strategy. The normalization is performed to transform the delay and noise values into dimension-less quantities so that they be correlated. The payoff function is modeled as the geometric mean of normalized delay and noise values. We have chosen geometric mean so as to give equal weights to both noise and delay components during their optimization.

We have used normal form game formulation to mathematically represent and solve the problem. The strategy set and the payoff matrix of the players are sufficient to solve a normal form game. The players simultaneously chooses a strategy $s_i \in S_i$ such that their respective payoff is maximized or minimized with respect to the payoffs of the other players. The equilibrium of the game is computed by using the Nash equilibrium condition. Consider a channel consisting of N net segments. The wire size of any net segment in the channel is influenced only by its immediate left and right neighbors. Thus, for each channel, instead of having a single game with N-players, we divide the game into N sub-games with each sub-game involving 3-players: the given net segment, its left neighbor and its right neighbor.
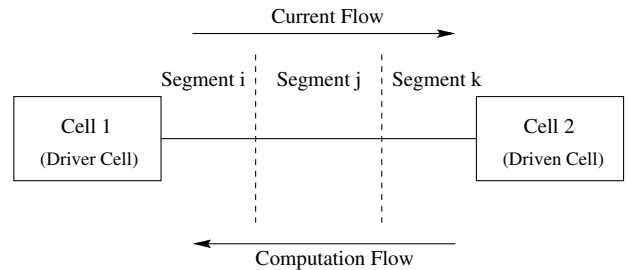

Fig. 2. An example scenario

As an example, consider a net connected between cell 1 and cell 2 with cell 1 driving the net and cell 2 receiving, as shown in Figure 2. In this example, the net is divided into three segments just as an example for illustration. The load capacitance of segment k is the input capacitance of the cell 2, which is known. The cell 2 and segment k act as loads for segment j. The wire capacitance of segment k depends on its wire width. Hence, in order to calculate the load capacitance of segment j, the wire width of segment k has to be optimized, *requiring segment k to play the game before*

segment j. In general, the load capacitance of a net segment can be calculated only when its down-stream wire segments are optimized. A score, defined as the difference between the total net segments and the number of terminal nets belonging to a channel, is used for ordering the channels. *The ordering of the channels aid in considering the effects of wire sizes of the down-stream net segments. Even though the game is played for a segment at a time, the load capacitance takes into account the effects of its complete net. Thus, the resulting solution is not a local solution confined to a segment of the net.*

A channel with lowest score is selected to play the game with its non-terminal net segments assigned to a default load capacitance. Nash equilibrium is evaluated and the Nash widths are used to update the load capacitances of net segments belonging to adjacent channels. The scores of only the neighboring channels have to be updated to reflect the net segments with known load values as terminal net segments. Hence, after a channel is played out, the load and score values of at most six adjacent channels (left, right, top, bottom in same layer, and, above and below in adjacent layers) have to be updated to reflect the calculated Nash widths. Again, a channel with lowest score is selected to play the game and this process is repeated until all the channels are played out. Algorithm 1 represents the pseudo-code of the complete wire sizing algorithm for optimization of delay and crosstalk noise.

A. Time and Space Complexity

The worst-case time complexity of evaluating Nash equilibrium for a general M-player game with S strategies for each player is given as $O(M * S^M)$ [22]. In this work, we have modeled the problem of simultaneous interconnect delay and crosstalk noise to use 3-player games. The number of strategies for each player depends on its range of possible wire sizes. We have chosen the step size such that the number of strategies for any net segment is less than five. Each net segment in the channel will form a 3-player game with its left and right neighbors. Hence, the complexity of calculating Nash equilibrium for a channel with N net segments is given as $O(N * 5^3) \approx O(N)$. The Nash equilibrium chooses optimal wire sizes for the players considering each game individually. But, a player will participate in three different games formed for itself, its right neighbor and its left neighbor. We noticed from our experiments that the widths resulting from the three games are equal for around 70% of net segments. In case of different widths, maximal likelihood Nash width is assigned to the net segment. Considering all the channels and the layers in a given design, the worst-case time complexity of proposed algorithm is given as

$$O\left(L * \sum_{i=1}^{C} N_i \right) = O\left(\sum_{\forall i \in nets} n_i \right)$$

where L is the number of metal layers, C is the number of channels in a layer, N_i is the number of net segments in channel i and n_i is the number of net segments for net i. Hence, the time complexity of the proposed algorithm is

linear in terms of total net segments in the design. The space complexity of the proposed algorithm is dependent entirely on the number of net segments in the design and the payoff matrix. The space complexity of the payoff matrix depend on the number of strategies for each player in the game. As the games are played sequentially, the total space required by all games put together is equal to the space complexity of a game involving players with maximum number of strategies. Hence, mathematically, the space complexity is given as $O(S_1 * S_2 * S_3) \leq O(5*5*5)$, where S_1, S_2, and S_3 are the strategy sets of 3-player game involving the players with maximum strategies. Hence, the space complexity of the proposed algorithm is given as

$$O\left(\sum_{\forall i \in nets} n_i + 5 * 5 * 5 \right) \approx O\left(\sum_{\forall i \in nets} n_i \right)$$

B. Proof of Existence of Nash Equilibrium Solution for Wire Sizing Formulation

In this section, we provide the proof of existence of Nash equilibrium in the case of wire sizing problem for simultaneous optimization of interconnect delay and crosstalk noise. As the wire size of a net increases, the interconnect delay decreases and the coupling capacitance increases resulting in a convex payoff function. Let $G = \{S_1, \ldots, S_n; f_1, \ldots, f_n\}$ be a game with each player $i \in N$ having a strategy set S_i containing its possible wire sizes and its payoff given by f_i. We have modeled the strategy set S_i for each player as a non-empty, compact set of a finite dimensional Euclidean space. Because of the convex nature of the interconnect delay and crosstalk noise, the modeled payoff function f_i becomes upper semicontinuous on $S = \Pi_{i=1}^{N} S_i$ and for any fixed $u_i \in S_i$, the function $f_i(u_i, .)$ is a lower semicontinuous on $S_{(-i)}$ [23]. For any $u \in S$, the best reply or the expected payoff $B_i(u)$ is also convex. According to Kakutani's fixed point theorem [24], the game G has at least one Nash equilibrium point if the graph

$$G_B = \{(x, y) : x \in S, y \in B(x)\}$$

is closed.

Lets assume that its not closed. Then, $\exists (x^0, y^0) \notin G_B$, such that every neighborhood (in $S \times S$) of (x^0, y^0) contains a point of G_B.

$\because x^0$ is a wire size, it has to be one of those from the set of possible wire sizes for the given player in order to satisfy the DRC rules of the used process technology.

$\therefore x^0 \in S \Rightarrow y^0 \notin B(x^0)$

In other words, for at least one net segment playing the game (say segment 1), there is an $y_1^1 \in S_1$ such that

$$f_1(y_1^1, x_2^0, \ldots x_n^0) \geq f_1(y_1^0, x_2^0, \ldots x_n^0) \tag{7}$$

Let F be a function such that $F : S^2 \to \Re$ and given as

$$F(x, y) = f_1(y_1^1, x_2, \ldots x_n) - f_1(y_1, x_2, \ldots x_n)$$

Since f_i is upper semicontinuous on S and $f_i(u_i, .)$ is lower semicontinuous on S_{-i}, F is lower semicontinuous and $C = \{(x,y) \in S^2 : F(x,y) \leq 0\}$ is closed. Hence, for any $(\bar{x}, \bar{y}) \in G_B, F(\bar{x}, \bar{y}) \leq 0$. But, by Equation 7, $F(x^0, y^0) \geq 0$, contradicting the closedness of C. Thus, there is a point $s^* \in S$ such that $s^* \in B(s^*)$, which is a Nash equilibrium point.

C. Discussion

In this section, we explain the rationale behind the optimization of all the nets of the design rather than only the critical nets. In the context of wire sizing at post-route phase, the maximum size with which a net can be sized is fixed. The sizing of a net has to be performed within this feasible range or else a considerable number of nets have to be rerouted. *This applies to the critical nets also and hence, have to be sized with the amount of routing resources available to it*. With the available routing resources, the game theoretic formulation allows a better allocation for the critical nets when compared to its neighbors. This is because the payoff values for critical nets dominate that of its neighbors and hence, Nash equilibrium gives more weightage to the critical nets and results in a solution which is in best interest for both critical nets and its neighbors. *The routing resources available at other locations can be better used to optimize the corresponding nets, rather than leaving them unused*. Hence, we have planned to optimize all the nets in the design. Also, optimizing all the nets in design will have an advantage of enforcing the timing closure, the signal integrity for all nets and hence, aids in other post-layout optimization techniques. The experimental results validates our claims depicting better critical net savings for our approach when compared to the simulated annealing and genetic search.

D. Design Flow

The design flow for obtaining an optimally wire sized circuit from a verilog/VHDL description is shown in Figure 3. The behavioral verilog/VHDL description is synthesized using a library of standard cells. We have used the First Encounter™ RTL-to-GDSII tool from Cadence® Design Systems to perform the placement and routing of gate-level RTL design. The net information required for calculations of delay and crosstalk is extracted from the routed design. A gawk script is developed which extracts this information from the exported routed DEF file. The models of Interconnect delay and crosstalk noise and the modeling of payoff function are described in Sections III and IV respectively. The payoff function is used by the game theoretic based wire size solver described in Algorithm 1 to optimize interconnect delay and crosstalk noise. The optimized wire sizes resulted from the game theoretic wire size solver are used to update the routed design. We have developed another gawk script which updates the wire sizes of all the nets in the original DEF design with their corresponding optimized wire sizes. It should be noted here that the resulting optimized design do not require rerouting as all the sized nets satisfies the design rules of the given process technology.
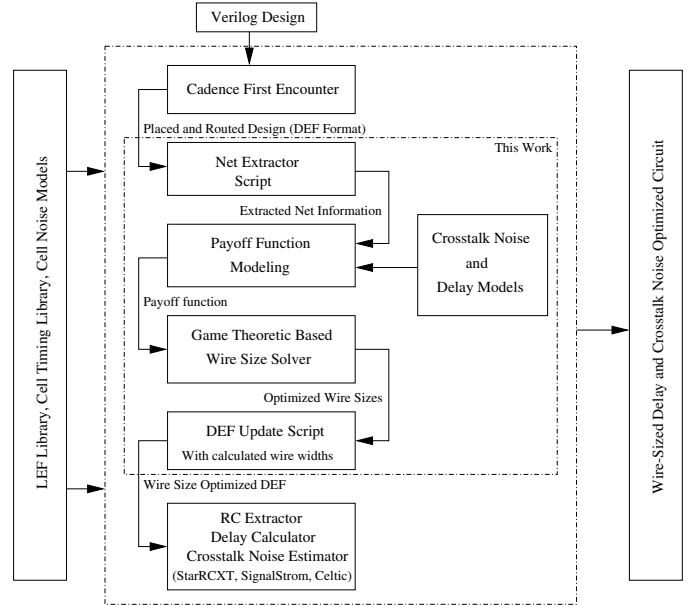

Fig. 3. General Design Flow

V. Experimental Results

We have implemented the proposed algorithm in C and executed on a UltraSPARC-IIe 650MHz, 512MB Sun Blade 150 system operating on Solaris 2.8 and tested with the ASIC designs from Opencores [25]. A 180nm, 6-Metal standard library is obtained from Crete [26], an educational university campus program developed and maintained by Cadence design systems. ASIC designs, written in behavioral style are converted to structural VHDL/Verilog with the help of BuildGates from Cadence design systems. We have modified the ASIC designs such that all the blocks in the design are flattened to standard cells without maintaining the hierarchy. The on-chip memory modules are realized as D-flipflop register arrays. Cadence First Encounter is used for placing and routing the the structural VHDL/Verilog design. *We have set the row utilization to 95% to have a compact floorplan for all the designs*. The net information is extracted from the DEF file and given as input to game theoretic wire size solver. The calculated wire sizes are used to update the wires to generate an optimized DEF. It can be noted that the optimized DEF is created with the help of gawk script and is not rerouted. The parasitic resistances and capacitances from both original and optimized DEF files are extracted using StarRCXT from Synopsys Inc. *The interconnect delay and crosstalk noise are estimated using Cadence Signalstrom and CelticIC respectively with their robust models, and not using the analytical models used in this paper*.

Several of the pioneering works reported in the literature for the problem of wire size optimization [5], [7], [8], [10]–[12], only present results for arbitrary nets and do not consider routing congestion, floorplan compaction, etc, of the designs. *Thus, it is not possible to provide a direct comparison of our*

Open core Design [25]	Total Nets	Die Area (mm^2)	Genetic Search Approach						Simulated Annealing Approach						Game Theoretic Approach [This Work]					
			Run time (mins)	% Delay Savings		% Noise Savings			Run time (mins)	% Delay Savings		% Noise Savings			Run time (mins)	% Delay Savings		% Noise Savings	
				Avg.	Crit.	Avg.	Crit.			Avg.	Crit.	Avg.	Crit.			Avg.	Crit.	Avg.	Crit.
Mult	854	0.199	34.16	2.45	5.32	3.10	4.32		14.32	6.15	8.91	5.12	13.26		1.89	9.87	11.79	12.13	17.23
PCI bus	19520	0.434	183.23	12.79	20.16	13.78	19.96		47.35	10.31	21.22	12.36	23.39		5.23	19.32	34.21	21.42	37.38
Serial ATA	43563	1.624	418.31	17.94	31.02	11.53	25.82		124.83	18.91	28.65	12.41	26.37		11.86	29.87	39.95	20.14	42.15
RISC	61468	2.102	729.47	11.91	17.37	9.19	15.46		188.33	20.39	39.89	16.31	24.25		16.86	25.22	35.21	22.31	29.73
AVR μP	78770	11.103	972.51	10.18	11.25	13.67	22.13		232.67	17.57	21.35	27.67	40.12		21.32	22.45	37.63	31.34	40.31
P16C55 μC	102021	19.984	1301.43	11.64	15.48	25.91	29.18		288.36	17.98	29.47	31.67	39.45		28.98	19.86	27.45	43.29	57.98
T80 μC	157850	30.388	1689.24	13.76	14.11	15.23	18.10		353.25	14.86	15.97	23.39	29.74		39.48	23.78	34.87	33.12	39.89
Average				11.52	16.39	13.63	19.28			15.17	23.64	18.42	28.08			21.48	31.26	26.25	37.81

* No area overhead for all three approaches. The percentage values indicated are w.r.t placed and routed design without wire sizing.

[1] *Table Legend: Avg: Average savings of all the nets in the entire design; Crit: Savings on the critical path net of the design; Runtime: indicates the running time.*

results with those works. To compare our results, we have implemented simulated annealing and genetic search based algorithms and executed on the same Solaris machine with same set of inputs and constraints. The annealing process in the implementation ***simulated annealing*** based solution was determined through extensive experiment in order to get the best results and the maximum optimization. The nets are divided into net segments and the set of possible wire sizes for each net segment is calculated as indicated in Section IV. In each move of the annealing process, a net segment is randomly selected and its size is assigned from the set of its possible wire sizes. The cost function is defined as the geometric mean of the interconnect delay and the crosstalk noise summed over all the net segments. The initial temperature is determined by finding the average change in the cost for a set of random moves from the starting configuration and selecting the temperature which leads to an accept probability of 0.95. The number of moves per temperature for each design is set to 20 times the number of net segments in the design so as to allow an average of at least 10 to 15 moves for each net segment before settling for its solution. The up-hill moves are accepted with a probability of $e^{-\frac{\delta C}{T}}$, where δC is the change in the cost and T is the current temperature of the iteration. The temperature is cooled at the rate of 0.95.

The wire sizing problem for simultaneous interconnect delay and crosstalk noise optimization is modeled as a ***genetic search*** mechanism and solved using GALib [27]. The initial population contains the net segments with their corresponding wire sizes as used in the original unsized design. Each individual in the population called chromosome is represented as a set of three integers indicating the net number, the segment number and the wire size assigned to the segment. The chromosomes evolve through successive iterations called generations. During each generation, the chromosomes are evaluated for their fitness test. We have defined the fitness criterion as the deviation of the crosstalk noise and interconnect delay of each net segment from its worst-case values. The chromosomes with lower values of crosstalk noise and interconnect delay are given higher fitness values. We have used steady-state genetic algorithm available as a part of GALib library to generate overlapping populations which retains its 30% of fittest chromosomes in its new generations. The mutation process for a chromosome is defined as to randomly select a wire size from its set of possible wire sizes. The new chromosomes are created using single point crossover and are validated against their set of possible wire sizes. The selection process of chromosome is adopted by the roulette wheel selection approach. We have set the convergence-of-population as the stopping measure for the evolution of generations.

Table II shows the experimental results. First column indicates the name of the design and the second column indicates its corresponding number of nets. The area indicated in third column is chip area occupied by the core without considering its I/O pins. The fourth, ninth and fourteenth columns indicate the runtime of genetic search, simulated annealing and game theoretic wire size solvers respectively. Columns five and seven indicate the average delay and noise savings for all the nets of the design obtained by genetic search mechanism. Columns ten and twelve indicate the same for simulated annealing approach where as Columns fifteen and seventeen indicate for game theoretic approach. Columns six and eight indicate the critical net delay and noise savings obtained by genetic search mechanism. Columns eleven and thirteen indicate the same for simulated annealing approach where as Columns sixteen and eighteen indicate for game theoretic approach. The experiments were conducted such that the area overhead is zero in all three approaches. The savings obtained in terms of interconnect delay and crosstalk noise depend on the factors like floorplan compaction, routing congestion. This is because the routing congestion decides the wire size scaling of the nets routed through that region. It can be noticed that game theoretic approach yields better savings than genetic search and simulated annealing for all the test case designs. In addition, our algorithm has significantly smaller run times than genetic search or simulated annealing for considerably large-scale designs. *Hence, our approach is scalable and can handle the complexity of large SOC designs.*

VI. CONCLUSIONS

Game theory allows the simultaneous optimization of multiple metrics in the context of conflicting objectives leading

to a convex objective function in the problem formulation. This essentially makes it possible to use game theory for simultaneous optimization of interconnect delay and crosstalk noise. Optimizing both interconnect delay and crosstalk noise is extremely critical in deep submicron and nano regime circuits. The use of game theory and Nash equilibrium for the problem of wire sizing to optimize interconnect delay and crosstalk noise is being attempted for the first time. The proposed method results in a linear time algorithm with significantly better results than simulated annealing, making this work an important contribution.

Our intention in this work was to show that wire sizing can be used to achieve simultaneous optimization of interconnect delay and crosstalk noise at post-route stage. We observed that the previous algorithms for wire sizing target for single metric optimization with other parameters as constraints and have not been tested with all the design constraints such as routing congestion, floorplan compaction, position of nets, etc. Further, prior works have not indicated a viable design flow to include wire sizing [11], [13]. It has been pointed out in [13] that wire tapering for the entire net can yield 5% more savings in delay when compared to uniform wire sizing. However, performing uniform wire sizing within a net segment for all the segments of a net can yield significant savings in terms of crosstalk noise and interconnect delay at post-route stage.

VII. Acknowledgments

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