RFIC Design and Testing for Wireless Communications

A PragaTI (TI India Technical University) Course
July 18, 21, 22, 2008

Lecture 8: Frequency synthesizer design I (PLL)

By

Vishwani D. Agrawal
Fa Foster Dai

200 Broun Hall, Auburn University
Auburn, AL 36849-5201, USA

RFIC Design and Testing for Wireless Communications

Topics

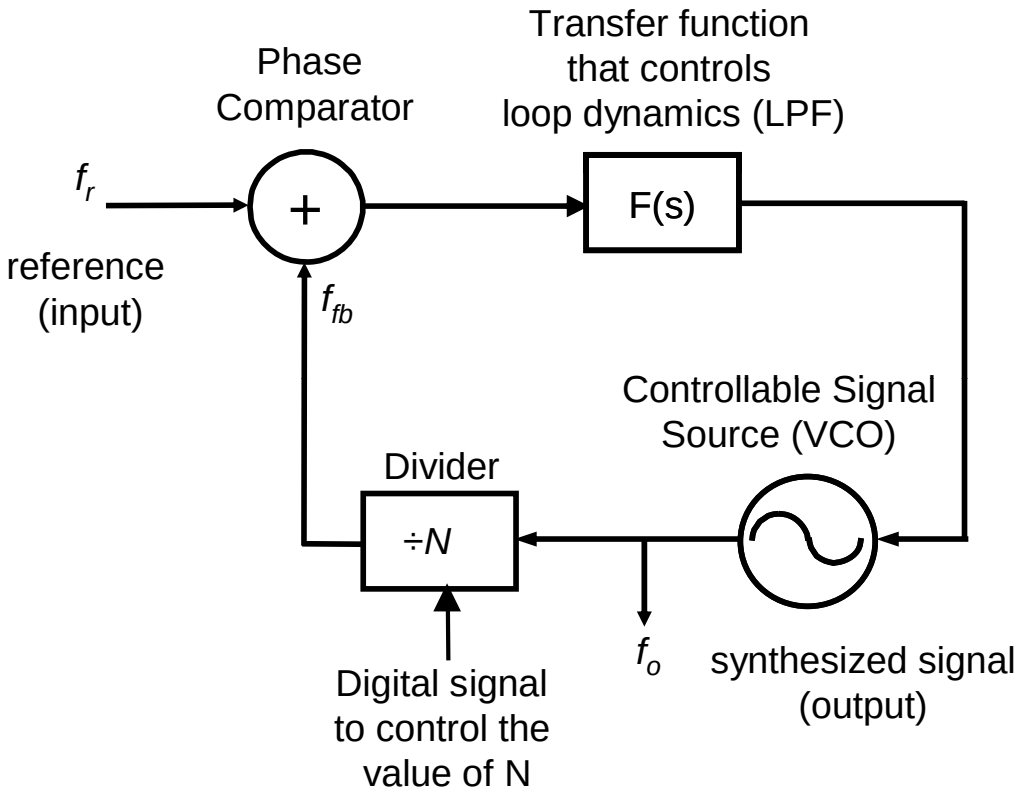
Monday, July 21, 2008

9:00 – 10:30	Introduction – Semiconductor history, RF characteristics
11:00 – 12:30	Basic Concepts – Linearity, noise figure, dynamic range
2:00 – 3:30	RF front-end design – LNA, mixer
4:00 – 5:30	Frequency synthesizer design I (PLL)

Tuesday, July 22, 2008

9:00 – 10:30	Frequency synthesizer design II (VCO)
11:00 – 12:30	RFIC design for wireless communications
2:00 – 3:30	Analog and mixed signal testing

Phase Lock Loop Integer-N Frequency Synthesizer



$$f_o = N \cdot f_{\text{ref}}$$

N is an integer → the minimum step size = f_r →to get a smaller step size, the reference frequency must be made smaller → N must be higher in order to generate the same f_o → larger phase noise (in-band noise magnified 20logN times by the loop).

Fractional-N Concept

If the loop divisor *N* is a fractional number, e.g., N=K/F, where K and F are integer numbers → the minimum step size = f_r /F→ can achieve small step size without lowering the reference frequency → loop divisor N can be small in order to generate the same f_o → better phase noise (in-band noise magnified 20logN times by the loop).

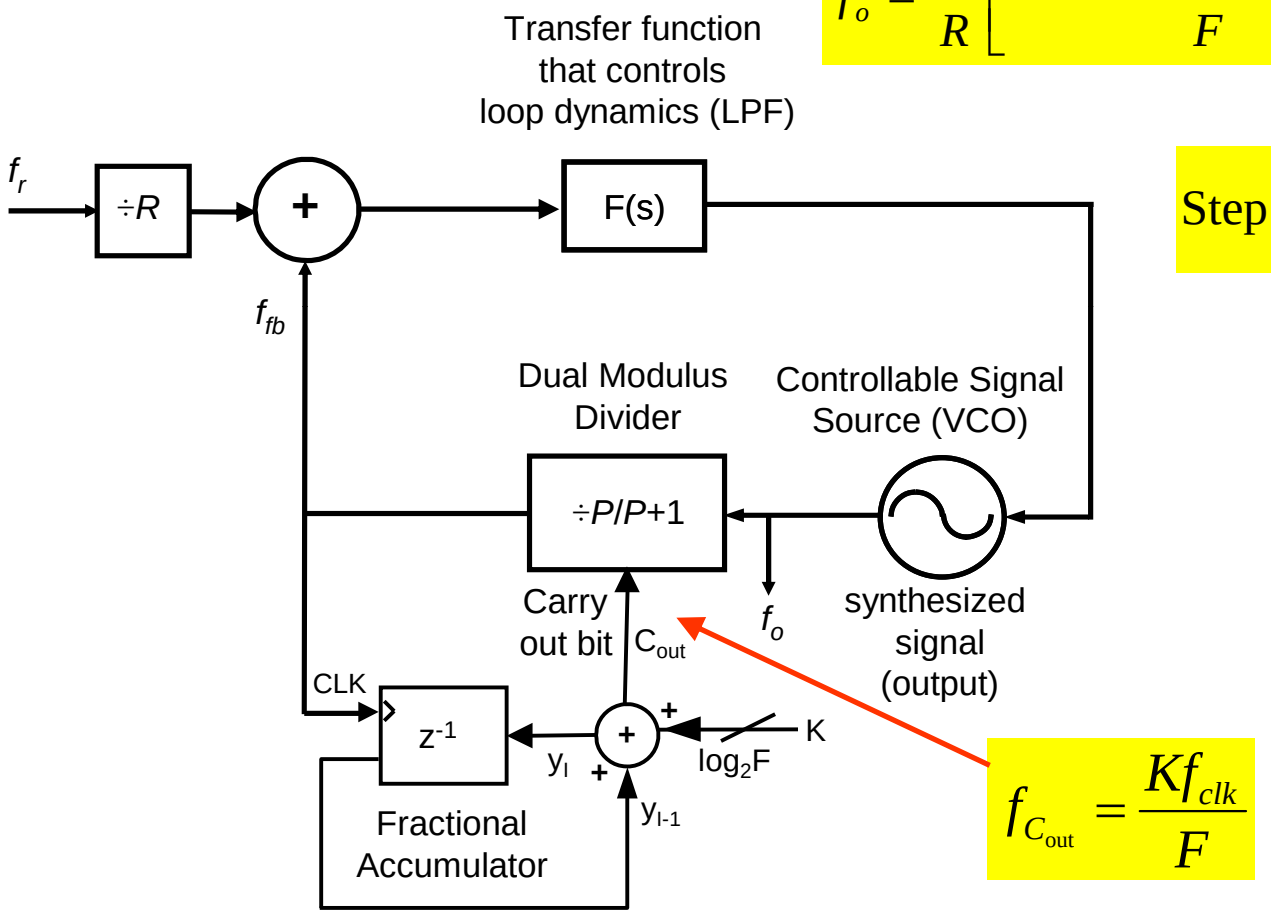
How can we design a fractional divider? Divider is a digital block and its output transits only at the input clock edge → we can only generate integer frequency divider!!

Dual-modulus divider P/P+1: by toggling between the two integer division ratios, a fractional division ratio can be achieved by time-averaging the divider output. As an example, if the control changes the division ratio between 8 and 9, and the divider divides by 8 for 9 cycles and by 9 for 1 cycle and then the process repeats itself, then the average division ratio will be:

$$\overline{N} = \frac{8 \times 9 + 9 \times 1}{10} = 8.1$$

Fractional-N synthesizer with a dual modulus prescaler

$$f_o = \frac{f_r}{R}\left[\frac{(P+1)K + P(F-K)}{F}\right] = \frac{f_r}{R}\left[P + \frac{K}{F}\right]$$

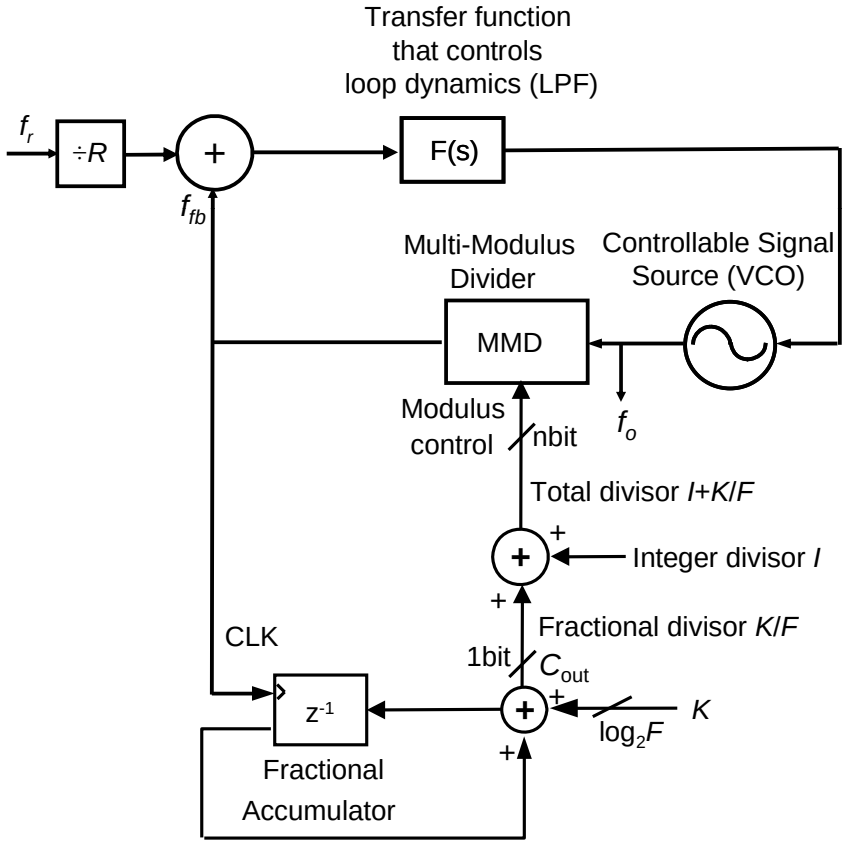


$$\text{Step Size} = \frac{f_r}{RF}$$

$$f_{C_{out}} = \frac{Kf_{clk}}{F}$$

Fractional-N frequency synthesizer with a multi-modulus divider

$$N_{\mathrm{MMD}} = P_1 + 2^1 P_2 + \ldots 2^{n-2} P_{n-1} + 2^{n-1} P_n + 2^n$$

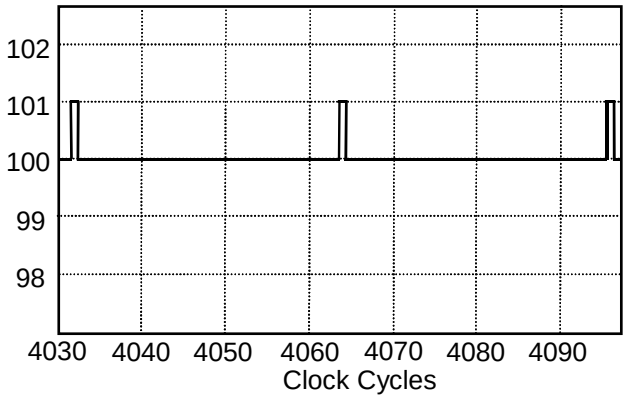


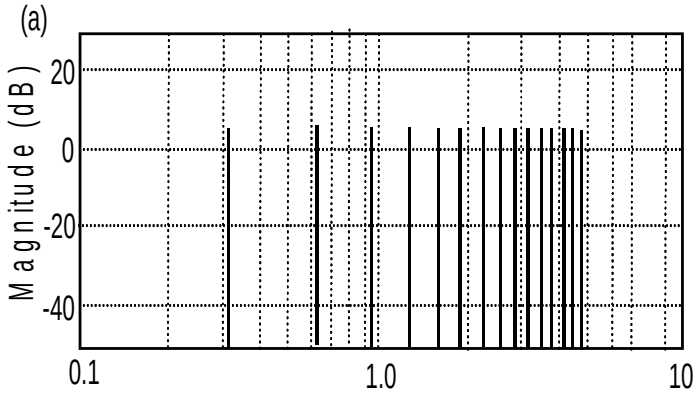
$$f_o = \frac{f_r}{R}\left[I + \frac{K}{F}\right]$$

Fractional-*N* Spurious Components

Any repeatable pattern in the time domain causes spurious tones in the frequency domain.

The fractional accumulator periodically generates the carry out that toggles the loop division ratio → spurious tones at multiples of the carryout frequency $f_r \cdot (K/F)$, which is the step size of the fractional-N synthesizer. → the smaller the step size is, the closer the spur locates to the carrier.



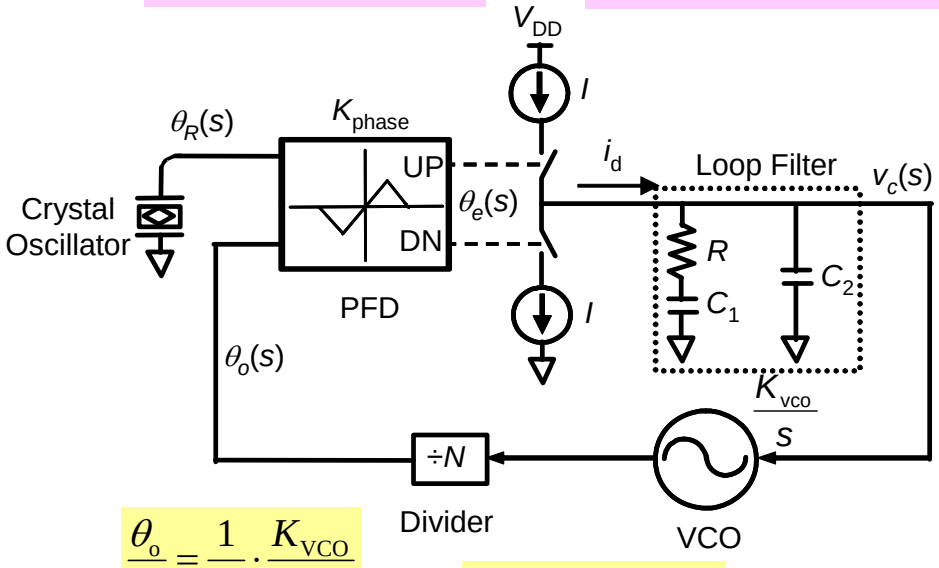


PLL Frequency Synthesizer

$$v_e(s) = K_{\mathrm{PD}}(\theta_R - \theta_o)$$

$$i_d = K_{CP}K_{PD}(\theta_R - \theta_o)$$

$$v_c = \frac{K_{\mathrm{PD}}K_{\mathrm{CP}}(\theta_R - \theta_o)(1 + sC_1R)}{s(C_1 + C_2)(1 + sC_sR)}$$

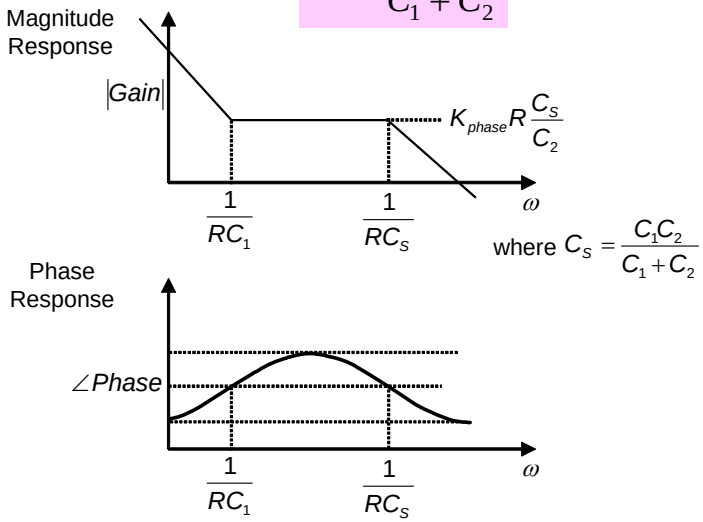


$$\frac{\theta_o}{v_c} = \frac{1}{N} \cdot \frac{K_{\mathrm{VCO}}}{s}$$

$$\frac{\theta_{\mathrm{VCO}}(s)}{v_c(s)} = \frac{K_{\mathrm{VCO}}}{s}$$

$$\omega_{\mathrm{VCO}} = K_{\mathrm{VCO}}v_c$$

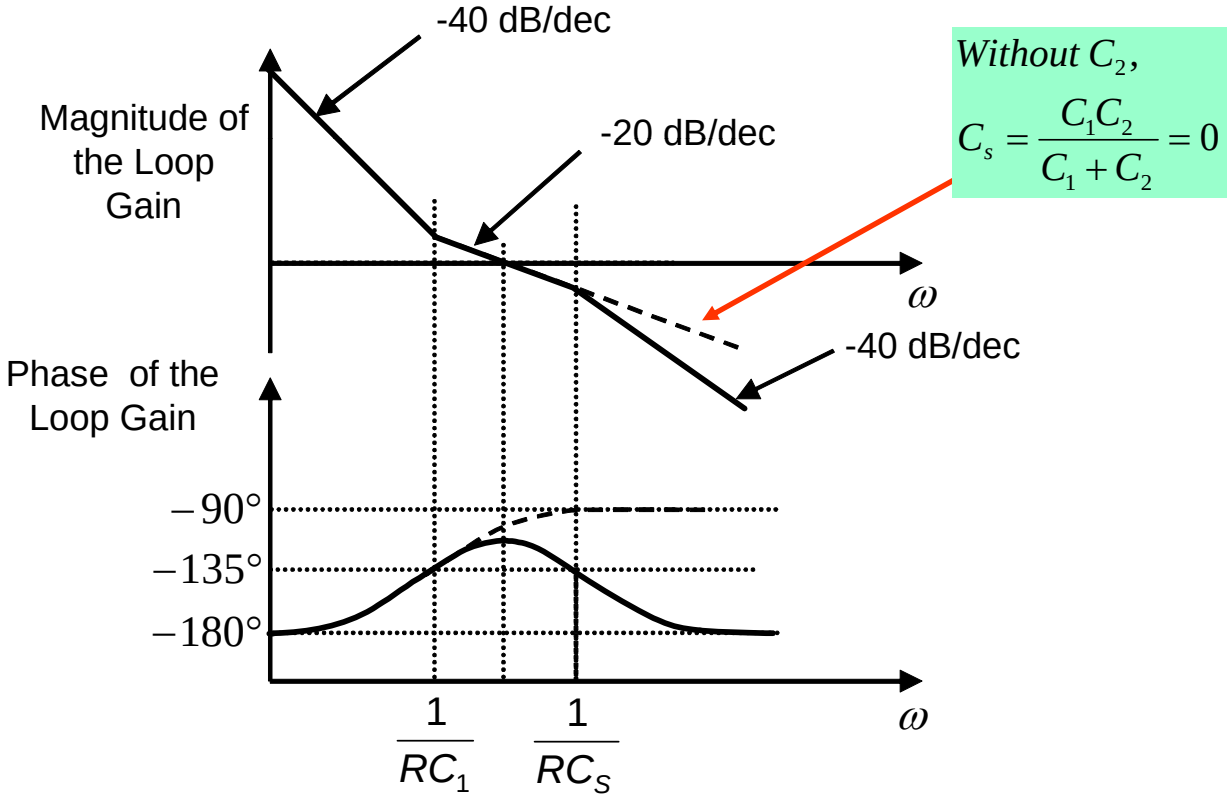
$$C_s = \frac{C_1C_2}{C_1 + C_2}$$



Open Loop Transfer Function

$$\left(\frac{\theta_o}{\theta_R}\right)_{\text{open loop}} = \frac{K_{VCO}K_{PD}K_{CP}(1+sC_1R)}{s^2N(C_1+C_2)(1+sC_sR)}$$

C_2 (about $C_1/10$) adds a high frequency pole to clean up high frequency ripple on the control line.



Without C_2,

$$C_s = \frac{C_1C_2}{C_1+C_2} = 0$$

Closed Loop Transfer Function

$$\frac{\theta_o}{\theta_R} = \frac{K_{VCO}K_{PD}K_{CP}(1+sC_1R)}{s^2N(C_1+C_2)(1+sC_sR)+K_{VCO}K_{PD}K_{CP}(1+sC_1R)}$$

$2nd-orderPLL$
$Without\ C_2, C_s = 0$

$$\frac{\theta_o}{\theta_R} = \frac{K_{VCO}K_{PD}K_{CP}(1+sC_1R)}{s^2NC_1+K_{VCO}K_{PD}K_{CP}(1+sC_1R)}$$

natural frequency

$$\omega_n = \sqrt{\frac{K}{NC_1}}$$

$$\frac{\theta_o}{\theta_R} = \frac{\omega_n^2\left(\frac{2\zeta}{\omega_n}s+1\right)}{s^2+2\zeta\omega_n s+\omega_n^2}$$

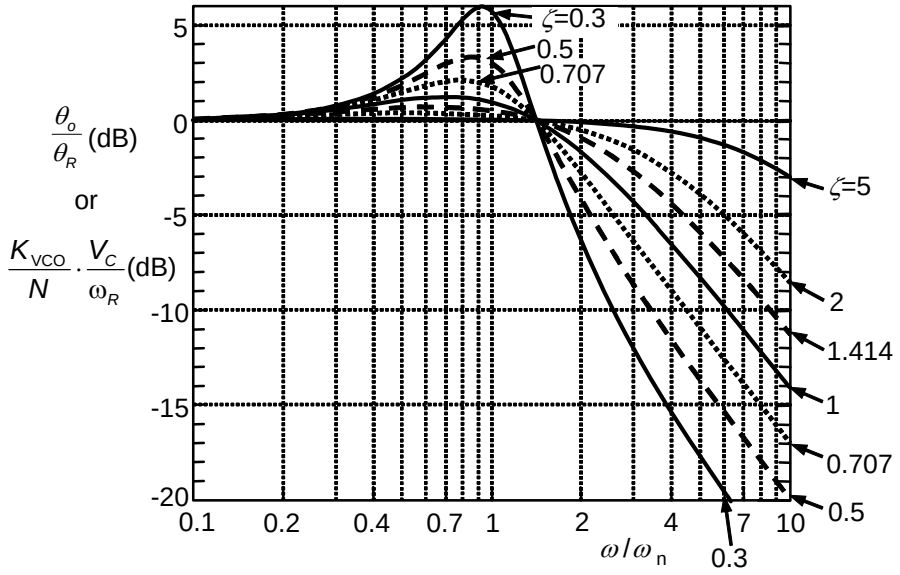
damping constant

$$\zeta = \frac{R}{2}\sqrt{\frac{KC_1}{N}}$$

$$\omega_{3dB} = \omega_n\sqrt{1+2\zeta^2+\sqrt{4\zeta^4+4\zeta^2+2}}$$

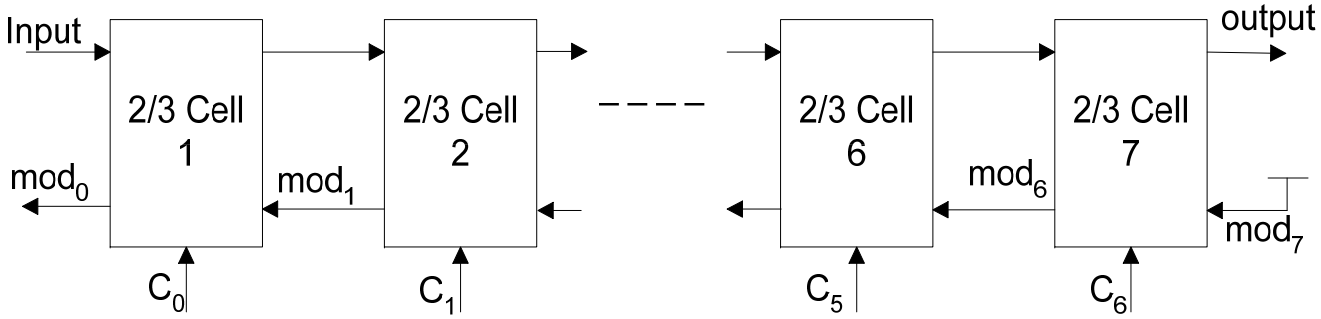
$$\omega_{3dB} \approx (1+\zeta\sqrt{2})\omega_n \quad \zeta < 1.5$$

$$\omega_{3dB} \approx 2\zeta\omega_n = K/N \quad \zeta > 1.5$$



PLL frequency response

MMD Architecture Using 2/3 Cells



$$N_{MMD} = 2^n + 2^{n-1}C_{n-1} + 2^{n-2}C_{n-2} + \cdots + 2C_1 + C_0$$

$$\text{For 3 bit MMD, } N_{MMD}(n=3) = 8 + 4C_2 + 2C_1 + C_0 = 8 \sim 15$$

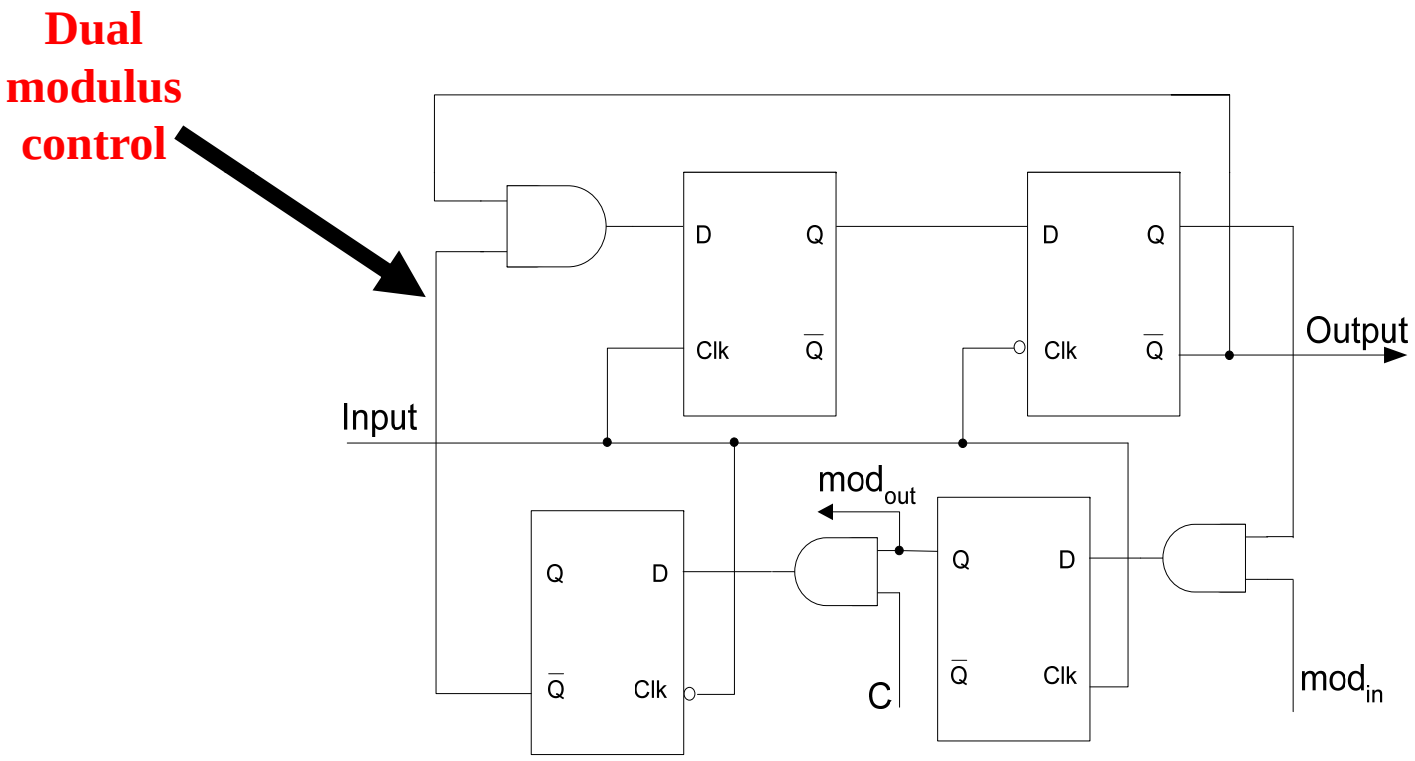
Say, we need an MMD with division ratios: 128-135.

$$N = 2^7 + 2^6C_6 + 2^5C_5 + 2^4C_4 + 2^3C_3 + 2^2C_2 + 2^1C_1 + C_0$$

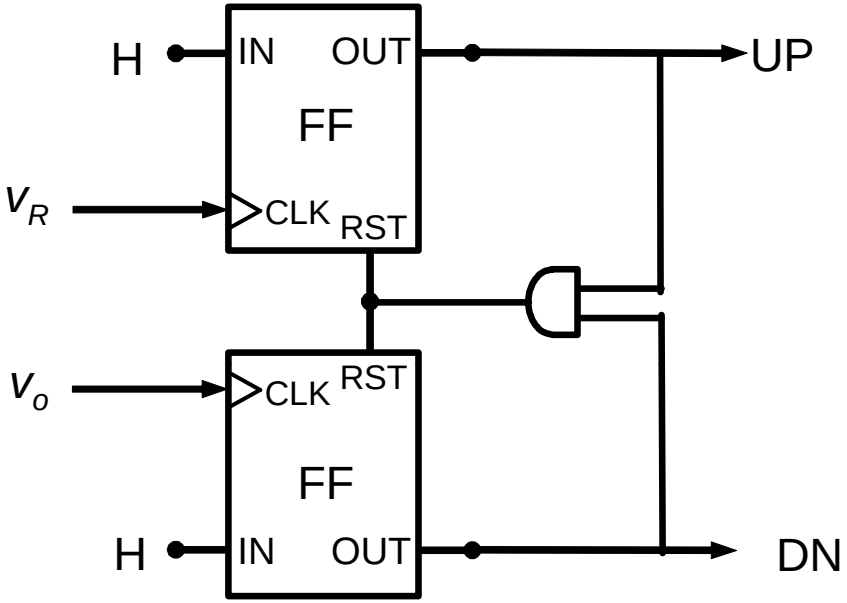
The division ratios obtained using 2/3 cells: 128-255.

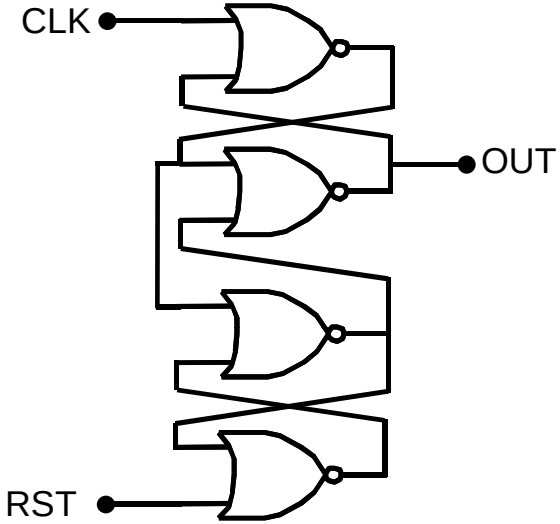
Dual Modulus Prescaler – 2/3 Cell

mod_{in}=1 and C=1 → F_o/F_{in}=1/3; mod_{in}=1 and C=0 → F_o/F_{in}=1/2
mod_{in}=0 and p=x → F_o/F_{in}=1/2



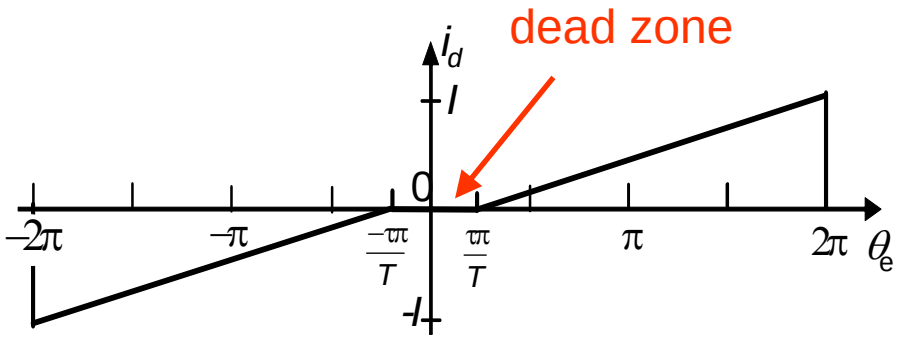
Tri-State PFD Circuit

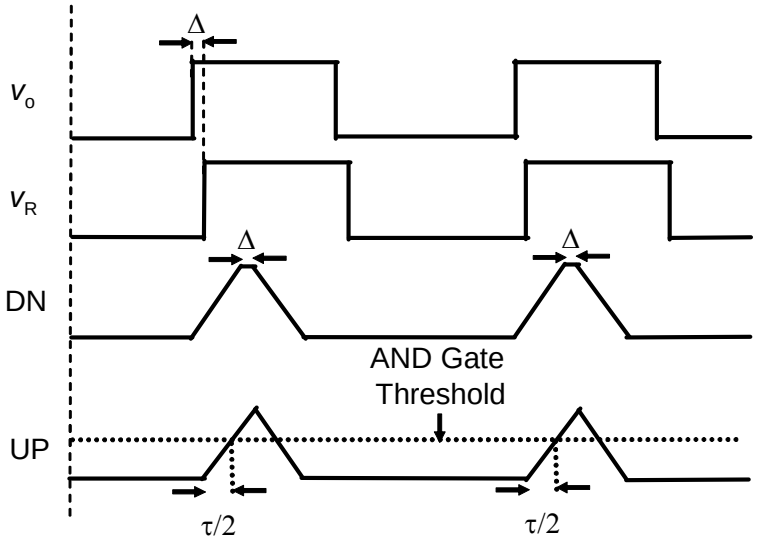


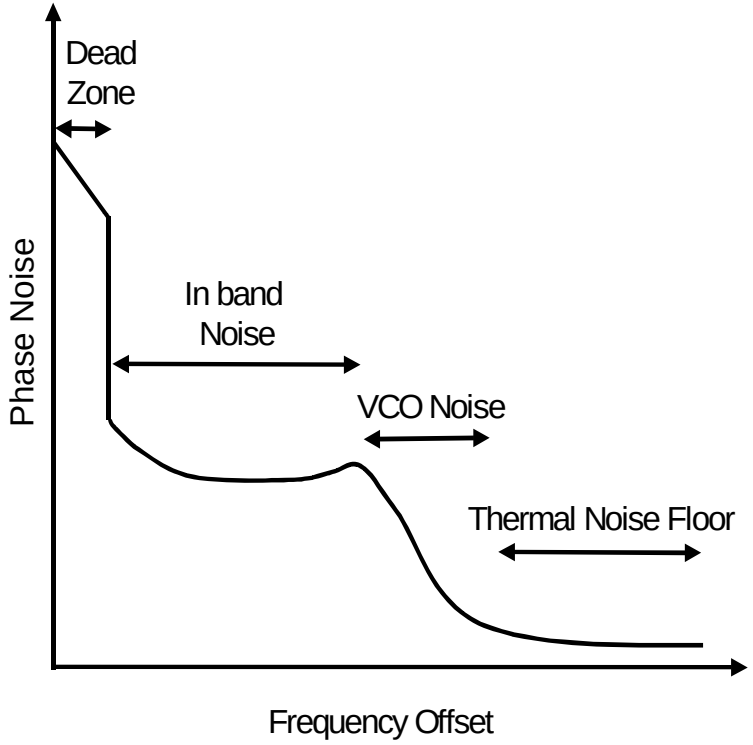


Positive edge-triggered D flip-flop with active low reset and hidden *D*=1

PFD Dead Zone

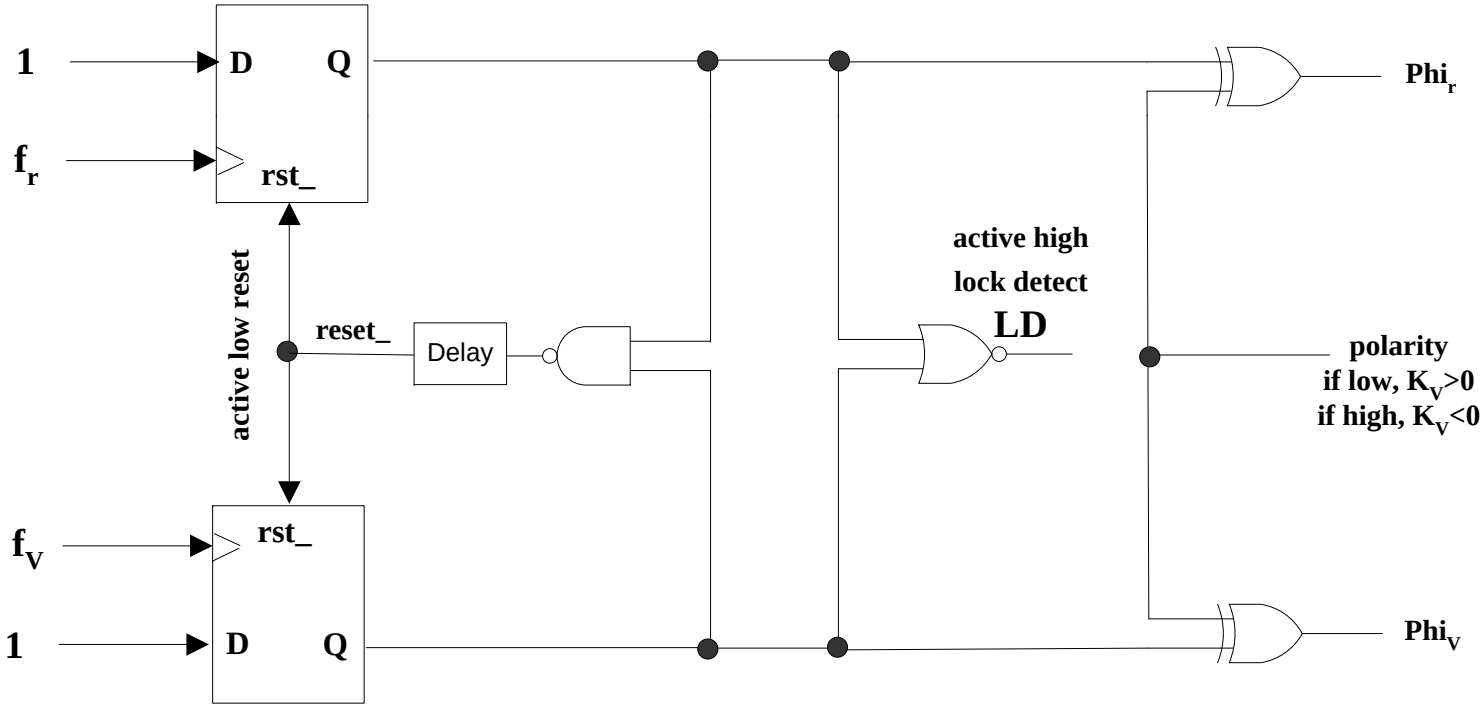




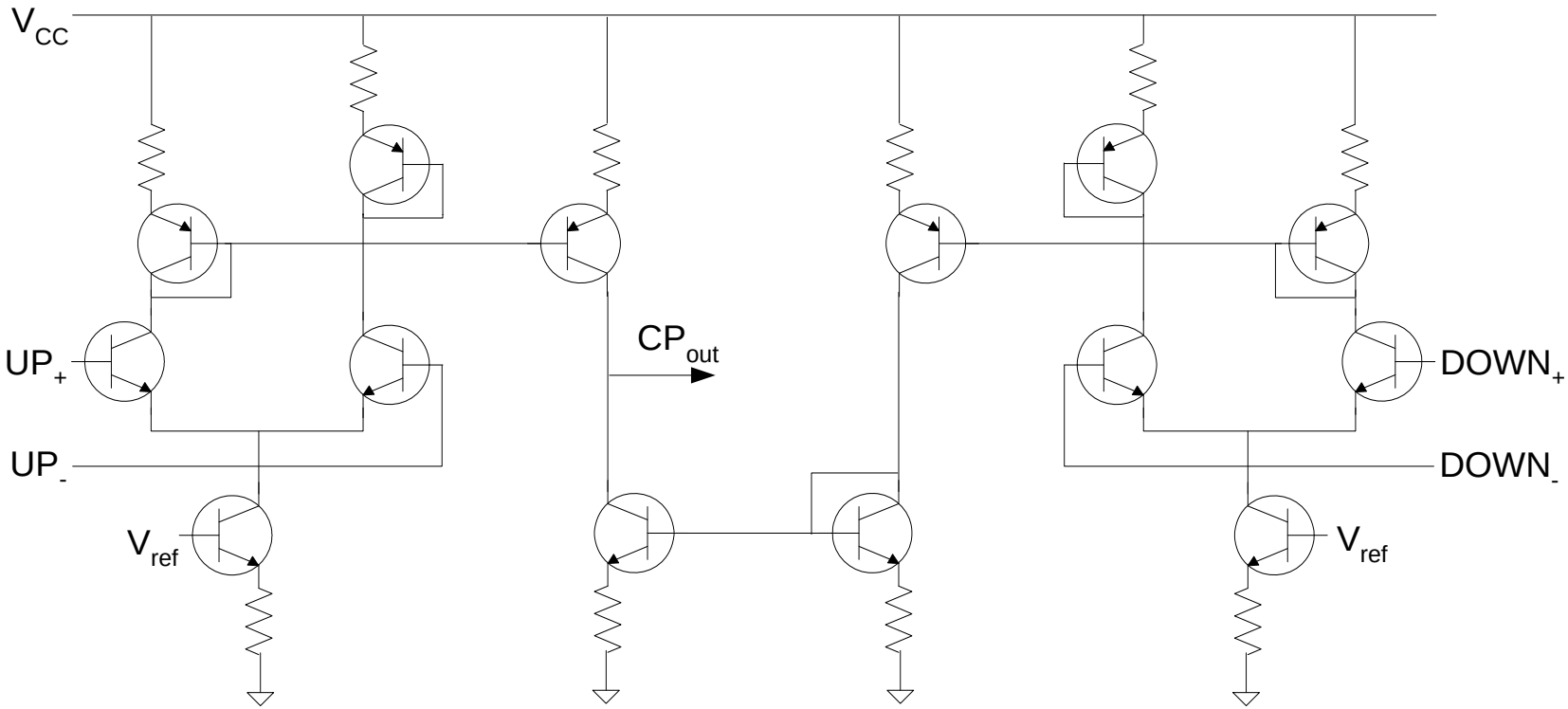


Phase/Frequency Detector

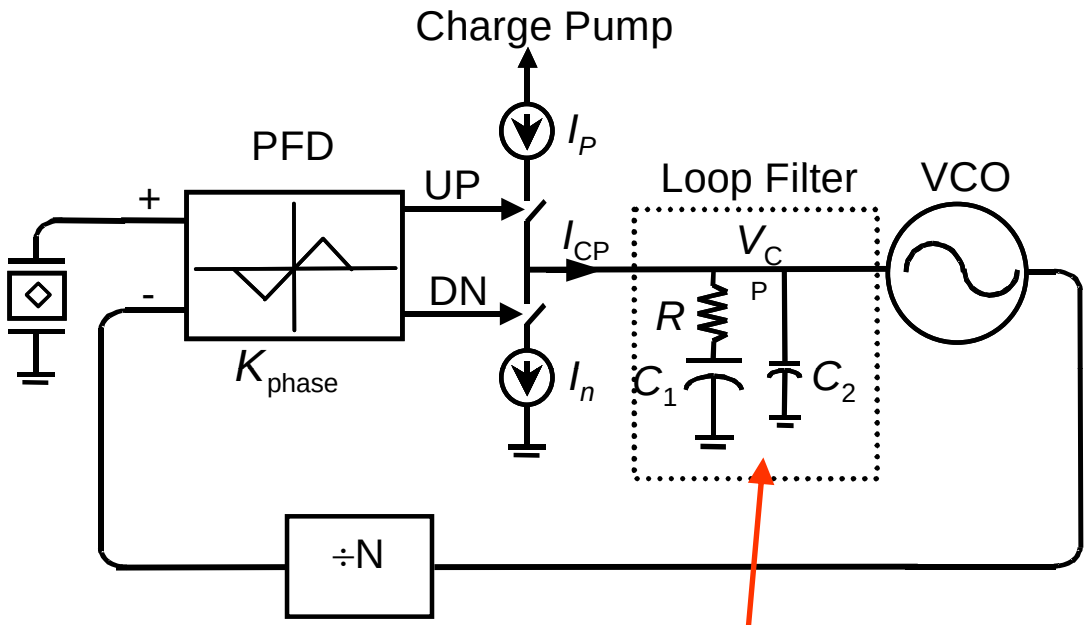
Tri-State Phase/Frequency Detector



Differential charge pump circuitry



2nd Order Passive Loop Filters

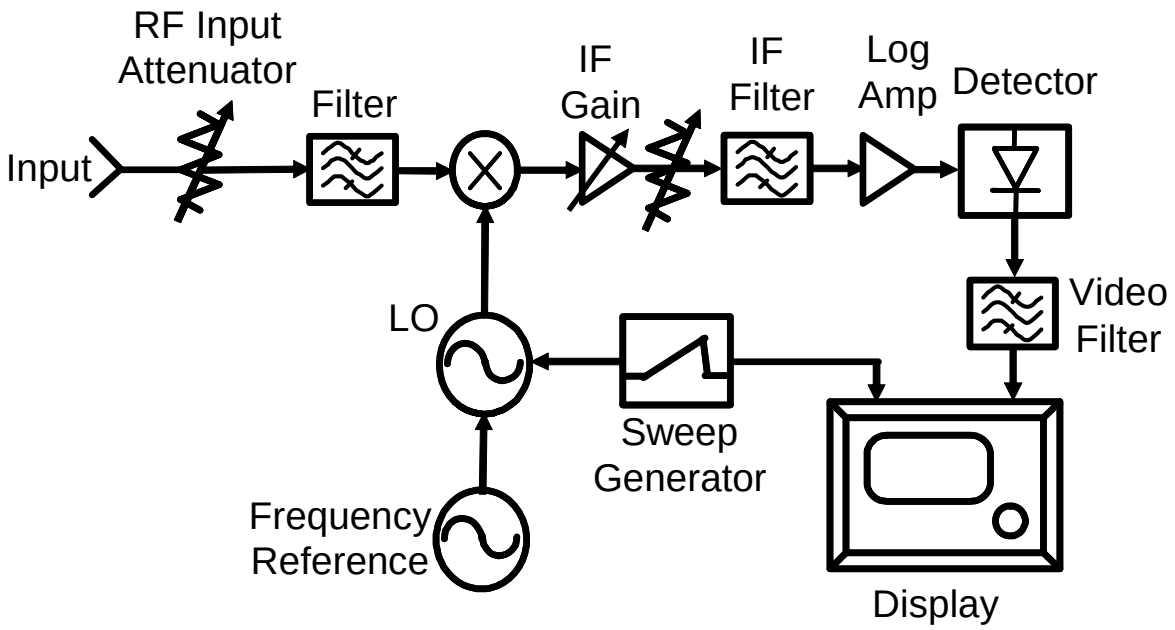


The 2nd-order filter is the highest order passive RC filter that can be built without series resistors between the charge pump and the VCO tune line

$$F(s) = \frac{(1 + sC_1R)}{s(C_1 + C_2)(1 + sC_sR)}$$

$$C_s = \frac{C_1C_2}{C_1 + C_2}$$

Spectrum analyzer basic block diagram

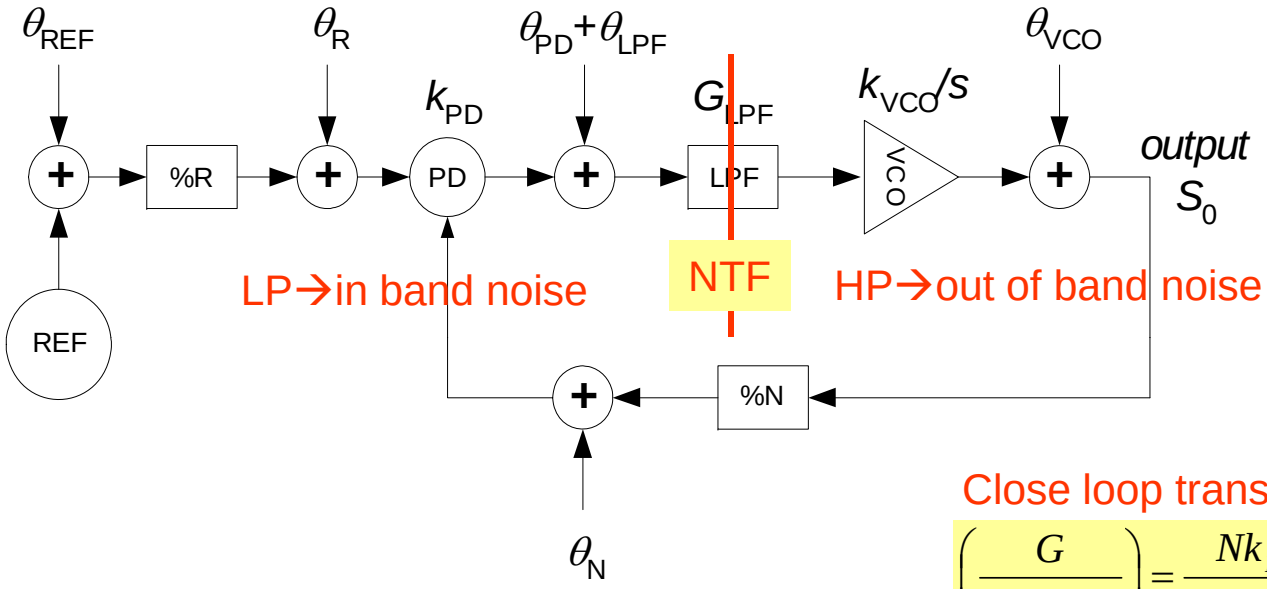


Getting the Best Sensitivity Requires Three Settings

- Narrowest resolution bandwidth
- Minimum RF attenuation
- Sufficient video filter to smooth noise (VBW < 0.01 Resolution BW)

PLL Phase Noise Sources

$$G(s) = k_{PD} G_{LPF} k_{VCO} / s$$



Close loop transfer function

$$\left(\frac{G}{1+G/N}\right) = \frac{N k_{PD} G_{LPF} k_{VCO}}{Ns + k_{PD} G_{LPF} k_{VCO}}$$

Total output noise power spectral density

$$S_0(f) = \left[\frac{S_{REF}}{R^2} + S_R + S_N + \frac{S_{PD} + S_{LPF}}{k_{PD}^2}\right]\left(\frac{G}{1+G/N}\right)^2 + S_{VCO}\left(\frac{1}{1+G/N}\right)^2$$

LPF

HPF

$$\left(\frac{1}{1+G/N}\right) = 1 - \frac{1}{N}\left(\frac{G}{1+G/N}\right)$$

In-band PLL Phase Noise

$$S_0(f)=\left[\frac{S_{REF}}{R^2}+S_R+S_N+\frac{S_{PD}+S_{LPF}}{k_{PD}^2}\right]\left(\frac{Nk_{PD}G_{LPF}k_{VCO}}{Ns+k_{PD}G_{LPF}k_{VCO}}\right)^2 \underset{s\to 0}{\rightarrow}\left[\frac{S_{REF}}{R^2}+S_R+S_N+\frac{S_{PD}+S_{LPF}}{k_{PD}^2}\right]N^2$$

PLL magnifies the noise from the reference, phase detector, LPF and the dividers by the amount of 20logN dB → Smaller N leads to lower in-band noise.

For integer-N Synthesizer: output frequency Fo=Fref*N, step size = Fref → cannot simultaneously achieve fine step size and small N. → poor in-band noise performance.

For fractional-N Synthesizer: output frequency Fo=Fref*(N+K/F), step size = Fref/F → can achieve fine step size and small N simultaneously. → better in-band noise performance.

Out-Of-Band PLL Phase Noise

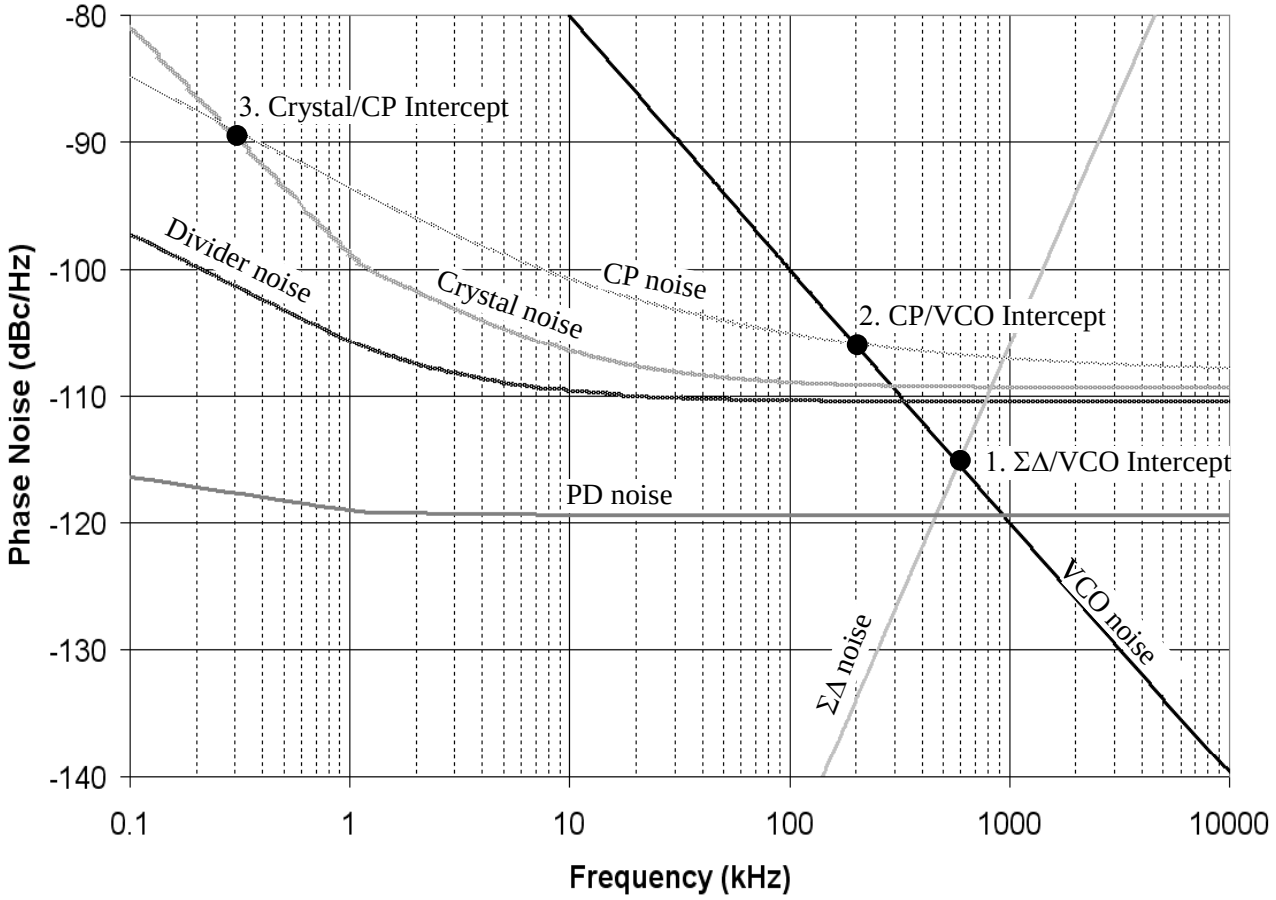
The noise outside of the PLL bandwidth is determined by the VCO phase noise, namely,

$$S_0(f) = S_{VCO}\left(\frac{1}{1+k_{PD}G_{LPF}k_{VCO}/Ns}\right)^2 \underset{s\to\infty}{\rightarrow} S_{VCO}$$

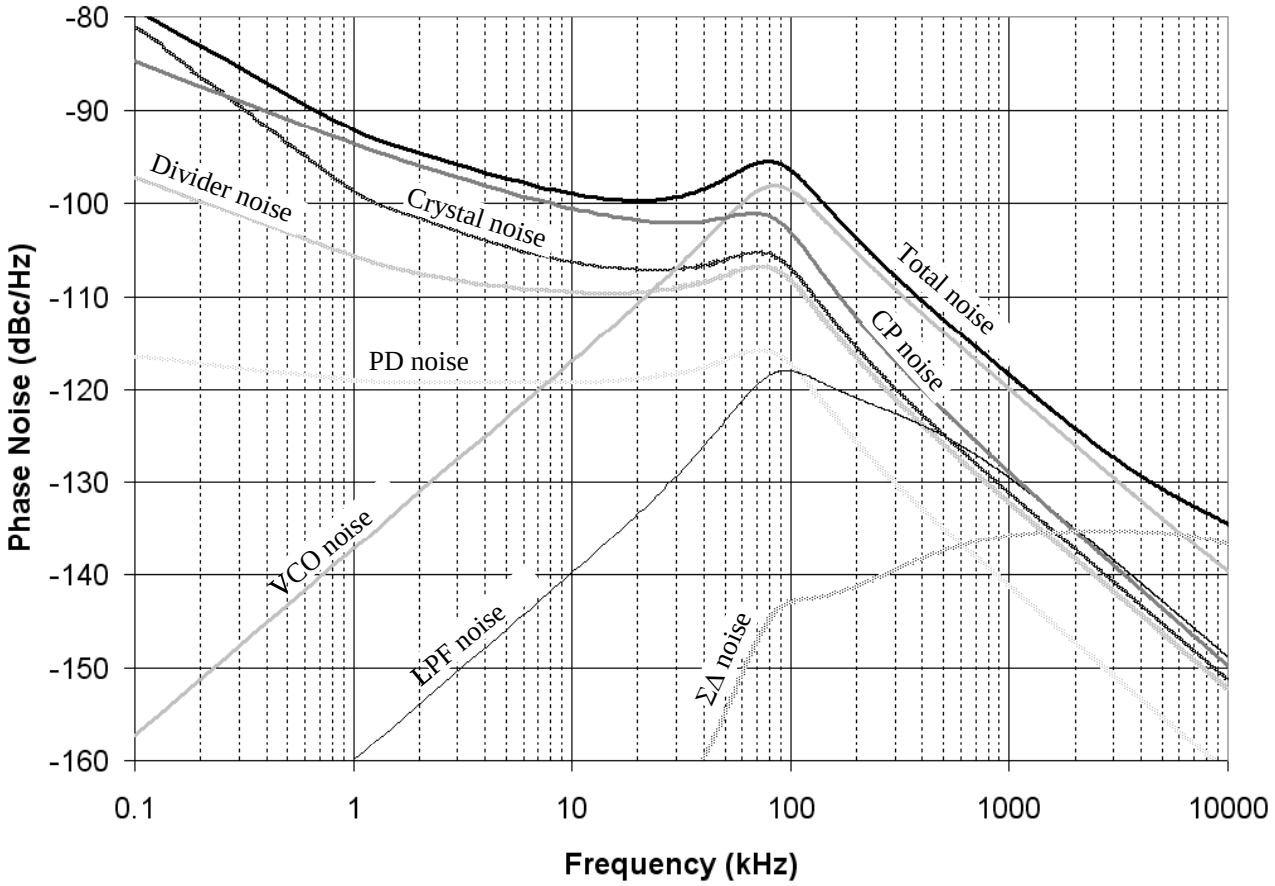
$$S_{VCO}(\Delta f) = 10\log\left\{\frac{FkT}{2P_s}\left[1+\left(\frac{f_0}{2\Delta f\cdot Q_L}\right)^2\right]\cdot\left[1+\frac{f_c}{|\Delta f|}\right]\right\}$$

Flicker 1/f noise is caused by trapping in the semiconductor material. Flicker noise corner fc is an empirical parameter depending on the device size and processing. For CMOS, fc is found to be 3~7 kHz typically and for bipolar transistors fc is about as 50 kHz. Notice that fc has impact only on close-in noise. Q_L is the loaded Q of the resonant circuit, ranging from 5~20 for on-chip resonator and 40~80 for off-chip tank. Ps is the average signal power at output of the oscillator active device, and F is oscillator effective noise factor.

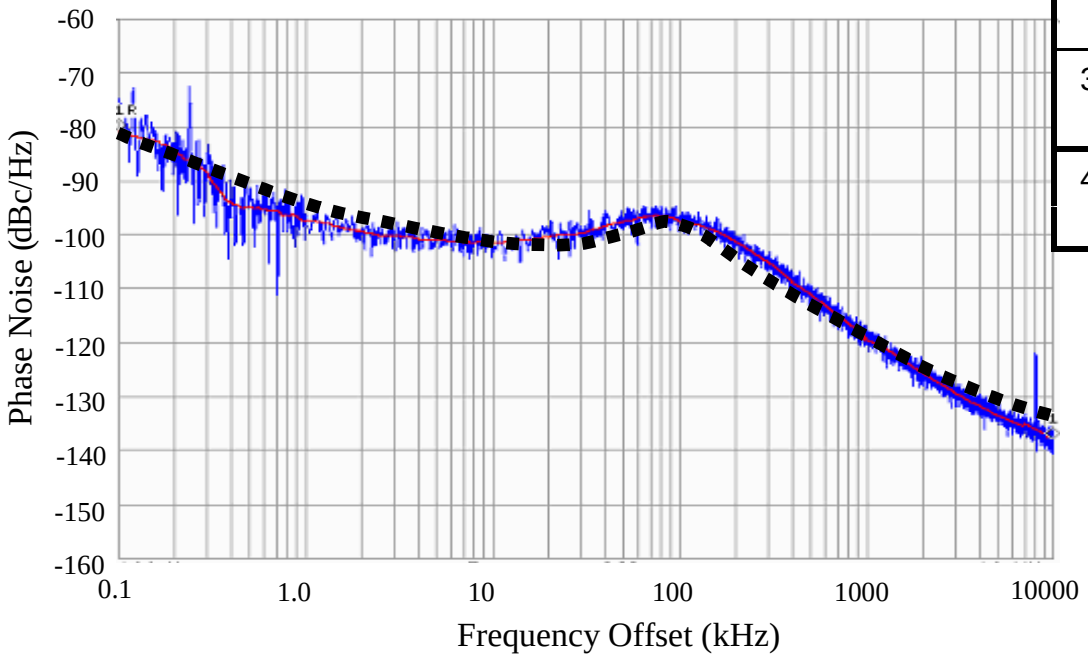
Simulated PLL Phase Noise Sources



Simulated PLL Phase Noise With Loop Effect



Comparison of measured and simulated phase noise



Frequency Band	Simulated Phase Noise	Measured Phase Noise
3.2-3.3GHz	0.44°rms	0.50°rms
4.1-4.3GHz	0.50°rms	0.535°rms

Parameter	Value
C_1	3nF
C_2	600pF
R	600Ω

References

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