RFIC Design and Testing for Wireless Communications

A PragaTI (TI India Technical University) Course
July 18, 21, 22, 2008

Lecture 7: RF front-end design – LNA, mixer

By

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RFIC Design and Testing for Wireless Communications

Topics

Monday, July 21, 2008

9:00 – 10:30	Introduction – Semiconductor history, RF characteristics
11:00 – 12:30	Basic Concepts – Linearity, noise figure, dynamic range
2:00 – 3:30	RF front-end design – LNA, mixer
4:00 – 5:30	Frequency synthesizer design I (PLL)

Tuesday, July 22, 2008

9:00 – 10:30	Frequency synthesizer design II (VCO)
11:00 – 12:30	RFIC design for wireless communications
2:00 – 3:30	Analog and mixed signal testing

LNA Design Challenges

(1) Amplify extremely low signals without adding much noise.

(2) Amplify large signals without distortions.

(3) Variable gain to compensate large input signal variation.

(4) Input matching and flat gain over wide bandwidth for muti-mode transceivers.

(5) Input dynamic range of a WLAN LAN from -80dBm to -20dBm

Parameters for Microwave and RFIC Design

Peak-to peak voltage: V_{pp}

Root-mean-square voltage:

$$V_{rms} = \frac{V_{pp}}{2\sqrt{2}}$$

Power in Watt :

$$Pwatt = \frac{V^2_{rms}}{R} = \frac{V^2_{pp}}{8R}$$

Power in dBm :

$$P_{dBm} = 10\log_{10}\left(\frac{Pwatt\,[mW]}{1mW}\right)$$

Refection coefficient :

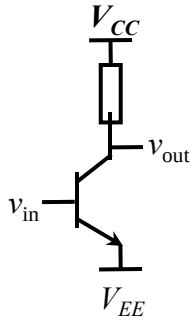
$$\Gamma = S_{11} = \frac{Z_{in} - R_S}{Z_{in} + R_S} \qquad \text{Return loss} = -20\log|\Gamma|$$

Voltage standing wave ratio (VSWR):

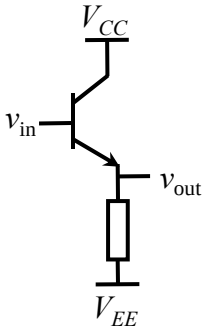
$$VSWR = \frac{V_{\max}}{V_{\min}} = \frac{1+|\Gamma|}{1-|\Gamma|}$$

Basic Amplifiers

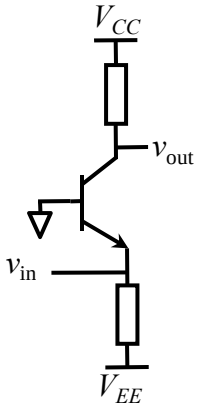
- The common emitter amplifier is often used as a drive for an LNA.
- The common-collector, with high input impedance and low output impedance, makes an excellent buffer between stages or before the output driver.
- The common-base is often used as a cascode in combination with the common-emitter to form a LNA stage with gain to high frequency.



Common-Emitter (LNA Driver)

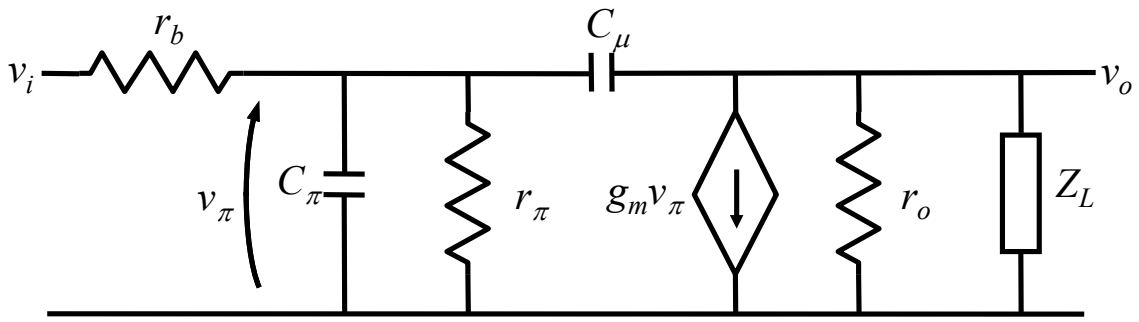


Common-Collector (Buffer)



Common-Base (Cascode)

Common-Emitter Amplifier



- Voltage gain

$$A_{vo} = \frac{v_o}{v_i} = -\frac{r_\pi}{r_b + r_\pi} g_m Z_L \approx \frac{Z_L}{r_e}$$

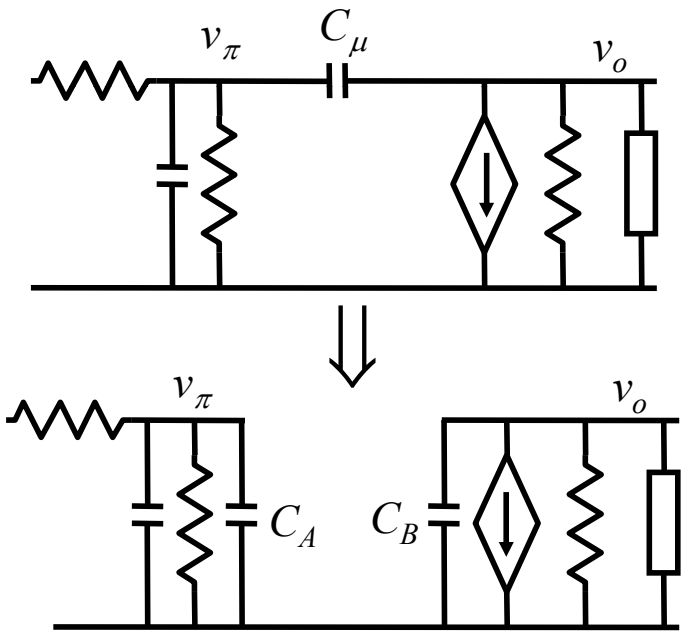
- Note that $r_\pi = \beta r_e$ and $g_m = 1/r_e$. for low frequencies, the parasitic capacitances have been ignored and $r_b << r_\pi$.

- Input impedance at low frequencies

$$Z_{in} = r_b + r_\pi$$

Miller Capacitance in Common-Emitter Amplifier

C_μ is replaced with two equivalent capacitors C_A and C_B



$$C_A = C_\mu\left(1-\frac{v_o}{v_\pi}\right) = C_\mu(1+g_m Z_L) \approx C_\mu g_m Z_L$$

$$C_B = C_\mu\left(1-\frac{v_\pi}{v_o}\right) = C_\mu\left(1+\frac{1}{g_m Z_L}\right) \approx C_\mu$$

- Two RC time constants or two poles: one consisting of $C_A + C_\pi$, and the other consisting C_B.

Miller Capacitance in Common-Emitter Amplifier

- The dominant pole is one formed by C_A and C_π:

$$f_{P1} = \frac{1}{2\pi \cdot \left[r_\pi \| (r_b + R_s)\right] \cdot \left[C_\pi + C_A\right]}$$

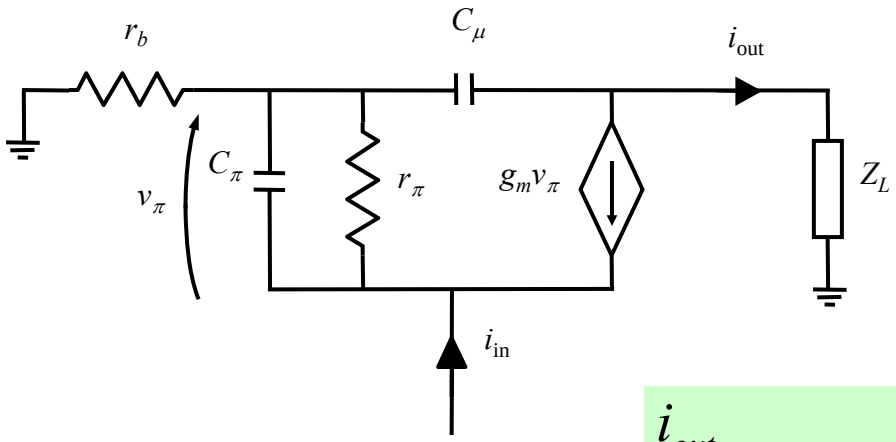
- Recall F_t calculation, the output is loaded with a short circuit → removes Miller multiplication, 3db current gain bandwidth:

$$f_\beta = \frac{1}{2\pi \cdot r_\pi (C_\pi + C_\mu)}$$

The unity current gain frequency:

$$f_T = \frac{g_m}{2\pi \cdot (C_\pi + C_\mu)}$$

Common-Base Amplifier



$$\frac{i_{out}}{i_{in}} \approx \frac{1}{1+j\omega C_\pi r_e} \approx \frac{1}{1+j\dfrac{\omega}{\omega_T}}$$

Current gain (ignoring C_u and r_o)

$$A_v \approx \frac{\alpha_0 R_L}{R_S} \cdot \frac{1}{1+j\omega r_e C_\pi} \cdot \frac{1}{1+j\omega R_L\left(C_\mu + C_{CS}\right)}$$

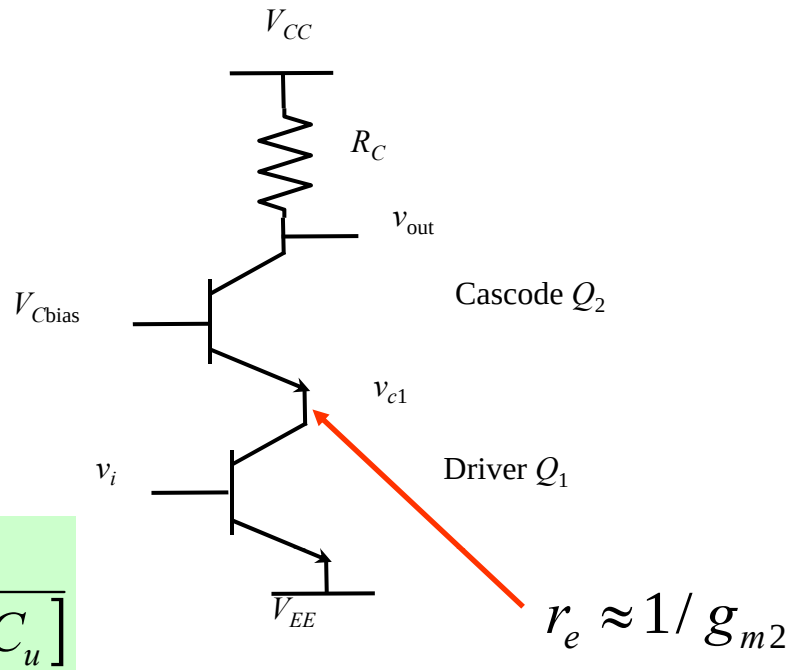
At low frequencies, the current gain = 1.

The pole in this equation is usually at much higher frequency than the one in the common-emitter amplifier

$$r_e < r_b + R_S$$

Cascode LNA

$$v_o / v_i \approx -g_m R_C$$

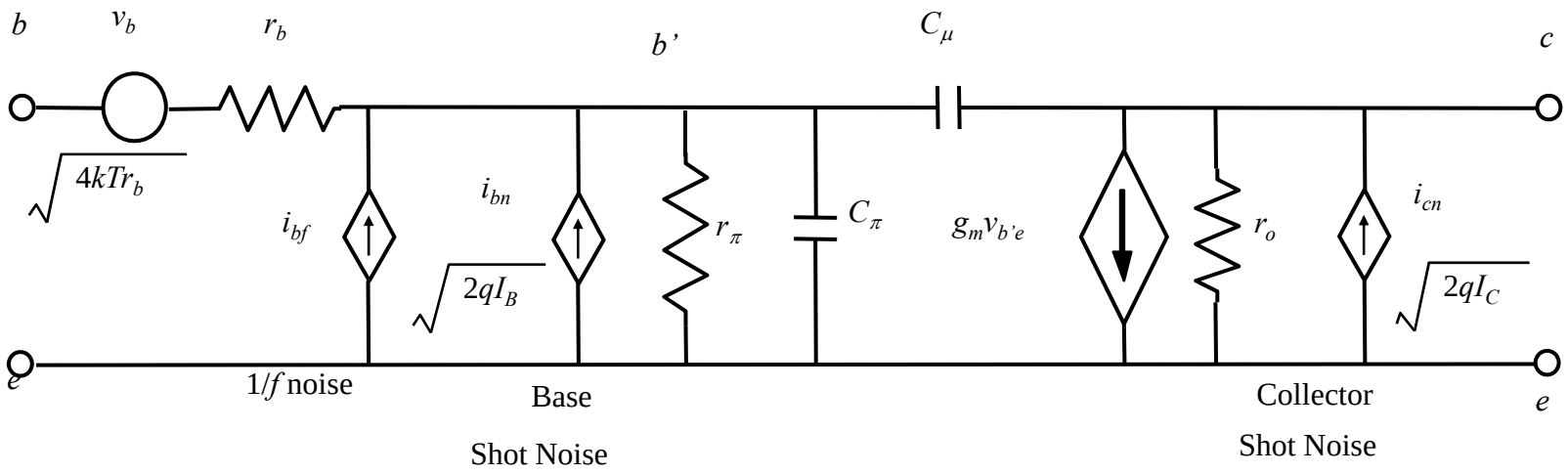


Common emitter dominant pole

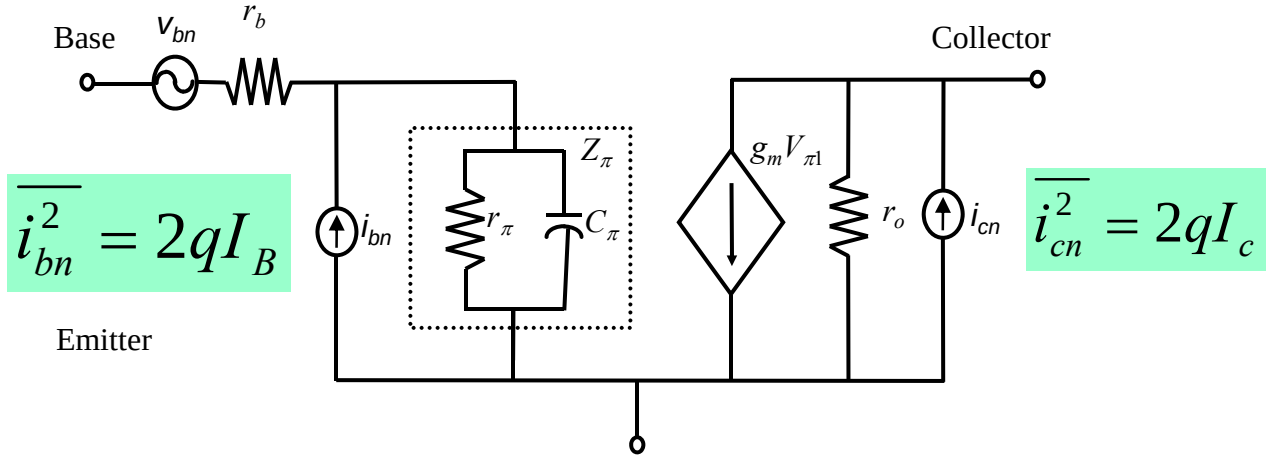
$$f_{P1} = \frac{1}{2\pi \cdot \left[r_{\pi 1} \| (r_{b1} + R_s)\right] \cdot \left[C_\pi + 2C_u\right]}$$

- Current *ic1* through *Q1* is about the same as the current i***c2*** through *Q2* ← current gain ~1 → Gain is the same as for the common-emitter amplifier.
- The cascode transistor reduces the feedback of *Cu1* (why?) → increased high frequency gain.
- Cascode has good isolation with reduced S_{12}.
- Disadvantage: cascode transistor uses voltage headroom → reduced linearity; add another pole to the amp → -12dB/oct roll-off; add little extra noise (to the 1st order approximation, cascode NF = common emitter NF); common base may cause noise and oscillation.

Bipolar Transistor Noise Model



$$\overline{v_{bn}^2} = 4kTr_b$$

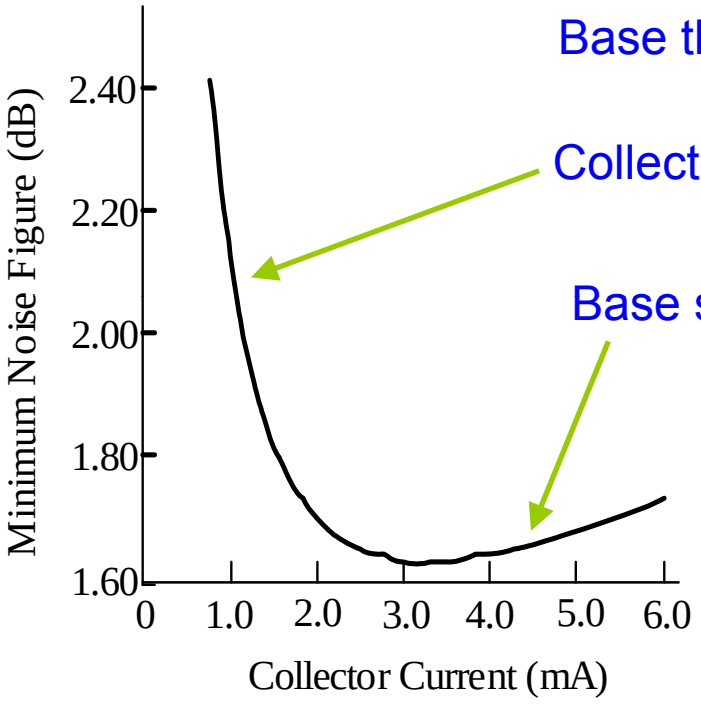


$$\overline{i_{bn}^2} = 2qI_B$$

Emitter

$$\overline{i_{cn}^2} = 2qI_c$$

Noise Figure versus Bias Current



Output signal $v_{so} \approx v_{si} \cdot g_m R_L$

Base thermal noise $v_{no,r_b} \approx \sqrt{4kTr_b} \cdot g_m R_L$

Collector shot noise $v_{no,I_c} \approx \sqrt{2qI_C} R_L$

Base shot noise $v_{no,I_B} \approx \sqrt{\frac{2qI_C}{\beta}} R_s g_m R_L$

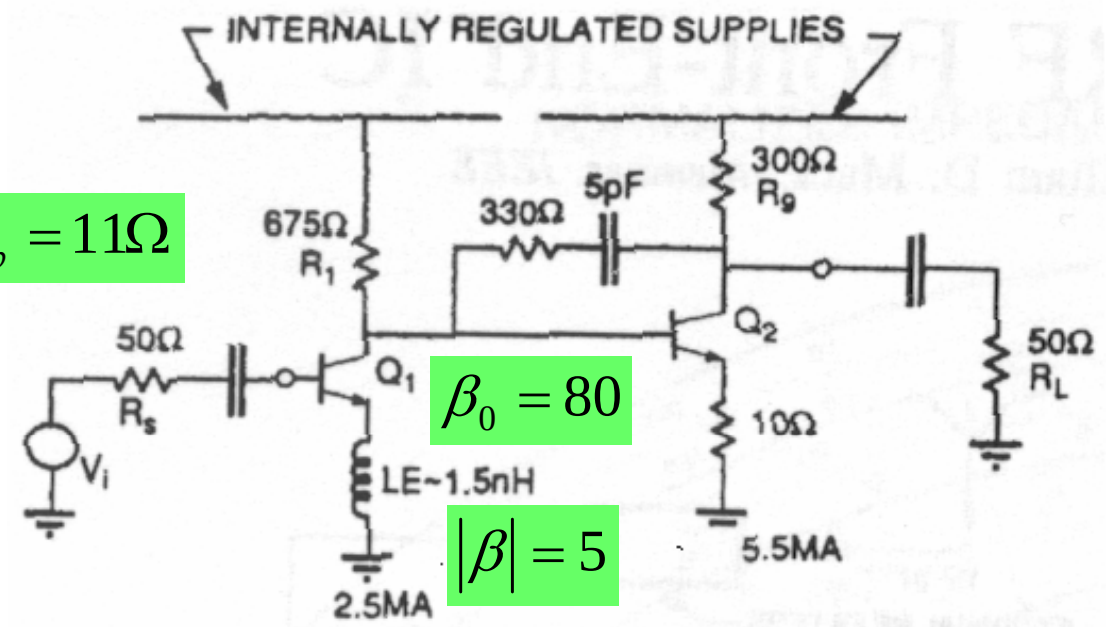
base thermal noise

base shot noise

collector shot noise (correlated)

$$NF = 1 + \frac{R_{eq}}{R_S} = 1 + \frac{r_b}{R_S} + \frac{1}{2g_m R_S} + \frac{g_m R_S}{2\beta_0} + \frac{g_m R_S}{2|\beta|^2}$$

Noise Figure of A Two Stage LNA



$r_b = 11\Omega$

$\beta_0 = 80$

$|\beta| = 5$

$f_t = 5GHz$

$f_{in} = 1GHz$

$g_m = 0.1\Omega^{-1}$

$$NF = 1 + \frac{r_b}{R_S} + \frac{1}{2g_m R_S} + \frac{g_m R_S}{2\beta_0} + \frac{g_m R_S}{2|\beta|^2}$$

$$= 1 + \frac{11}{50} + \frac{1}{10} + \frac{5}{160} + \frac{5}{50} = 1.62dB$$

NF dominated by base resistance

NF increases at high frequency

Minimum Noise Figure of Common Emitter LNA

$$NF = 1 + \frac{r_b}{R_S} + \frac{1}{2 g_m R_S} + \frac{g_m R_S}{2\beta_0} + \frac{g_m R_S}{2|\beta|^2} = 1 + a\frac{1}{R_S} + b \cdot R_S$$

$$\frac{dNF}{dR_S} = -a\frac{1}{R_S^2} + b = 0$$

$$R_{S,opt} = \sqrt{\frac{a}{b}} = \frac{1}{g_m}\sqrt{\frac{1 + 2 g_m r_b}{\frac{1}{\beta_0} + \frac{1}{|\beta|^2}}} \approx \frac{f_T}{f}\sqrt{\frac{2 r_b}{g_m}}$$

R_S=50 Ohm → choose bias (g_m) and emitter length to achieve noise matching

$$NF_{\min} = 1 + 2\sqrt{ab} = 1 + \sqrt{(1 + 2 g_m r_b)\left(\frac{1}{\beta_0} + \frac{1}{|\beta|^2}\right)}$$

More on LNA Noise Figure

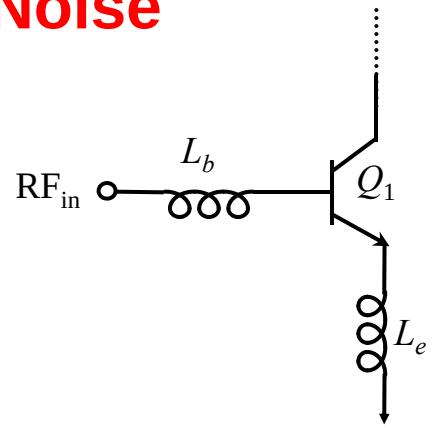
$$NF = NF_{\min} + \frac{b}{R_S}\left(R_S - R_{S,opt}\right)^2 \approx NF_{\min} + \frac{f^2 g_m}{2 f_T^2 R_S}\left(R_S - R_{S,opt}\right)^2$$

$\text{High frequency}, R_{S,opt} \approx \frac{f_T}{f}\sqrt{\frac{2r_b}{g_m}}$	$NF_{\min} \approx 1 + C_\pi \omega \sqrt{\frac{2r_b}{g_m}}$
$\text{Low frequency}, R_{S,opt} \approx \sqrt{\frac{2r_b\beta_0}{g_m}}$	$NF_{\min} \approx 1 + \sqrt{\frac{2g_m r_b}{\beta_0}}$

- For a given technology, NF_{min} is a strong function of bias current.
- For low operation frequency, NF_{min} can be reduced by increasing emitter length.
- For high operation frequency, NF_{min} is a weak function of emitter length. Increase device size does reduce r_b, yet capacitance also increase.
- For high operation frequency, NF_{min} degrades as frequency increases.

Input Matching of LNA Noise

Power matching:



- Input impedance (assuming C_u and r_π is not significant):

$$Z_{in} = j\omega L_b + r_b - \frac{j}{\omega C_\pi} + j\omega L_e + \frac{g_m L_e}{C_\pi}$$

- Power matching: Real part=R_s

$$\frac{g_m L_e}{C_\pi} + r_b = R_S \longrightarrow L_e = \frac{(R_S - r_b)C_\pi}{g_m} \approx \frac{R_S}{\omega_T}$$

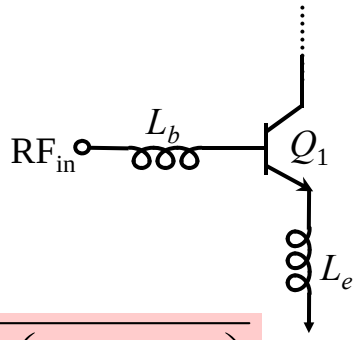
Imaginary part=0

$$L_e + L_b = \frac{1}{\omega^2 C_\pi} \longrightarrow L_b = \frac{1}{C_\pi \omega^2} - \frac{(R_S - r_b)C_\pi}{g_m} \approx \frac{\omega_T}{g_m \omega^2} - \frac{R_S - r_b}{\omega_T}$$

- If C_u is considered, $C_\pi$replaced by $C_\pi + C_A$, and therefore a larger inductor is required for matching.

$$C_A = C_\mu(1 + g_m Z_L) \approx C_\mu g_m Z_L$$

LNA Design Steps



(1) Noise matching: sizing the transistor (emitter length) and adjusting bias current to achieve minimum NF

$$R_{S,opt} = \frac{1}{g_m}\sqrt{\frac{1+2g_m r_b}{\frac{1}{\beta_0}+\frac{1}{|\beta|^2}}} = 50\Omega$$

$$NF_{\min} = 1+\sqrt{(1+2g_m r_b)\left(\frac{1}{\beta_0}+\frac{1}{|\beta|^2}\right)}$$

(2) Power matching: adjusting L_e such that the real part of the LNA input impedance equals to 50 Ohm. For 5AM, Le is about 0.2nH → Use multiple downbonds to reduce the package effect.

$$L_e = \frac{R_S}{\omega_T} = \frac{50}{\omega_T}$$

(3) Power matching: adding L_b such that the imaginary part of the LNA input impedance equals to zero

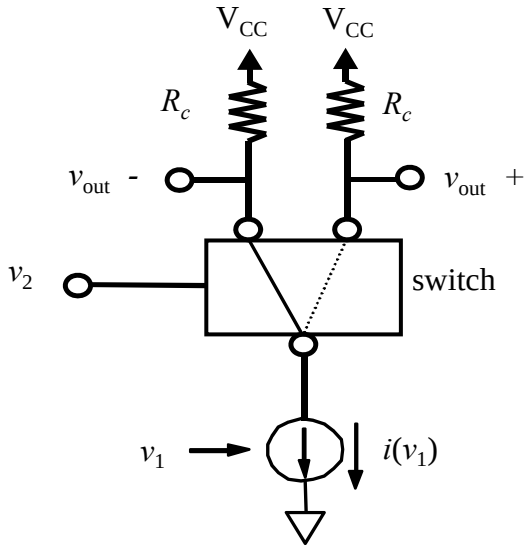
$$L_b \approx \frac{\omega_T}{g_m \omega^2}$$

(4) Gain/bandwidth: Choosing load tank to meet gain and bandwidth requirements.

(5) Using SPICE sim to fine tune the component values, iterations to trade off the various parameters are expected.

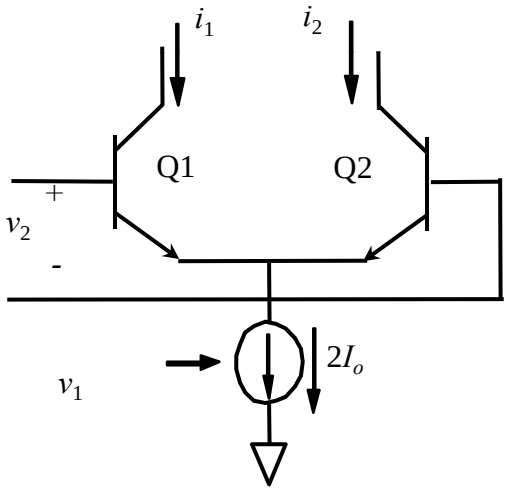
Mixing with Nonlinearity

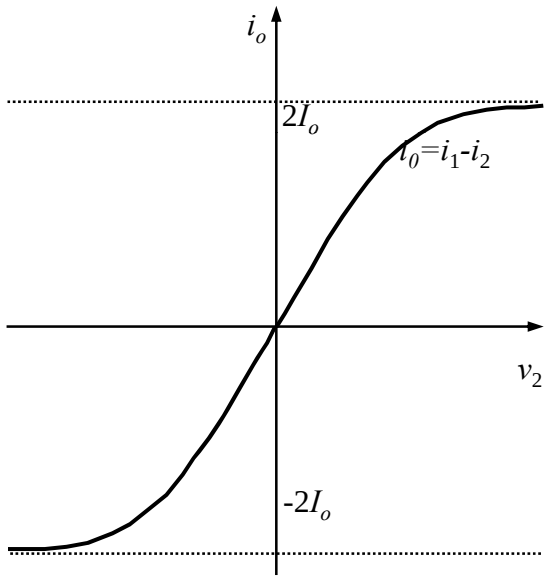
- Mixer is to convert a signal from one frequency to another → intrinsically needs a nonlinear transfer function. A diode or a transistor can be used as a nonlinear device.
- Two inputs at ω_1 and ω_2 , which are passed through a nonlinearity multiplier will produce mixing terms at $\omega_1 \pm \omega_2$ →with other terms (harmonics, feed-through, intermodulation) that need to be filtered out.
- Mixers (multiplier) can be made from an amplifier with a controlled switch.



Controlled Transconductance Mixer

- The current is related to the input voltage *V2* by the transconductance of the input transistors Q1 and Q2. The transconductance is controlled by the current I_0, which in turn is controlled by the input voltage *V1*.





$$i_1 = \frac{I_O}{1+e^{-v_2/v_T}}$$

$$i_2 = \frac{I_O}{1+e^{v_2/v_T}}$$

Controlled Transconductance Mixer

$$i_o = i_1 - i_2 = I_o\left(\frac{I_O}{1+e^{-v_2/v_T}} - \frac{I_O}{1+e^{v_2/v_T}}\right) = I_o \tanh\frac{v_2}{2v_T}$$

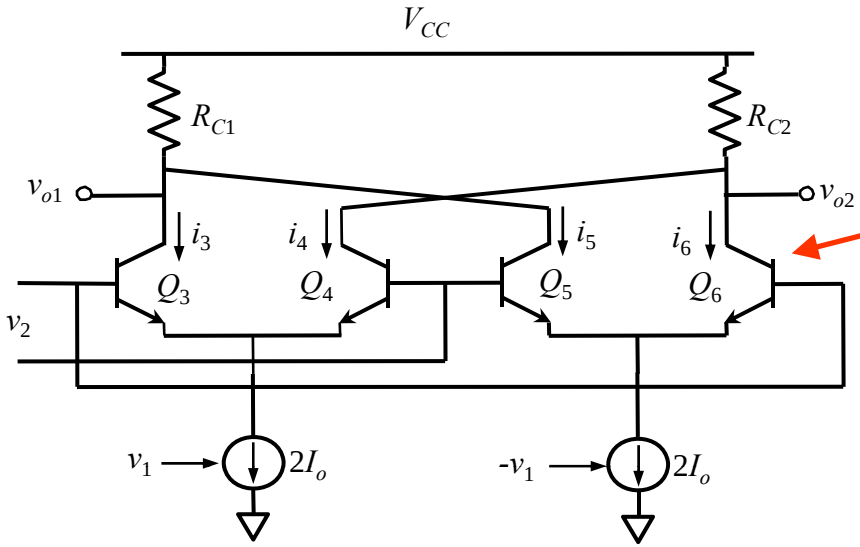
- If $v_2 << v_T$ $\quad i_o \approx I_o \frac{v_2}{2v_T}$

- Current source is modulated by small v_1 → I_o is replaced with $I_o + g_{mc}v_1$, where g_{mc} is transconductance of the current source:

$$i_o = (I_o + g_{mc}v_1)\tanh\frac{v_2}{2v_T} = \underbrace{I_o \tanh\frac{v_2}{2v_T}}_{V_2 \quad feedthrough} + \underbrace{g_{mc}v_1 \tanh\frac{v_2}{2v_T}}_{multiplication \ (mixing)}$$

not appear in differential output voltage → double balanced mixer

Double-balanced Mixer



- Use switching quad to eliminate the v_2 feedthrough

- 2nd pair current:

$$i_o^{'} = i_6 - i_5 = I_o \tanh\frac{v_2}{2v_T} - g_{mc} v_1 \tanh\frac{v_2}{2v_T}$$

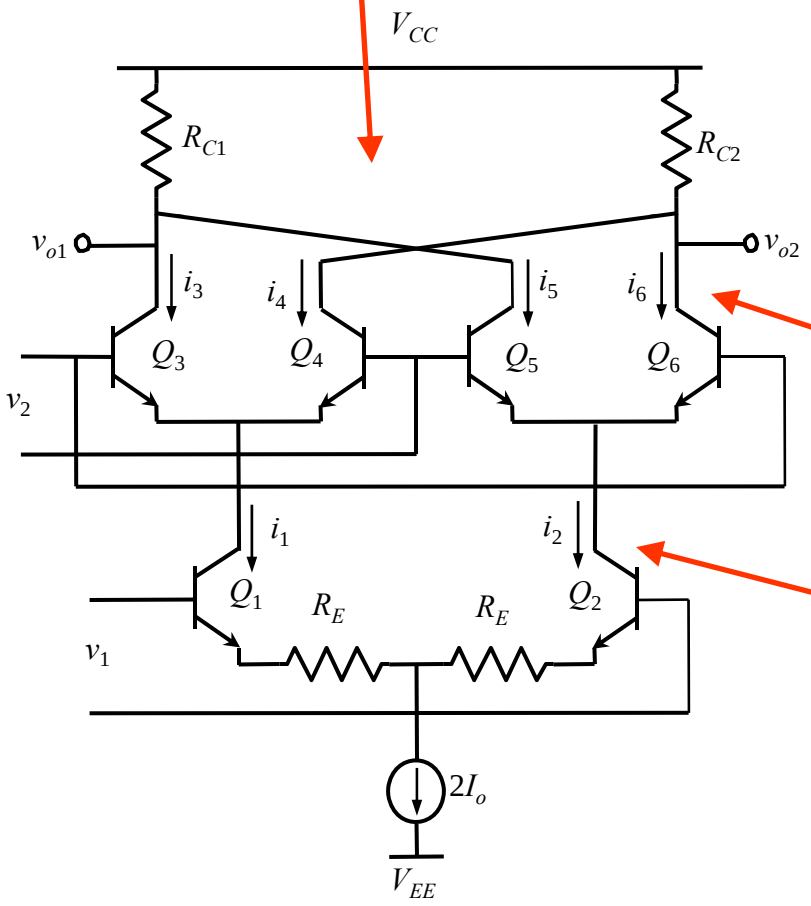
- Total differential current:

$$i_{ob} = i_o - i_o^{'} = 2g_{mc} v_1 \tanh\frac{v_2}{2v_T}$$

Double-balanced Mixer

$$(i_3 + i_5) - (i_4 + i_6) = \tanh\left(\frac{v_2}{2v_T}\right)(i_1 - i_2) = \tanh\left(\frac{v_2}{2v_T}\right)\frac{v_1}{r_e + R_E}$$

Assuming small signal for V_1



$$i_3 = \frac{i_1}{1 + e^{-v_2/v_T}} \qquad i_4 = \frac{i_1}{1 + e^{v_2/v_T}}$$

$$i_5 = \frac{i_2}{1 + e^{v_2/v_T}} \qquad i_6 = \frac{i_2}{1 + e^{-v_2/v_T}}$$

$$i_1 \approx I_o + \frac{v_1}{2}\frac{1}{r_e + R_E}$$

and

$$i_2 = I_o - \frac{v_1}{2}\frac{1}{r_e + R_E}$$

Double-balanced Mixer

- Output differential voltage

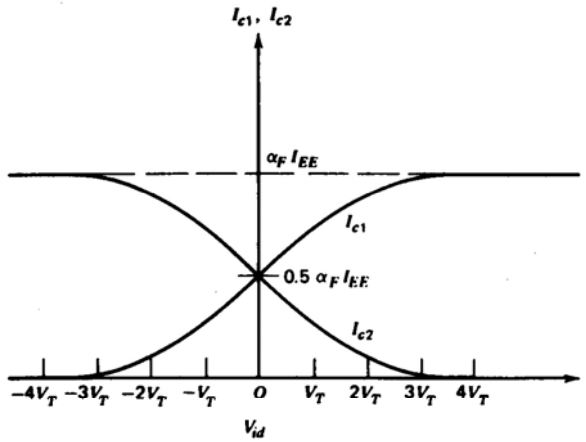
$$v_o = -\tanh\left(\frac{v_2}{2v_T}\right)\frac{v_1}{r_e + R_E}R_C$$

- Conversion gain relative to v_1

$$\frac{v_o}{v_1} = -\tanh\left(\frac{v_2}{2v_T}\right)\frac{R_C}{r_e + R_E}$$

- With R_E=0, a general large-signal expression for the output:

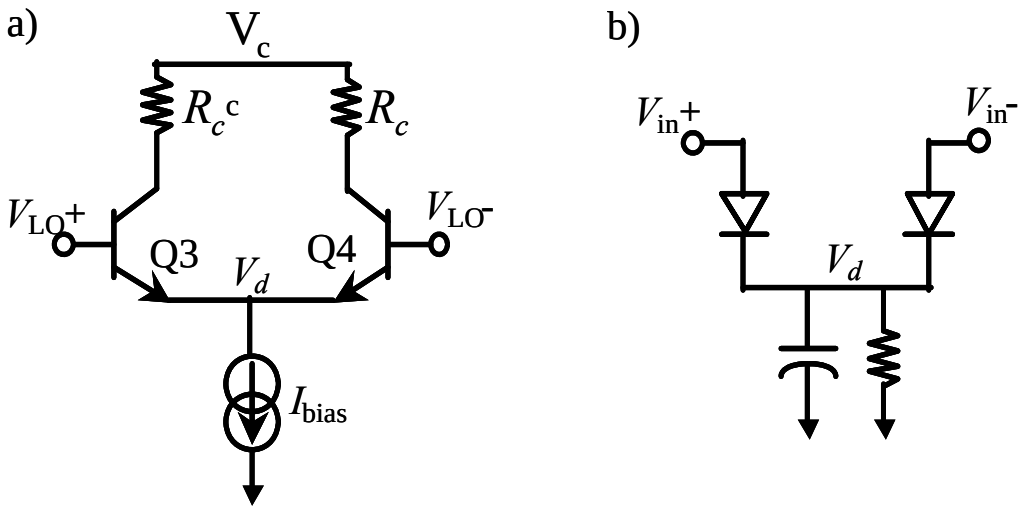
$$v_o = -2R_C I_o \tanh\left(\frac{v_1}{2v_T}\right)\tanh\left(\frac{v_2}{2v_T}\right)$$



LO Level at Upper Quad Transistors

- The differential pair needs an input voltage swing of about 4 to 5 v_T for the transistors to be hard-switched one way or the other.
- LO input to the mixer should be at least 100mV peak for complete switching. At 50Ω, 100mV peak is -10 dBm.
- -10 to 0 dBm (100~300 mVpp = 200~600mVpp diff) is a reasonable compromise between noise figure, gain and required LO power. This is also the reasonable level for all switching circuits
- If the LO voltage is too large, large current has to be moved into and out of the bases of the transistors during transition → lead to spikes in the signals and reduce the switching speed → cause an increase in LO feed-through.
- Large LO also pushes switching transistor into saturation → loose switching speed and inject mixer noise into substrate.

w1



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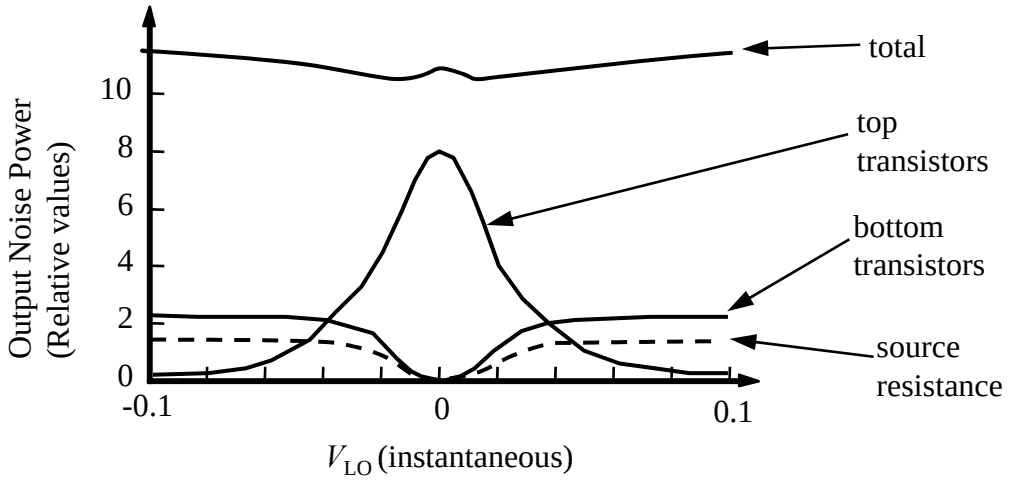
Mixer Noise

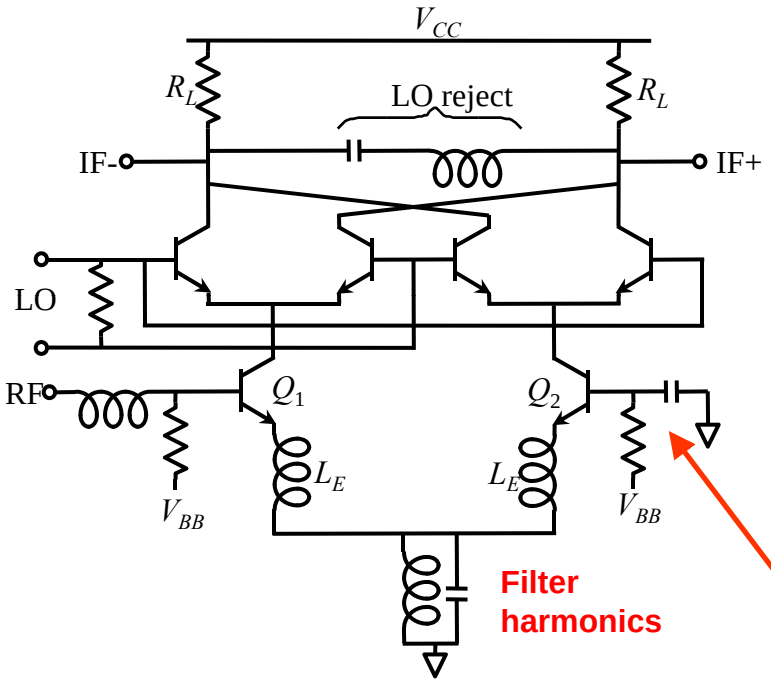
$$NF = 10\log\frac{N_{0tot}}{N0(source)}$$
$$= 10\log\frac{11}{1.5} = 8.65dB$$



- Top transistor contributes significant noise during transition and contributes ignorable noise when fully switched, either in cutoff or saturation (without gain).
- Gain from RF input is maximum when top transistors are fully switched (cascode).
- → need sharp transition buffer for LO → large LO such that minimal time is spent around 0V.
- Mixer noise figure can be approximately analyzed using a lowly swept dc voltage at the LO input or with an actual LO signal.
- With a slowly swept dc voltage, the mixer becomes equivalent to a cascode amplifier and the LO input served as a gain-controlling signal.
- For mixer, any noise (or signal) is mixed to two output frequencies, thus reducing the output level → mixer having less gain than the equivalent differential pair.
- However, both RF and image is mixed to IF → doubling noise power at output.

Mixer with Simultaneous Noise and Power Match

- Use inductor degeneration and inductor input achieving simultaneous noise and power matching similar to that of a typical LNA.



$$L_E = \frac{Z_0}{2\pi f_T}$$

$$IIP3 \approx \frac{\omega g_m Z_0}{2\pi f_T}$$

Single-to-differential

- Noise matching: sizing L_E, and RF transistor, and operating the RF transistors at the current required for minimum NF.
- The quad switching transistors are sized for maximum f_T, (typically about five to ten times smaller than the RF transistors.)

Mixer Design Issues

Sizing Transistors

- The RF differential pair is basically an LNA stage, and the transistors and associated passives can be optimized using the LNA design techniques.
- The switching quad transistors are sized so that they operate close to their peak f_T at the bias current that is optimal for the differential pair transistors are biased at their minimum noise current, then the switching transistors end up being about one-eighth the size.

Increasing Gain

- Voltage gain without matching and assuming full switching of the upper quad:

$$v_o = \frac{2}{\pi} \frac{R_C}{r_e + R_E} v_{in}$$

- To increase the gain → increase the load resistance R_C, to reduce degeneration resistance R_E, or to increase the bias current I_B.
- Make sure that increasing output voltage swing will not cause the switching transistors to become saturated.→ Enough headroom.

Mixer Design Issues

Increasing IP3

- Identify which part of the circuit is compressing. Compression can be due to overdriving of the lower differential pair, clipping at the output, or the LO bias voltage being too low, causing clipping at the collectors of the bottom differential pair. Adjust the bias and voltage swing to avoid clipping.
- 1. If the compression is due to the bottom differential pair (RF input), then linearity can be improved by increasing R_E or by increasing bias current.
- 2. Compression caused by clipping at the output is typically due to the quad transistors going into saturation. Saturation can be avoided by reducing the load resistance or adjust the quad transistor bias. Too large LO will also cause saturation.
- 3. If compression is caused by clipping at the collector of the RF input differential pair, then increasing the LO bias voltage will improve linearity; however, this may result in clipping at the output.

Improving Noise Figure

- **NF will be largely determined by the choice of topology.**
- **Use the simultaneous matched design technique.**
- **To minimize noise, the emitter degeneration resistor should be kept as small as possible. Use inductor as degeneration to achieve low noise.**
- **Make top transistors switching fast.**

Mixer Design Issues

Matching, Bias Resistors, and Gain

- Use resistive matching to achieve broad band. For a resistively degenerated mixer, the RF input impedance will be fairly high; for example, with $R_E = 100\ \Omega$, Z_{in} can be of the order of a Kilo Ohm → easier for LNA output stage to drive the mixer.
- At the output, if matched, the load resistor Ro is equal to the collector resistor R_C. Furthermore, to convert from voltage gain Av to power gain Po/Pi, one must consider the output resistance R_i and load resistance $R_o = R_C$ as follows:

$$\frac{P_o}{P_i} = \frac{\frac{v_o^2}{R_o}}{\frac{v_i^2}{R_i}} = \frac{v_o^2}{v_i^2}\frac{R_i}{R_o} = A_v^2 \frac{R_i}{R_o} \approx \left(\frac{2}{\pi}\frac{R_C/2}{R_E}\right)^2 \frac{R_i}{R_C}$$