Timing Simulation of 45 nm Technology and Analysis of Gate Tunneling Currents in 90, 65, 45, and 32 nm Technologies

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***Abstract*—A timing simulation is presented for a MOSFET implemented inverter and 2-input NAND gate in a 45 nm technology. Gate tunneling currents are characterized for technology nodes less than 180 nm and the temperature dependence of this leakage is discussed.**

I. Introduction

FORWARD progression in the MOS/VLSI industry is driven by the demand for faster circuit speed. An increase in MOSFET operating speed is often accomplished by decreasing channel length. As a result, the gate oxide thickness is often decreased proportionally as well. Two topics will be discussed in this paper. First, the delay of both an inverter and 2-input NAND gate for the 45 nm technology node will be presented. Second, the effects of leakage current due to gate tunneling currents as gate thickness is scaled down is examined. The temperature dependence of gate tunneling currents is also discussed. When the gate SiO_2 thickness is less than 2 nm the effects of carrier tunneling through the oxide begin to degrade the performance of the transistor [1]. The International Technology Roadmap for Semiconductors (ITRS) specifies the maximum allowed gate leakage current density (J_{limit}) for high- performance CMOS logic chips to be 188 A/cm^2 for 90 nm technology [2]. J_{limit} is defined at 300K. It can be seen that this limit is reached when the gate oxide thickness (t_{ox}) is scaled down to 1.5 nm [3]. Due to the demand of devices with a gate oxide thickness at or below 1.5 nm, the effects of temperature variation on gate tunneling current should be studied more thoroughly. In this paper a nMOSFET will be considered.

II. Timing Analysis of 45 nm Technology

A. FreePDK45 Library

The models (NMOS_VTL and PMOS_VTL) provided in the free open-source 45 nm library, FreePDK45, developed by NCSU were used in simulation of the inverter and the 2-input NAND gate. LTSpice was used to run the netlist file. The rise and fall time of all input stimuli were set to 1 ns and the supply voltage was set to 1.2 V.

B. MOSFET Inverter

For the simulation of the inverter the input alternates between VDD and ground at a frequency of 10 MHz. When the input to the inverter, Vin, changes from low to high, the output of the inverter, Vout, takes 7 ns to fall to a steady state value. However, when Vin changes from high to low, Vout takes 45 ns to rise to a steady state value. The netlist shown in Fig. 1 was used to generate the plot shown in Fig. 2.

```
*Main inverter netlist
.param supply=1.2
.include '180nm.lib'
.global Vdd Gnd
Vdd Vdd Gnd 'supply'
.include NMOS_VTL.inc
.include PMOS_VTL.inc
.tran 0 115ns 0 0.1ns
M1 Out In Gnd Gnd NMOS_VTL
M2 Out In Vdd Vdd PMOS_VTL
V1 In Gnd pulse(0 'supply' 10n 1n 1n 50n 100n)
.END
```

Fig. 1. Netlist for inverter

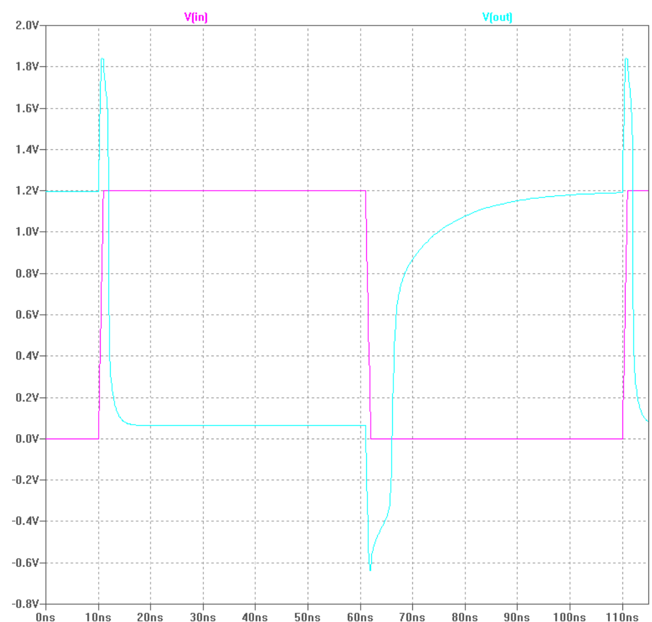

Fig. 2. Plot of Vin and Vout of inverter

C. 2-input NAND Gate

For the simulation of the 2-input NAND gate, input A alternates from high to low at a frequency of 2 MHz while input B is held high. A 17 ns delay is observed for the output to change from high to low and a 49 ns delay is observed for the output to change from low to high.

```
*Main 2 input nand gate netlist
.param supply=1.2
.include NMOS_VTL.inc
.include PMOS_VTL.inc
.options post
.tran 0 115ns 0 0.1ns
M1 VDD B Vout Vout PMOS_VTL
M2 VDD A Vout Vout PMOS_VTL
M3 Vout A N001 N001 NMOS_VTL
M4 N001 B 0 0 NMOS_VTL
V1 A 0 PULSE(0 'supply' 10ns 1ns 1ns 50ns 100ns)
V2 B 0 'supply'
V3 VDD 0 'supply'
.END
```

Fig. 3. Netlist for 2-input NAND gate

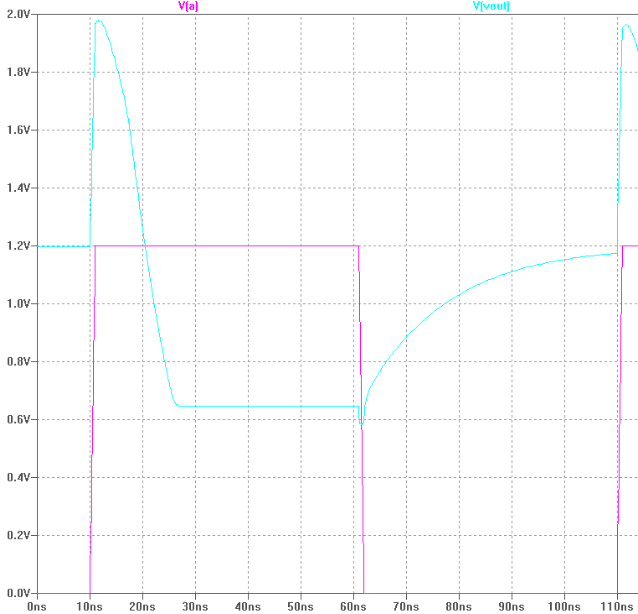

Fig. 4. Plot of A and Vout of 2-input NAND gate

III. Direct Gate Tunneling

A. Components

When the gate is biased positively with respect to the substrate the gate tunneling current is composed of two main components:

1) a current of minority carries tunneling from the semiconductor substrate to the gate (J), and
2) a current of majority carriers tunneling from the gate to the semiconductor substrate (J').

B. Components

Electrons in channel may tunnel through the oxide if there exists an empty state associated with exactly the same energy at the gate side. The probability of finding an empty state is given by

$$1 - f(E) \tag{1}$$

where f(E) is the Fermi level distribution function in the gate. The overall probability, P(E), for an electron energy E to tunnel from the channel to gate is

$$P(E) = T(E)[1 - f(E)] \tag{2}$$

where T(E) is the single electron tunneling probability and is derived using Wentzel-Kramer-Brillouin (WKIB) approximation [3]. The maximum potential barrier height at the Si/SiO$_2$ interface is denoted by χ. The potential well is modeled as a trapezoid as shown in Fig. 5.

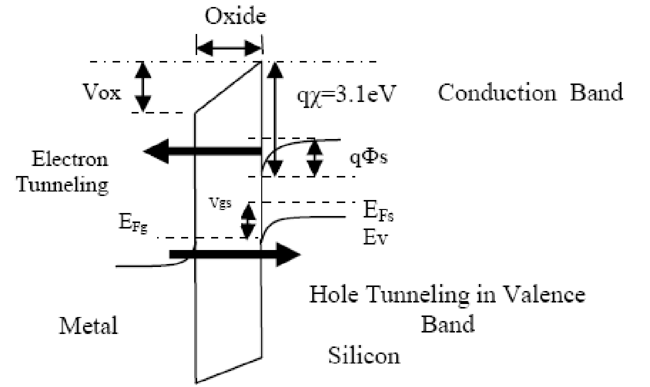

Fig. 5. Energy band diagram for nMOS structure [3]

C. Model

An equation describing the tunneling current density has been developed using the following relation

$$J = qvn \tag{3}$$

where q is the electron charge, v is the average tunneling velocity, and n is the tunneling electron density. The volume density of tunneling electrons can be expressed as a function of tunneling velocity as follows

$$n = \int_0^\infty n(v)P(E)dv \tag{4}$$

By substituting equations (4) into equation (1) the tunneling current density, J, from channel to gate is defined as

$$J = \int_0^\infty qvn(v)P(E)dv \tag{5}$$

The net tunneling current is then expressed as

$$J = J - J'$$

$$J_T = \left(\frac{4\pi m_e^{*3}}{h^3}\right)(kT)^2\left(1 + \frac{\gamma kT}{\sqrt{E}}\right) \left[1 - \exp\left(-\frac{qV_{gs}}{kT}\right)\right] \exp\left[\frac{q\Phi_s - q\Phi_B - \frac{Eg}{2}}{kT}\right] \exp\left[\left(\frac{2\gamma\sqrt{E}}{3}\right)\left(3\sqrt{q\chi E'}) + \frac{qV_{ox}^2}{E}\right)\right] \tag{6}$$

where k is Boltzmann's constant and

$$\gamma = 4\pi t_{ox}\sqrt{2m_{ox}}/h$$
$$E' = q\chi - 0.5qV_{ox}$$

$$E = q\chi + qV_{ox}\left(\frac{x}{t_{ox}}\right)$$

where h is Planck's constant and $V_{ox}=V_{gs}-V_{FB}-\Phi_S$, V_{gs} is the gate voltage, V_{FB} is the flat band voltage, and Φ_S is the surface potential of the channel [3]. Plots showing J_t vs. V_{gs} for n-type MOSFET operating in inversion mode are shown in Fig. 6. Plots from a different model which takes a purely quantum mechanical approach to solving the tunneling current density is shown in Fig. 7. The plots are in close agreement with one another.

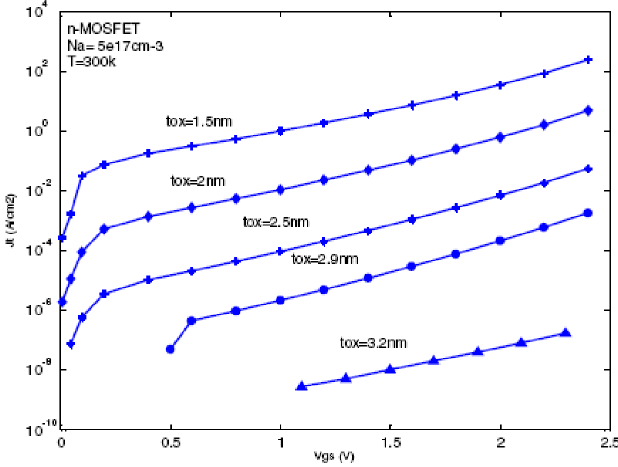

Fig. 6. Direct tunneling current density J_t(A/cm^2) versus V_{gs}(V) in n-MOSFET at various oxide thicknesses [3]

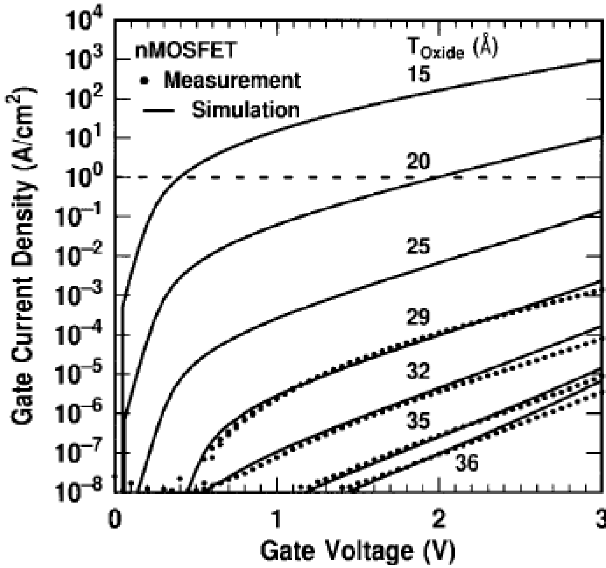

Fig. 7. Direct tunneling current density J_t(A/cm^2) versus V_{gs}(V) in n-MOSFET at various oxide thicknesses [4]

IV. Temperature Dependent Factors

A. Temperature Impact on Fermi Level

In general, for a p-type substrate the Fermi level E_{FS} approaches the acceptor ionization energy EA as temperature decreases and the Fermi level approaches the intrinsic energy level E_I as temperature increases. Fig 8 depicts the change of Fermi level with temperature. Impurities are considered weakly ionized at temperatures below T_S and the substrate is considered intrinsic at temperatures above T_i.

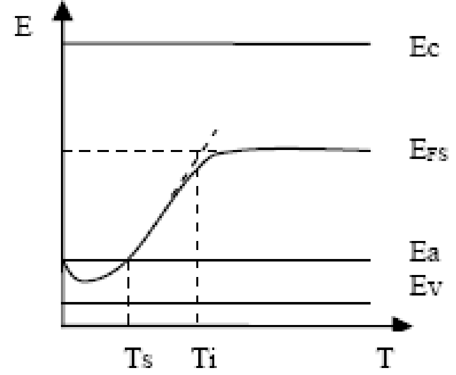

Fig. 8. Variation of Fermi level with temperature in NMOS device [5]

EFS can be estimated analytically by

$$E_{FS} = E_A - kTln(\alpha) \tag{7}$$

where $\alpha = \frac{-1+\sqrt{1+16\left(\frac{N_A}{N_V}\right)\exp(E_1/kT)}}{8}$

where E_1 refers to the acceptor ionization energy. A plot of Fermi level against temperature for N_A=1e17 cm^{-3} is shown in Fig. 9. A more accurate calculation of the Fermi level can be made by solving the charge neutrality equation numerically. A plot of Fermi level against temperature for N_A=1e17 cm^{-3} is generated using the charge neutrality condition and is shown in Fig. 10.

B. Temperature Impact on Energy Band Gap

The energy band gap tends to decrease with increasing temperature. Atomic vibrations increase with added thermal energy which in turn also increases the inner atomic spacing. The average potential seen by the electrons in the substrate decrease as the inner atomic spacing increases, thus the energy band gap of the substrate decreases. The energy band gap E_g for silicon is determined by

$$E_g = E_g(0) - \frac{\alpha T^2}{\beta + T} \tag{8}$$

where Eg(0) = 1.166 eV, α = 0.473 meV/K, and β = 636 K. A plot of the energy band gap against temperature is shown in Fig. 11.

C. Temperature Impact on Intrinsic Carrier Concentration

The intrinsic carrier concentration ni is a strong function of temperature as described by

$$n_i^2 = BT^3\exp\left(\frac{E_g}{kT}\right) \tag{9}$$

where B = 1.08x10^{31} K^{-3}cm^{-6}. A plot of the intrinsic carrier concentration against temperature is shown in Fig. 12. The three temperature dependent factors discussed previously all affect gate tunneling current. The inclusion of the three factors into the equation for gate tunneling current allows for further study of the temperature dependence of gate tunneling current density.

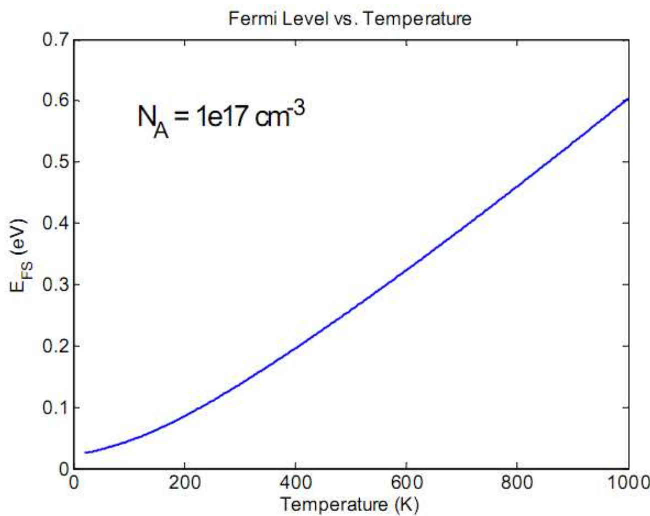

Fig. 9. Fermi level versus temperature using equation (7)

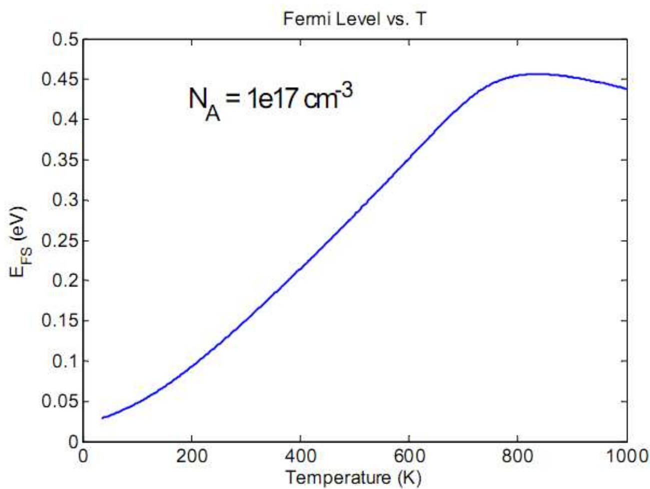

Fig. 10. Fermi level versus temperature using charge neutrality condition

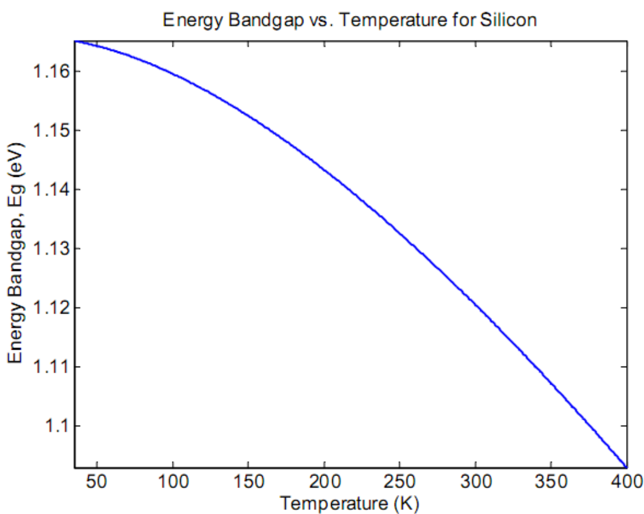

Fig. 11. Energy band gap versus temperature for silicon

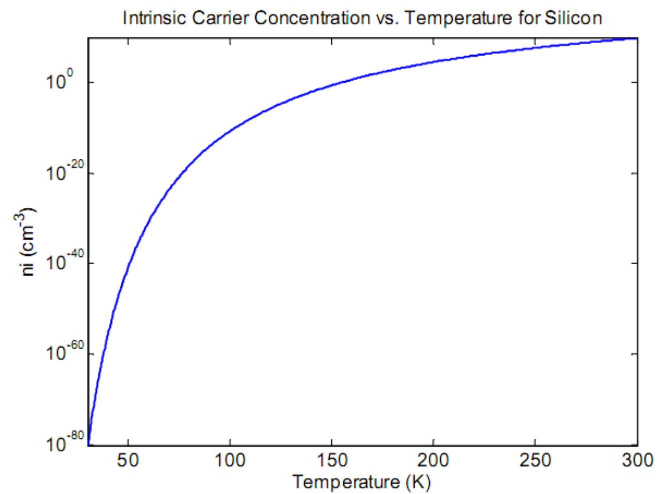

Fig. 12. Intrinsic carrier concentration versus temperature for silicon

V. Effect of Temperature Variation on Gate Tunneling Current

A. *Effect of Temperature Variation on Gate Tunneling Current at 90 nm Technology Node*

A plot of gate tunneling current density against temperature (V_{gs} = 1V) for 90 nm technology is shown in Fig. 13. The J_{limit} as specified for the 90 nm technology node by ITRS is 188 A/cm^2 [2]. Fig. 13 shows that nMOS devices with an equivalent oxide thickness (EOT) of 1.2 nm can be operated up to 370 K without exceeding the J_{limit} while a nMOS device with an EOT of 1.1 nm can only be operated up to 240 K without exceeding the J_{limit}.

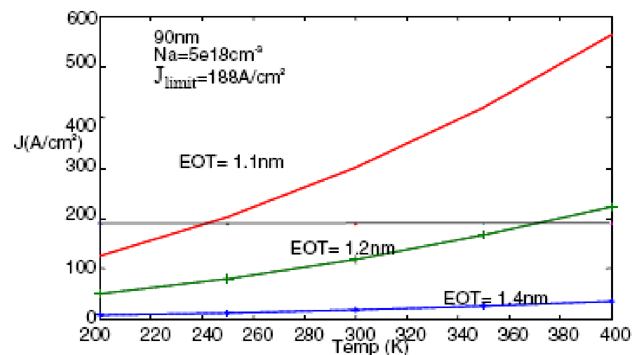

Fig. 13. Variation of gate tunneling current at 90 nm technology node for different values of EOT [3]

B. *Effect of Temperature Variation on Gate Tunneling Current at 65 nm Technology Node*

A plot of gate tunneling current density against temperature (V_{gs} = 1V) for 65 nm technology is shown in Fig. 14. The J_{limit} as specified for the 90 nm technology node by ITRS is 800 A/cm^2 [2]. Fig. 14 shows that nMOS devices with an EOT of 1.2 nm and 1.1 nm are well below J_{limit} at 400 K while a device with and EOT of 1 nm can only be operated up to 315 K without exceeding the J_{limit}.

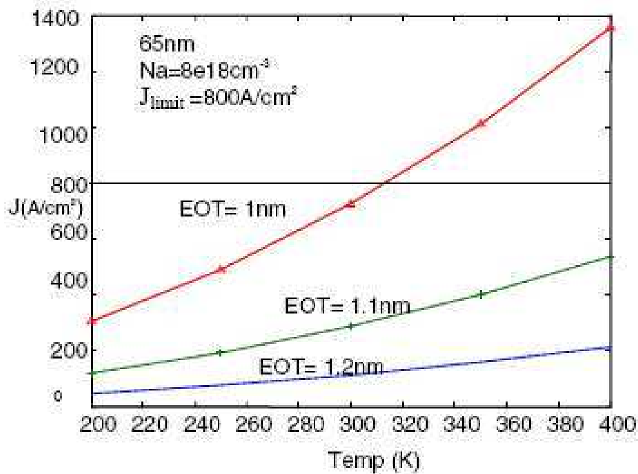

Fig. 14. Variation of gate tunneling current at 65 nm technology node for different values of EOT [3]

C. Effect of Temperature Variation on Gate Tunneling Current at 45 nm Technology Node

A plot of gate tunneling current density against temperature (V_{gs} = 1V) for 45 nm technology is shown in Fig. 15. The J_{limit} as specified for the 45 nm technology node by ITRS is 1560 A/cm^2 [2]. Fig. 15 shows that nMOS devices with an EOT of 1.2 nm and 1.1 nm are well below J_{limit} at 400 K while a device with and EOT of 1 nm can only be operated up to 280 K without exceeding the J_{limit}.

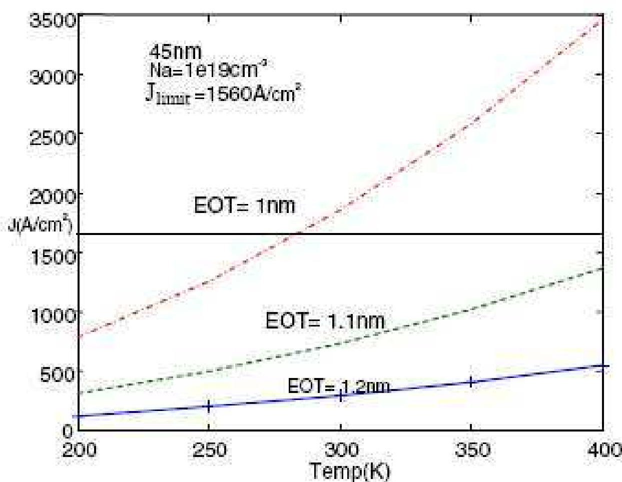

Fig. 15. Variation of gate tunneling current at 45 nm technology node for different values of EOT [3]

D. Effect of Temperature Variation on Gate Tunneling Current at 32 nm Technology Node

A plot of gate tunneling current density against temperature (V_{gs} = 1V) for 32 nm technology is shown in Fig. 16. The J_{limit} as specified for the 32 nm technology node by ITRS is 2430 A/cm^2 [2]. Fig. 16 shows that nMOS devices with an EOT of 1 nm and 0.9 nm are well below J_{limit} at 400 K while a device with and EOT of 0.8 nm can only be operated up to 340 K without exceeding the J_{limit}.

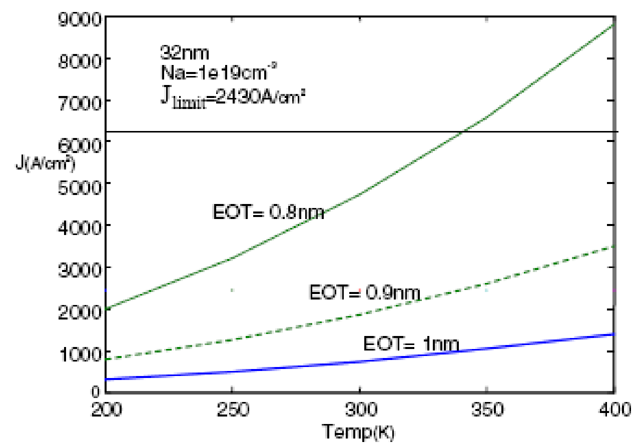

Fig. 16. Variation of gate tunneling current at 32 nm technology node for different values of EOT [3]

VI. CONCLUSION

For each technology node, leakage due to gate tunneling currents is not a strong function of temperature until the EOT becomes sufficiently thing. When designing a nMOS device for use in a high temperature environment (greater than 400K) it has been shown that the EOT must be considered. For the 90 nm, 65 nm, 45 nm, and 32 nm technology nodes nMOS devices with an EOT equal to or greater than 1.2 nm, 1.1 nm, 1.1 nm, and 0.9 nm respectively should be considered for use in high temperature environments. If a nMOS device is designed for use in a low temperature environment (less than 240 K) then the designer has much more freedom in choosing the EOT.

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