α_j are 0.5 in Fig. 5 and 0.75 in Fig. 6. Note that, in both cases, the filter gain margin does not decrease as the feedback delay increases (as one might expect), but presents a local maximum value (at $2.8T$ and $3.3T$ in the first case and $0.25T$, $1.4T$ and $3.2T$ in the second case).

Conclusion: In this Letter, we have shown that the method proposed in [2] could be used even in the case where non-neglectible values of feedback delay are encountered. A very interesting conclusion is that an optimal gain margin may be reached with a nonzero value, i.e. a physical delay value. Furthermore, this delay (higher than one sampling period) allows for dynamic element matching techniques in the case of multibit modulators.

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P. Benabes, P. Aldebert, A. Yahia and R. Kielbasa (*École Superiéure d'Électricité, Service des Mesures, Plateau de Moulon, 91192 Gif-sur-Yvette, France*)

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Low power flip-flop with clock gating on master and slave latches

A.G.M. Strollo and D. De Caro

A new flip-flop is presented in which power dissipation is reduced by deactivating the clock signal on both the master and slave latches when there are no data transitions. The new circuit overcomes the clock duty-cycle constraints of previously proposed gated flip-flops. The power consumption of the presented circuit is significantly lower than that of a conventional flip-flop when the *D* input has a reduced switching activity.

Introduction: In recent years the desire for portable computing has steadily grown; the reduction of power dissipation is a crucial factor in IC design [1]. In many applications, the power consumption of the IC clock system is one of the main sources of chip power dissipation. This is due to the high switching activity and the heavy capacitive loading of the clock network. Consequently, many techniques have been recently proposed to reduce clock system power dissipation. In particular, in [2, 3] new flip-flop designs were presented in which the power consumption is reduced due to the clock signal being deactivated (clock gating) when there are no transitions on the *D* input. Unfortunately, previously proposed clock-gated flip-flops exhibit significant limitations. They require the use of a fine-tuned sub-nanosecond pulse generator to be shared among several flip-flops [2] or necessitate having hard constraints imposed on the clock duty-cycle to avoid timing failures [3]. In this Letter we present a new flip-flop design in which the gating technique is used for both master and slave latches, overcoming the limitations of previously proposed approaches. For a low level of input data switching activity, the power dissipation of our circuit is much lower than that of a standard (non gated) flip-flop, with a 64% power saving when the *D* input is idle.

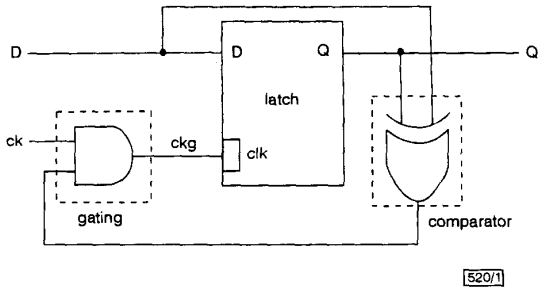

Fig. 1 *Positive level-sensitive latch with clock gating*

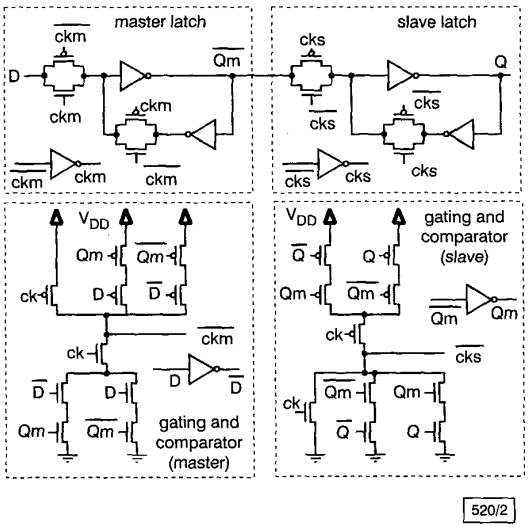

Fig. 2 *Schematic diagram of proposed circuit*

Master and slave latcher are realised with transmission gates and are both gated

Proposed circuit: A simplified schematic diagram of a gated latch is shown in Fig. 1. The latch is positive level-sensitive (it is transparent when $ckg = 1$ and on hold for $ckg = 0$). The comparison between *D* and *Q* is performed by an XOR gate, while the gating logic circuit compromises a simple AND gate. The operation of the circuit is as follows. If *ck* is 0, then *ckg* is also 0 and the latch is correctly in the hold state. On the other hand, when *ck* is high and *D* is different from *Q*, the gating logic enables the *ckg* signal so that the latch can correctly switch. Note that if *D* is equal to *Q* the gating logic inhibits the propagation of switching activity from *ck* to *ckg*. In this way the power consumption is reduced, assuming that the capacitance on the *ckg* node is higher than the input capacitance of the gating logic.

It is worth noting that the approach shown in Fig. 1 cannot be straightforwardly applied to an edge-triggered flip-flop. In this case a change of *D* while *ck* is high can cause a commutation of *ckg*, triggering the flip-flop. In previous work this problem has been avoided either by allowing *D* to change only when *ck* is low (that is, by imposing a timing constraint on the clock duty-cycle [3]), or by using a fine-tuned sub-nanosecond clock pulse generator [2]. A low-power clock-gated flip-flop that overcomes the limitations of previously proposed approaches can be easily designed by cascading two clock-gated latches in a master-slave configuration. Note that a negative level-sensitive clock-gated latch is quite similar to the schematic circuit diagram shown in Fig. 1, the difference being in the gating logic (implemented with an OR gate) and in the comparator logic (implemented with an XNOR gate). Fig. 2 shows, as an example, the schematic diagram of a clock-gated flip-flop in which latches are simple static transmission-gate circuits. The circuit has been designed joining the comparator and the gating logic in a single complex CMOS gate. In this way the number of nodes is reduced, with a further limitation on the power consumption.

Simulation and results: The flip-flop of Fig. 2 has been designed to layout level for 0.8μm technology. For all NMOS devices, W/L = 3.6μm/0.8μm, while for all PMOS devices, W/L = 7.2μm/0.8μm. The circuit was extracted from the layout, including parasitics, and simulated using SPICE with a supply voltage of 5V. For comparison, a conventional flip-flop was also designed to layout level with the same device sizing, and simulated. The SPICE simulation of Fig. 3 shows correct circuit operation, without timing failures, for a 50% duty-cycle clock signal and in the presence of glitches on the D input.

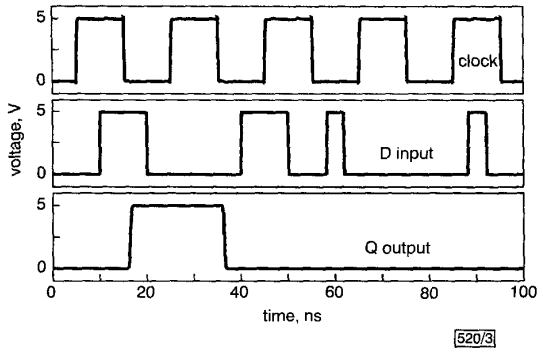

Fig. 3 *SPICE simulation of new flip-flop*

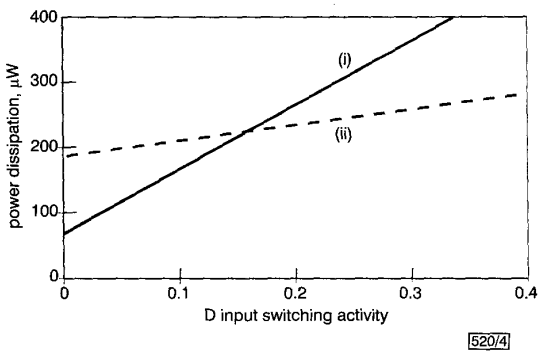

Fig. 4 *Power dissipation of flip-flop of Fig. 2, compared with that of conventional, non-gated circuit, against D input switching activity*

Clock frequency: 50MHz
(i) proposed flip-flop
(ii) conventional flip-flop

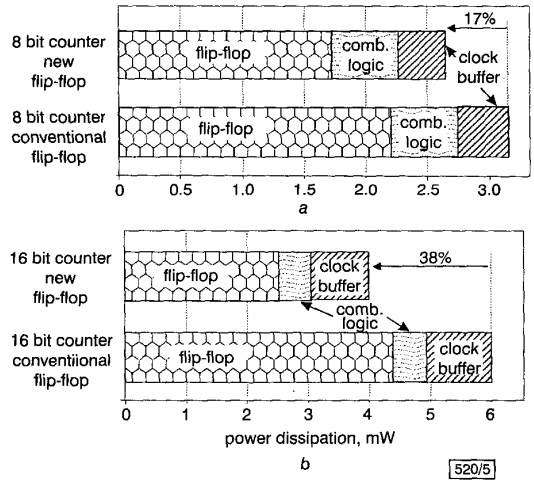

Fig. 5 *Power dissipation of 8 and 16 bit counters implemented with standard and clock-gated flip-flops*

a 8 bit counter
b 16 bit counter

To estimate the power consumption, many simulations were performed by varying the switching activity of the D input. The switching activity is defined here as the average number of transitions of D in a clock cycle. The result of simulations with a clock frequency of 50MHz is shown in Fig. 4. The best reduction of power consumption is achieved when D is idle. In this case the power dissipation of the gated flip-flop is only 36% of that of a conventional flip-flop. The proposed circuit, however, gives higher power dissipation than the conventional flip-flop when the D switching activity is > 0.16. Therefore clock-gated flip-flops are best suited in applications in which data switching activity is kept low [2, 3]. An example is a binary counter, in which the input switching activity of each flip-flop is known beforehand and is equal to 2^{-k} for the kth bit. This suggests the use of standard flip-flops for the lower-order bits (with high switching activity) and of clock-gated flip-flops for the remaining bits [3].

To investigate the performances of the clock-gated flip-flops proposed in this Letter in counter applications, two 8 bit and 16 bit counters were designed to the layout level and simulated. Note that, on the basis of the results of Fig. 4, conventional flip-flops have been used for the bits from 0 to 2, as in this case the switching activity is >0.16 and the power consumption of the clock-gated flip-flops is larger than that of standard flip-flops. Simulation results are shown in Fig. 5, where the power dissipation of counters employing only standard flip-flops is also reported, for comparison. The use of clock-gated flip-flops results in a power saving of 17% for the 8 bit counter and of 38% for the 16 bit counter.

Conclusions: In this Letter a new low-power flip-flop design in which a gating technique is used for both master and slave latches is presented. The new circuit represents an improvement on previously proposed approaches [2, 3] at the cost of an increased circuit complexity. The use of the proposed clock-gated flip-flop results in a significant power saving when the input signal switching activity is low.

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A.G.M. Strollo and D. De Caro (*Department of Electronic and Telecommunication Engineering, University of Naples 'Federico II', Via Claudio 21, 80125 Napoli, Italy*)

E-mail: strollo@diesun.die.unina.it

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Modified asynchronous wave-pipelining

Chansub Park and Duckjin Chung

A modified asynchronous wave-pipelining design method for optimising circuit performance is presented. Using this method, the number of latches in the circuit can be decreased compared with the asynchronous wave-pipelined circuit that uses latches at every gate level. As a result, the latency of the circuit can be reduced drastically and the number of delay elements used in the wave-pipelined circuit can be decreased. To verify the proposed method, the authors have designed an 8 × 8 multiplier and performed simulations using HSPICE. The latency of the multiplier decreased by 40% when compared with the asynchronous wave-pipelined circuit and a delay latch replaced two delay elements that were used in the wave-pipelined circuit. The designed multiplier works well at 1GHz.