Zeru Zhang

**Part V Report**

(a) What did you learn from this project?

At first, I learnt how to design a digital system by using VHDL language and FPGA media. Secondly, during debugging of the design, I gained a deeper comprehension about how do a single-cycle cpu work. And also, by practicing with Modelsim and Quantus softwares, I grasped the basic points to handle them. Together, my skill in VHDL programming become more proficient. What's more, I learnt the way how digital circuits are synthesized with FPGA software.

(b) What would you do differently next time?

Next time I will try a multi-cycle cpu design.

(c) What is your advice to someone who is going to work on a similar project?

Don't be haste to choose your cpu type.

Consider the realistic conditions we have when writing the VHDL code.(reset is negedge triggered, memory just have one signal to select write or read, LED must be added in the topmodule)

Make sure your design do work correctly in Quantus invoked simulation before you burning the circuit.

If you circuit wouldn't work on the board, try slower clock frequency or using button to generate test clock for the design.