**CPU Design Project – Part 6 – Hardware Implementation and a Working Processor Demo**

**ELEC 6200 – Report and Demo Required**

**ELEC 5200 – Only Report required, Demo Optional**

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**Report Due Friday, 5/1/2015**

1. Follow the [Altera Quartus II and DE2 Manual](http://www.eng.auburn.edu/~vagrawal/COURSE/E6200_Fall10/HW/HW3/Altera%20Quartus%20II%20and%20DE2%20manual.pdf) (posted on course website) for designing and implementing your circuit on the FPGA.
2. Reset can be connected to any of the 4 Keys on DE2 Board. These Keys are normally at logic ‘1’. And pressing them will change the logic to ‘0’. So make the changes in your design as needed.
3. Clock can be connected to any of the two free-running clock frequencies available, 27MHz and 50MHZ. To connect to any of these clock inputs, the pin numbers are mentioned in the [Pin Assignment MSExcel](http://www.eng.auburn.edu/~vagrawal/COURSE/E6200_Spr08/PROJECT/DE2_pin_assignments.csv) sheet. You can also debug your design by connecting the clock to one of the manual keys on the DE2 board, manually creating clock pulses instead of using free-running clock.
4. The “inr” input that selects the register number can be connected to any 4 switches on the board. And the “outvalue” that displays the contents of the register selected, can be connected to the LEDs or LCD on the board. For using 7 segment displays on the board you will require a [HEX to 7 segment](http://www.eng.auburn.edu/~vagrawal/COURSE/E6200_Fall10/PROJECT/hexto7seg.vhd) conversion model provided on the course website.
5. Run the test program and verify the results with your simulation in part 5.
6. You will have to show the implemented design on your DE2 Board. You will be conducting a demo as follows:

(a) Briefly describe what is implemented, what program you will run and what result is expected.

(b) Run the program pointing to the functions of the buttons you press. Let the viewer examine the result.

(c) Offer to make a change to some parameter to a viewer selected value and rerun the demo.

(d) Total duration of demo: FIVE MINUTES.

1. **Part 6 report must be a one-page reply to three questions:**
2. **What did you learn from this project?**

**From the course of “Computer Architecture and Design”, I reviewed some courses taken during my undergraduate study. This course tells me how to design a virtual CPU, how to set Datapath and also VHDL.**

1. **What would you do differently next time?**

**This time we use multi-cycle. As a matter of fact, we wanted to use pipeline, but failed. Next time we are going to try out again.**

1. **What is your advice to someone who is going to work on a similar project?**

**This board sometimes doesn’t run well. When you want to put the compiled program to the FPGA board, you should be very patient. It usually takes about 3 mins to run the program and 2 mins to put the program to the board. So please be patient!**

**(d) Email report to** [**vagrawal@eng.auburn.edu**](mailto:vagrawal@eng.auburn.edu)