**CPU Design Project – Part 6**

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1. **What did you learn from this project?**

We learned a lot about how the data path in a CPU works. Prior to this project we had a basic idea as to how the data path worked, however now we fully understand how information is transferred from memory to the CPU where a task is performed and back to memory once the desired operation is finished. Also when building the data path we learned about timings in a multicycle operation.

It is a good experience for us to use the knowledge which learned from the course to do this project. For example, we need to design our instruction set architecture for a new 16-bit microprocessor that help us understand deeply about ISA. Then, we use the VHDL to write codes designing the every part of CPU and modalism software to do simulation. Finally, we simulate our processor on the Altera FPGA board provided in the lab and how to use the In-System Memory tools to run our test program.

1. **What would you do differently next time?**

First thing we would like to do differently next time is to try a different type of data path. At beginning, our team chose multicycle data path, however, after learning pipeline, we realize that pipeline would be more efficient than multi-cycle data path. Although pipeline would make this project more complicated, it also has many advantage that single cycle and multi cycle data path do not have. And then, we would worry less about reducing our total number of opcodes (since we only ended up with 8 or so by cleverly using the function argument) and worry more about what each opcode would need to influence on the board.

1. **What is your advice to someone who is going to work on a similar project?**

Although this project was really well laid out and well prepared, there are a few things which we think can improve the outcome of designs. As with our design, a lot of people ran into problems when trying to synthesize the board on the Altera FPGA. To prevent this we would recommend using the Altera board earlier in the project. Reviewing VHDL ahead of time.