CPU Design: Part 6 – Feedback Report

ELEC 5200

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1. Through the completion of this project, our team became much more familiar with the low-level architecture of a computer system. We gained further exposure to the CPU datapath and memory accesses required to execute a single instruction, and how the improve the efficiency of a CPU by retiring instructions at a quicker rate. We applied and improved our VHDL abilities and had to perform circuit simulation and verification.

Further, we gained an understanding of how instructions are decoded into a series of control that manage the execution of instructions.

1. If we were to do the project again, our team would likely implement a multi-cycle datapath for instruction execution. Implementing a single-cycle datapath initially appeared to be the simpler option. However timing concerns made the system cumbersome in parts. For instance, additional control signals were required to indicate to the program counter that a new instruction may be fetched. Had we implemented a multi-cycle datapath, the PC could be incremented on each rising clock edge and the architecture would be simplified.
2. Our advice to someone working on a similar project is to plan ahead and begin early. The project consumed a very large portion of our time devoted to school work, and any concerns not addressed as early as possible became much more problematic as the project went on. Think hard about timing constraints and the performance of the datapath operating on a clock.