**What did you learn from this project?**

This project gave us a hands-on experience in designing and implementing a micro-processor. We learned how to create an entire hardware/software system from the scratch. We became familiar with VHDL language, Modelsim , Quartus tools and programming on Altera FPGA Boards. This project also gave us a complete understanding of the multi-cycle datapath. We now understand the different steps involved in designing a multi-cycle datapath. The most challenging part was designing the FSM and integrating the Control Unit with the datapath. Through this project, we became familiar with using Quartus II with ModelSim to initially simulate, test, run and debug our CPU. In the final step of the project, we learned how to simulate our processor on the Altera FPGA board provided in the lab and how to use the ‘In-System Memory’ tools to run our test program straight from the Quartus software. Overall, the project was an up-hill task, but it was a great exciting learning experience for us.

**What would you do differently next time?**

Given a second chance, we would start really early and be ahead of the deadlines. Starting early would give us enough time to try running diverse and complex programs on our processor and better understand the errors we may run into.

We would also start off working with the Altera Quartus tools as soon as possible, so that we can resolve the errors created while running the code on the board. For example, we faced problems while running combination of ‘branch’ and ‘jump’ instructions for executing loops. Individually the two instructions were running fine, and there were no errors in the ModelSim simulations. But at the last moment when we tried to run the test program, the program was skipping the second instruction of the loop. We believe the problem was related to the updating of the program counter, but we could not look into the issue due to lack of time.

Now that we believe we understood multicycle datapath, next time we would implement the Pipelined dathapath with Hazard Detection and Forwarding unit.

**What is your advice to someone who is going to work on a similar project?**

We would like to recommend future students to start the project as early as possible. The project may look straightforward but one should not wait until the last minute as it becomes tricky in the later parts. For debugging, one needs to thoroughly check each component in the datapath one by one which is time consuming. We would suggest that students, who prefer to implement the multi-cycle datapath, to do the datapath verification part along with the Control Unit part. This would help them verify their datapath successfully. Verification of the datapath after designing the control unit becomes much simpler. One should start to work with the Altera Quartus tool as soon as possible, as it brings on a lot of issues to be resolved. Working in a group from the first part is a better option as it helps a lot. Finally, when stuck with any issues, do not hesitate to ask the professor, GTA or fellow students.

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