**CPU Design Project: Part 6**

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1. **What did you learn from this project?**

In this project, we learned how to use Quartus and Modelsim to complete the simulation of the project. Although we are not very familiar with Verilog HDL at the beginning, after the whole CPU design procedures finished, Verilog HDL is not as hard as we thought before. We implemented a multicycle datapath. If we didn’t implement it ourselves, we would never know the importance of control signals and time sequence. Our CPU component works properly in the project 4, but when we combine them together, the whole system broke down. The error in the FSM leads to the problem. So we spend nearly one day to rewrite the control signal table. It’s really important.

1. **What would you do differently next time?**

To be honest, if we do the project again, we will design an easier datapath. And we will take more time to think comprehensively before we start. Because every single step of the project will affect the final design. On the other hand, we will simulate our design as early as possible on Altera board. Even though the computer simulation seems perfectly, the actual situation always shows some new problems.

**(c) What is your advice to someone who is going to work on a similar project?**

As a beginner, choosing the right datapath is really important. The design is always harder and more complex than you expect. Some design beyond your ability will drive you exhausted. Starting early on hardware is another important advice. The design always break down on the board but not on the computer. Thirdly, be patient. The project is enormous, some parts are lengthy. Patience makes you more effective. The most important point is that people should think comprehensively before the project starts. If you want to change an instruction in the final parts, perhaps it means you need to change a lot about your datapath.