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ELEC 5200 – Computer Architecture

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CPU Design Project Part 6

(a) What did you learn from this project?

From this project, I learned about the design process and got hands on experience concerning a CPU design. It was helpful to be able to connect what we learned in class to the project sections along the way. The first installment of the project showed me how difficult it was to define an instruction set that will accomplish all the tasks required. We spent a significant amount of time trying to ensure our instruction set would serve all required needs as well as make the programs written flow easily for the author. I also got a refresher in VHDL which will be useful in my job next semester.

(b) What would you do differently next time?

Next time I would attempt to coordinate the clocks better to allow for a single clock rather than multiple clocks. My group used a total of 5 clock signals to correspond to the 5 cycles. This was very helpful in the simulation because it ensured our components always executed in the correct order, but I would have liked for the 5 clocks to derive their cycles from a master clock input to make simulation setup more straightforward.

(c) What is your advice to someone who is going to work on a similar project?

I would advise someone who is starting a similar project to execute the single cycle design. I believe the datapath was easier to construct and troubleshoot than a multicycle or pipelined datapath. Also, I would advise them to thoroughly test each of their components and their connections. It saves time in the long run to spend the time upfront rather than try and debug the datapath as a whole if you know the pieces are correct.