**CPU Design Project: Part 6**

**Hardware Implementation and a Working Processor Demo**

ELEC6200 Due Monday, 12/7/2015

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**What did you learn from this project?**

By doing this project, we are enchanted by the field of computer architecture. We learned Von Neumann architecture by designing memory. We learned knowledge about the component of CPUs, and designed pipeline datapath which is more efficient and consume less energy. We also finished the datapath diagram with the hazard control. we implement the control unit and add hazard detection into the datapath. And we write VHDL code and test VHDL models of each individual component. We also learned how to write top-level which works with a single memory. By using modelism we simulated the whole CPU which can fulfill all the tasks that are needed. In the last part we use quartus to compile, simulate and run on the FPGA.

**What would you do differently next time?**

This time, we designed pipeline datapath and run on the FPGA. Although the result fulfills the expectation, the efficiency of our CPU is not altered to its ultimate ability. If we will design it for the second time, we will improve the efficiency. Besides, we will try single path or multicycle to learn more about processor, since we already finished the pipeline. At this time we did this project step by step, because when we did the first part, there are much knowledge that we have not learned from the course. Next time, we will see this project as a whole instead different parts, so we will design whole processor instead of altering it for many times.

Currently, our instruction can be download into the board, but we still cannot initialize the data memory. So we have to use the in system content memory editor to initialize the data. In the rest of this week, we will try to figure it out.

**What is your advice to someone who is going to work on a similar project?**

First, we strongly recommend that the one who does this project should record the alternation and every change. If the alternation and change are not carefully recorded and the error cannot be fixed, it is hard to return to its original status without reprogramming everything.

Second, we are strongly recommend that one should learn the VHDL ahead of time, because the VHDL is used in many part of this project and it takes a lot of time to write and compile the code without errors for the starters.

Third, we recommend new students to choose pipelined implementation, because the pipeline is of significance in this course. Doing is project of pipeline can help us understand the knowledge better. The pipe line is more complex than the single cycle, so if one master the pipeline, he or she will also find it is easy to mater single cycle or multicycle.

Fourth, the quartus in the lab is 15 version, which cannot be used on the DE2 Board in the lab. It is different from the manual. It takes hours for us to realize that the 15 version cannot work. So new students should setup 13 version on their own computer to accomplish the request.