**CPU Design Project – Part 6**

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1. **What did you learn from this project?**

The CPU design project lead us to a better understanding of the architecture and the operation of a processor. We used a single cycle data path for our processor. The initial stage was easy and straightforward. Once all the components were created, putting them together became a nightmare. We learned that port mapping a top-level model is not as easy as it sounds. We also learned how to use two software tools: ModelSim and Altera Quartus II IDE. ModelSim is mostly used for simulation of the VHDL model. We have become more familiar with testing and debugging the VHDL model by using ModelSim. For Quartus II, we learned how to build a memory module and use it in the CPU project.

1. **What would you do differently next time?**

Next time, I would take more time to think about the top-level model. Since it’s the heart of project, anything wrong with component connections will cause errors. We believe this was the source of many of our errors. Additionally, we might try to use multiple cycle data path or pipeline for our CPU. Since we have gained experience on single cycle data path, it would be benefit for us to learn a little more about multicycle and pipeline.

1. **What is your advice to someone who is going to work on a similar project?**

The biggest advice for you is to understand your CPU. Take time on the design portion of the project. Understand each component of the CPU, get an idea of how each work, and how they are related to other components. The better understanding, the less confusion you will have. Another piece of advice is to do more simulation on all the components. When simulating each of the components, instead of simulating just for functionality, try simulating typical inputs based on your designed ISA. Also, keep very good track of the size of all inputs and outputs to avoid frustration during compilation.