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SECTION: ELEC 5200, MWF 11:00  
DATE: 5 December 2015  
SUBJECT: Project Part 6: Final Report

**What did you learn from this project?**

This project was an excellent introduction to datapath design and provided an excellent introduction to all aspects of CPU design. I learned how to conceptualize and develop an ISA for a set sized microcontroller that covers all basic C programming constructs. I learned how to convert these instructions into assembly and machine language formats for use with a real datapath. Once this ISA was created, I learned how to conceptualize and design a RTL model of a datapath to implement an instruction set. I learned how to integrate registers, ALUs, MUXes, and various other components into a working datapath. Once this was done, I learned how to convert the previously designed instruction set into a set of control signals so that they could actually be executed on the datapath. I learned how to take this conceptual RTL model and design actual VHDL components for it, then how to integrate these components into a top level model of the entire unified datapath. I then learned how to integrate memory blocks and troubleshoot the datapath to create a working system.

**What would you do differently next time?**

I can’t think of anything I could change to make the project significantly easier, so I would create a Harvard architecture, and possibly a pipelined datapath. Both would, I feel, make the project more difficult to complete, but they would provide an opportunity to learn even more than I did during this project. Whether or not I made any changes to the structure of the project, I would spend more time planning the ISA and the datapath to reduce the number of problems encountered in the rest of the design.

**What is your advice to someone who is going to work on a similar project?**

To plan the ISA and RTL models up front as thoroughly as possible. Most of the problems I encountered with this project were because of overlooked problems in the design of my ISA or original conceptual datapath. Fixing these problems required revisions in my ISA which then rippled throughout the rest of the stages of the design. Had I been able to eliminate these problems up front I would have been able to eliminate a large amount of extra work I was forced to undertake.