Project Report

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This project is heuristic and enlightening for us to process the further study of Computer Hardware in a practical way with FPGA and relative software like Modelsim and Quarters II. To make preparation for that we learned the VHDL.Necessarily, a whole task should be divided into several parts and then be done step by step. Making collaboration with your group members is always an effective path to get the ideal result. We interpret the individual points and brainstorm and finally reach consensus.

In this project, we selected the multi-cycle model as architecture but actually it may not be a wise choice when trivial contents considered in part 4 and 5.We met several problems in later stages and have to check backward to find errors and make it revised to keep consistence with the other parts. I think we would choose the pipeline or single-cycle next time for their simpler architecture. It would be better to make test on FPGA board before the last week to find the problems and solve them in time to avoid the accumulation of errors.

About advice, I think it is significant to make a considerate and specific plan before you process the first part to make sure you are in the right direction to avoid some critical errors may occur later. Keep patient when you met problems, and take full advantages of the references offered by professor to find the way out. If you are in group, make certain of the task distributed to each member for lassitude would possibly be your enemy.