**What did you learn from this project?**

In this project I learned a lot about how a processor is created and how it works. I also learned how complicated it is to synthesize a processor in VHDL. I mostly knew how to program in VHDL already so that was not a difficult part for me. I mostly had trouble with working on the ISA instructions and creating the data path. I wasn’t sure if my design would work until I got to the VHDL stage so I had a hard time decided how to create my instructions and my datapath. In the end I decided to go with a single stage datapath because it seemed like it would be the easiest to implement for a beginner like me. I learned a lot about how to create a datapath as I worked. I learned that control signals are extremely important. I also learned that you do not need a very complex instruction set in order to implement basic C functions. I learned as I went along in this project what instructions were actually needed and which instructions I did not need to add to my CPU. When I got to the VHDL portion of the project I felt like I pretty much understood what I was doing. I did need to learn how to use arrays in VHDL for the register file. The arrays really helped me to easily implement a register file as well as an instruction memory. Overall I think this project really helped me get a better understanding of how a processor works. I learned a lot from the lecture but getting the hands on experience really helped solidify the concepts we learned in class.

**What would you do differently next time?**

If I could do this project again I think I would try to implement a pipelined datapath or a multicycle datapath instead of the single cycle datapath. I think it would have been a good challenge. I just felt like I did not have enough time this time around to implement a more complicated datapath. I am also really interested in the one-instruction instruction set that was discussed in lecture. I think this would be fun to try to implement even if it’s really not practical. As far as things I could have improved on in this project, I think I would have created a better instruction set. My instruction set basically did everything I needed it to but I think I could’ve definitely made a better instruction set that was less complicated than the one that I created and more like the MIPS instruction set that was discussed in class.

**What is your advice to someone who is going to work on a similar project?**

My advice for anyone about to do this project is take the first two parts very seriously. If you can create a good design for the first two parts then the VHDL and implementation will come naturally. Creating a good instruction set it very important because it affects how complicated your datapath is. If you create an instruction set that is too complicated it will be a lot harder to correctly implement the datapath. Second, the datapath part of the project is probably the most important part of the whole project. If you have a good datapath that is well drawn, then creating the VHDL models and connecting them should be a lot easier. Finally, it is really important to not overcomplicate things. I made the mistake of thinking that I needed extra instructions that I actually did not need. This made my datapath messy and hard to implement. I really regret that I did not make a simpler datapath from the start.