**CPU Design Project – Part 6 – Hardware Implementation and a Working Processor Demo**

**ELEC 5200 – Only Report required, Demo Optional (Extra Credit)**

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1. Follow the [Altera Quartus II and DE2 Manual](http://www.eng.auburn.edu/~vagrawal/COURSE/E6200_Fall10/HW/HW3/Altera%20Quartus%20II%20and%20DE2%20manual.pdf) (posted on course website) for designing and implementing your circuit on the FPGA.
2. Reset can be connected to any of the 4 Keys on DE2 Board. These Keys are normally at logic ‘1’. And pressing them will change the logic to ‘0’. So make the changes in your design as needed.
3. Clock can be connected to any of the two free-running clock frequencies available, 27MHz and 50MHZ. To connect to any of these clock inputs, the pin numbers are mentioned in the [Pin Assignment MSExcel](http://www.eng.auburn.edu/~vagrawal/COURSE/E6200_Spr08/PROJECT/DE2_pin_assignments.csv) sheet. You can also debug your design by connecting the clock to one of the manual keys on the DE2 board, manually creating clock pulses instead of using free-running clock.
4. The “inr” input that selects the register number can be connected to any 4 switches on the board. And the “outvalue” that displays the contents of the register selected, can be connected to the LEDs or LCD on the board. For using 7 segment displays on the board you will require a [HEX to 7 segment](http://www.eng.auburn.edu/~vagrawal/COURSE/E6200_Fall10/PROJECT/hexto7seg.vhd) conversion model provided on the course website.
5. Run the test program and verify the results with your simulation in part 5.
6. You will have to show the implemented design on your DE2 Board. You will be conducting a demo as follows:

(a) Briefly describe what is implemented, what program you will run and what result is expected.

(b) Run the program pointing to the functions of the buttons you press. Let the viewer examine the result.

(c) Offer to make a change to some parameter to a viewer selected value and rerun the demo.

(d) Total duration of demo: FIVE MINUTES.

1. **Part 6 report must be a one-page reply to three questions:**

**(a) What did you learn from this project?**

**(b) What would you do differently next time?**

**(c) What is your advice to someone who is going to work on a similar project?**

**(d) Email report to** [**vagrawal@eng.auburn.edu**](mailto:vagrawal@eng.auburn.edu)

**What did you learn from this project?**

From the project assigned for Auburn’s Comp 5200 Class – “Computer Architecture” I was introduced to

the concepts of RISC and how these components work together in order to create a program through

the use of machine code and assembly code. Using the machine code created for 16 RISC instructions

one would be able to create various components for the virtual CPU. This project shows that the

essentials of VHDL language is not enough to fully understand the complexity of the project and that

what would fundamentally work doesn’t necessarily means it will.

**What would you do differently?**

I would allocate more time in figuring out how to get the simulations to work properly. By simulation

results worked when you test each component yet failed to yield results when you focus solely on the

instructions. The issue lies somewhere within how I designed my ALU and how it isn’t correctly working

with the RISC instructions.

**What is your advice to someone who is going to work on a similar project?**

My advice is this, work on the project with another member who can trouble shoot problems. This will

allow for one person ( or the group) to design the project and the fundamentals as well as having one

person to go through and test to see if it will work. If the option of another member isn’t available then I

would advise that you speak with a class member about simulating the results or at least talk with

someone who is more will versed in procuring results in order to test code.